

Bi-Directional Double-Side
Double-Gate IGBT Fabricated by Wafer Bonding

F.J. Kub¹, K.D. Hobart¹, M. Ancona¹, J.M. Neilson², K. Brandmier³, and P.R. Waind⁴

¹Naval Research Laboratory, Washington, D.C. 20375, hobart@nrl.navy.mil

²JMSN, 2620 Egypt Road, Norristown PA 19403, jmsn@prodigy.net

³Silicon Power Corporation, Commercial Power Division, Latham, NY 12110

⁴Dynex Semiconductor, Doddington Road, Lincoln, United Kingdom LN6 3LF

The concept of a double-side, double-gate insulated gate bipolar transistor (DIGBT) was first proposed and simulated by Nakagawa [1]. Huang et al. later simulated a DIGBT with a trench gate structure rather than a DMOS topography [2]. It has been predicted that such a transistor is capable lower turn-off loss through the use of the second gate to control excess minority carrier charge in the base. The transistor is essentially an IGBT with active anode shorting capability as shown in Fig. 1.

A bi-directional double-side, double-gate IGBT was fabricated utilizing low temperature (~400°C) hydrophobic direct wafer bonding [3,4]. The primary advantage of the very low temperature bonding process is that device wafers can be fully fabricated (with metallization) and qualified prior to bonding thus requiring only conventional single-side processing. The low temperature (~400°C) annealing approach avoids this problem and has been shown to be effective if anneal times are sufficiently long to provide adequate bond strength for dicing and packaging [5].

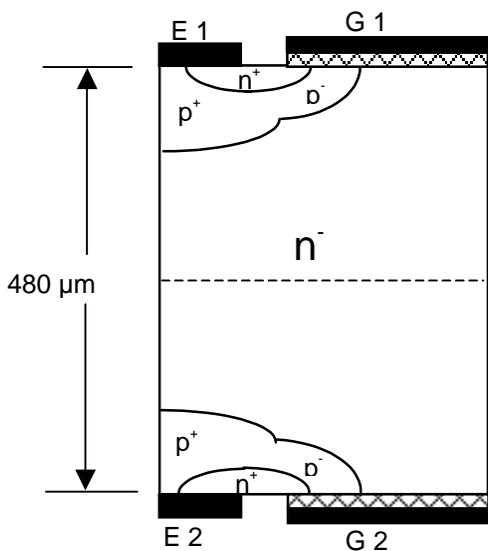


Fig. 1. Cross section of double-side, double-gate IGBT (DIGBT) showing generic labeling of terminals. The broken line indicates the location of the bonding interface.

The transistors were fabricated by joining identical 100 mm IGBT wafers supplied by Dynex Semiconductor. The fully functional IGBTs were nominal 3.3 kV, 50 A parts with an active area of 1 cm² and DMOS gate structures. Slight modifications were made to the IGBT process such as the elimination of back metal and protection of the Al pads and polyimide passivation with 0.5 μm PECVD nitride. The wafers were back thinned to a thickness of ~250 μm and the back sides were rendered smooth by chemical mechanical polishing. The substrates were thoroughly cleaned in an RCA process and the back sides were rendered hydrophobic by dilute HF treatment

delivered through a spin/spray system. No rinse followed the HF step so it was important to limit HF exposure of the front side. The wafers were aligned by mechanical registration of precisely sawn flats in a custom bonding jig. Following initial contact the wafer pair was annealed under light pressure at 150°C followed by a 400°C anneal in N₂ for 5 hours.

With the back gate disabled, the forward voltage drop, $V_{CE(sat)}$, was 1.6 V at 20 A compared to 2.7 V for the reference IGBT. The lower observed DIGBT forward drop is due to greater injection from the forward-biased p⁺-base that acts as the collector (E2), but is also indicative of minimal recombination at the bonding interface. With the back gate enabled the forward drop increased to 3.4 V. The forward and reverse blocking voltages were 1700–1800 V.

Inductive turn-off behavior was studied in a pulse mode configuration (summarized in Table I). Both the DIGBT and reference IGBT were switched at 20 A and 600 V. The switching loss and fall-time were clearly improved by switching G2 prior to switching G1 off. The benefit of the back gate switching was immediately apparent and E_{OFF} dropped to nearly half for no lead time over the case where G2 was disabled (i.e., no back gate bias applied). The benefit of the back gate switching diminished as the lead time increased but at 15 μs the turn-off loss and fall time were similar to the reference transistor at 3.84 mJ and 198 ns, respectively. The turn-off delay time also decreased to near that of the control device for a back gate lead time of 15 μs. Overall, the DIGBT gives a $V_{CD(sat)}$ - E_{OFF} trade-off improvement of 40% over the reference single-side IGBT.

Summarizing, a bi-directional double-side, double-gate IGBT has been characterized. Significant improvements in the trade-off between turn-off dissipation and forward drop are observed with the use of the second gate. Compared to an equivalently rated IGBT, a 40% reduction in $V_{CE(sat)}$ was observed due the geometry of the DIGBT, but the turn-off loss was similar with the aid of the second MOS gate.

Acknowledgements

The authors would like to acknowledge the Office of Naval Research for support of this project under the guidance of George Campisi, Program Manager.

Table I. Measured inductive turn-off parameters.

Measured Parameter	Ref. IGBT	G2 OFF	Gate 2 Lead Time (μs)				
			0	2.5	5	10	15
E_{OFF} (mJ)	3.83	20.3	11.0	8.90	6.95	4.46	3.84
Fall Time (ns)	190	4010	3711	2180	1106	211	198
Delay Time (ns)	324	323	505	505	486	388	323

1. A. Nakagawa, in *PESC '88 Record*, pp. 84–90, 1988.
2. Q. Huang and G.A.J. Amaratunga, *Solid-State Elec.*, vol. 38, pp. 829–838, 1995.
3. K.D. Hobart, F.J. Kub, G. Dolny, M. Zafrani, J.M. Neilson, J. Gladish, C. McLachlan *Proceedings of the 11th International Symposium on Power Semiconductor Devices and ICs*, p. 45–48, 1999.
4. F.J. Kub, K.D. Hobart, and C.A. Desmond, *Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding*, pp. 466–472, 1998.
5. C.A Desmond, K.D. Hobart, F.J. Kub, G. Campisi, and M. Weldon, *Proceedings of the Fourth International Symposium on Semiconductor Wafer Bonding*, pp. 459–465, 1998.