Device Applications Using Bonded thick SOI Wafers

Seiji Fujino, Shigeki Takahashi, Tuyoshi Fukada,
Hiroaki Himi and Kazunori Kawamoto
Electronics Device R&D Center, DENSO CORPORATION
Ashinoya, Kota-cho, Nukata-gun, Aichi Pref., 444-0193
Japan
Phone:81-564-7470 Fax:81-564-7947
E-mail: fujino@ice.denso.co.jp

1. Introduction

For the power ICs used in automotive electronics, it is an important issue to have the susceptibility in operating conditions of high ambient temperature, high humidity etc. and to have serge immunity such as ESD robustness. The automotive applications of power ICs are classified in the following three categories. ① power devices which contained peripheral ICs and power elements, ②single chip ECUs contained micro computer and ③ smart actuator. Among the manufacturing methods of power ICs , it is the best candidate to use the bonded thick SOI wafer by deep trenches. That is because the SOI structure is possible to eliminate the parasitic transistor operation and to be susceptible for negative polarity of input voltage. In addition to the advantages mentioned above, SOI structure has the effective aspect to design circuit easily due to the prevention of parasitic action. In this paper, it refers to the method of improvement of serge immunity of power elements and to the intelligent power ICs fabricated by using the partial SOI wafers. On the other hand, several examples of SOI wafers are reported in the field of MEMS application[1]. This paper also refers to the micro gravity sensor developed in our company.

2. ESD robustness improved LDMOS

As shown in figure 1, the adaptive n^+ layer is added to the drain region of conventional LDMOS[2] structure to relieve the electric field strength and the adaptive p^+ layer is also added to the body region under the source to prevent the parasitic operation. The demanding ESD robustness greater than 15 kV at 1 mm^2 is achieved due to optimization of impurity concentration in the drain adaptive (n^+) and body adaptive (p^+) layer. In the application in which the high ESD robustness is required, the UpDrain DMOS structure is ordinary used with the trade off of on-resistance. However, our proposed LDMOS having improved ESD robustness has low on-resistance of 180 mmΩ mm^2, which is the half of on-resistance of the UpDrain DMOS.

3. The intelligent power IC using the partial SOI wafer[3]

The silicon wafer direct bonding technology[4] combined with the oxide-burying technology by cavity oxidation makes it possible to fabricate the partial SOI wafer. Figure 2 shows the structure of the intelligent power IC developed by using the partial SOI wafer, which is constructed of the multiple channel of low on-resistance VDMOS and the logic part isolated by surrounding of dioxide. In the logic part of this intelligent power IC, it contains 16 bit micro computer.

4. Capacity type micro gravity sensor

Figure 3 shows the gravity sensing element developed by using the bonded thick SOI wafer, which detects the gravity from the electric capacity difference between the mobile electrode and fixed electrode. The mask count is only 4. The feature of this sensing element is the using of dry-etching method to release the mobile electrode, which enables to prevent the sticking problems occurring in the conventional wet-processing.

5. Conclusion

Using bonded thick SOI wafer, the power ICs and sensors which have the demanding performance required for automotive application are developed and manufactured in our company.

References

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3) S. Fujino et al., Jpn. J. Appl. Phys., 34. 864(1995)
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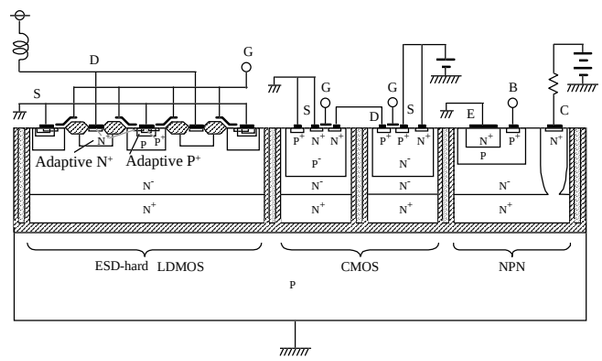

Fig. 1 ESD robustness improved LDMOS of Power IC

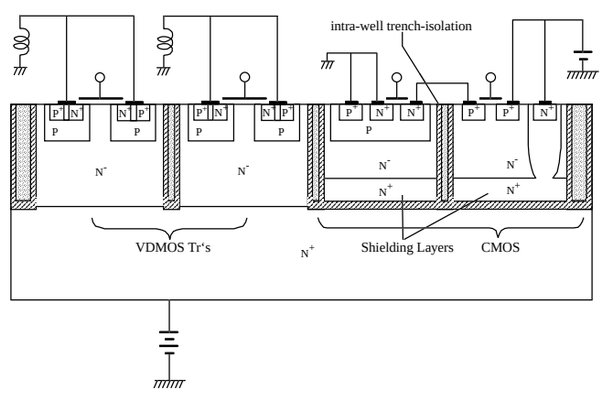

Fig.2 The intelligent power IC using the partial SOI wafer

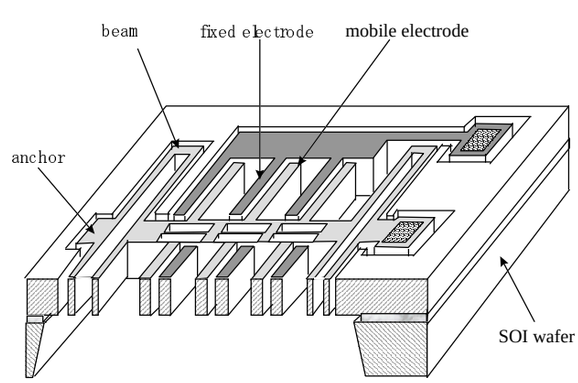

Fig. 3 The capacity type micro gravity sensor