

A Si/SiO<sub>2</sub>/Si heterostructure barrier varactor diode made by wafer bonding

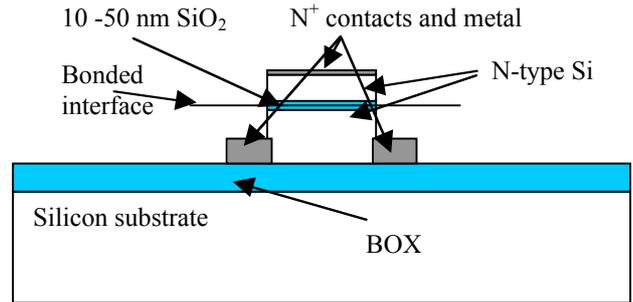
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Wireless communication is pushing mainstream microelectronics into the GHz regime. As a consequence the possibilities and limitations of silicon technology for devices and subsystems operating at 1-100 GHz are of increasing importance. Since the available output power of direct generators generally drops when the frequency increases the use of frequency multipliers may be necessary. Varactors are an important class of frequency multiplying devices and have been used for a long time in III-V technology. The simplest varactor is a reverse biased Schottky junction where its non-linear capacitance generates harmonics. The desired harmonic is chosen by a tuned matching network and by filtering. Since the Schottky junction is not a symmetric device it generates many different harmonics. It would be a large advantage if the varactor device exhibited a symmetric CV curve. Such a device was proposed in 1989 by Kollberg et al [1]. The heterostructure barrier varactor (HBV) consists of a large bandgap barrier material sandwiched between two low bandgap materials. Such a device will exhibit a symmetrical CV curve and it will generate only odd harmonics. Heterostructure barrier varactors have been realized in a number of material systems, GaAs/AlGaAs, InGaAs/AlInAs and InAs/AlSb. In this paper we show how a heterostructure barrier varactor can be realized in silicon technology using wafer bonding. Some initial work has been presented during the last year [2,3].

It is well known that the surface treatment before bonding largely influences the electrical properties of the bonded Si/Si interface [4]. For instance the interface exhibits a symmetrical CV curve due to the depletion regions in the two wafers [4,5]. We propose the use of this device for frequency multiplication. To reach high conversion efficiency and a high cut-off frequency of the varactor a number of requirements need to be fulfilled:

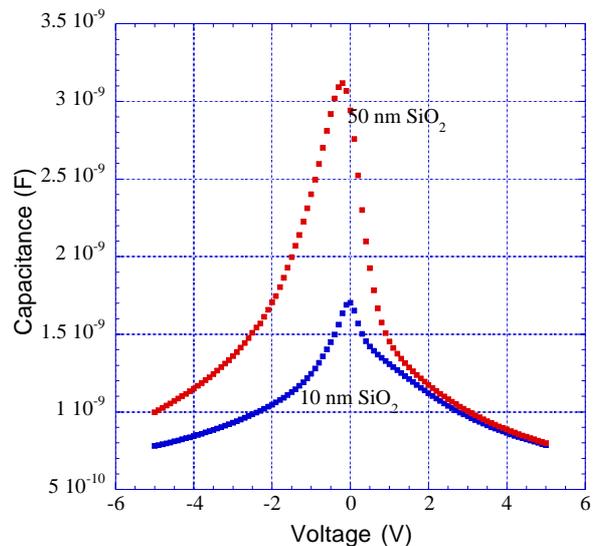
- The barrier should be such that the dc leakage current is minimized.
- The  $C_{\max}/C_{\min}$  within the operational region should be maximized.
- The series resistance should be minimized.
- The thickness and doping of the low bandgap materials surrounding the barrier must be such that the depletion regions can be accommodated during a pump cycle, but neither thicker nor lower doped.

In many aspects the Si/SiO<sub>2</sub> system is perfectly suited for this application. The silicon dioxide gives a very good barrier. The possible problems come from the low saturation velocity in silicon. In figure 1 a schematic view of the varactor structure is shown. In our case the varactor is based on bonding of two SOI wafers which after back-etch of one of the substrates will give two thin silicon films with a bonded interface positioned on the buried insulator of one of the substrates. At the bonded interface a thin film of silicon dioxide will restrict the leakage



**Figure 1.** Schematic view of the varactor structure.

To optimize the barrier initial experiments were made using Si/SiO<sub>2</sub>/Si structures with different silicon dioxide thickness ranging from 10 to 50 nm. The structures were manufactured using wafer bonding of n-type silicon wafers of 10  $\Omega$ cm resistivity. Capacitance vs. voltage curves for devices with 10 nm and 50 nm of silicon dioxide at the bonded interface are shown in figure 2. For 10 nm of silicon dioxide a ratio between  $C_{\max}(0\text{ V})$  and  $C_{\min}(3\text{ V})$  of roughly 1.9 is achieved. For a 50 nm oxide a ratio of 2.4 is achieved. For Si/Si junctions without thermal oxide ratios of more than 10 have been published [5]. As a trade-off between the requirement on  $C_{\max}/C_{\min}$  and the leakage current, 50 nm of oxide seems to be a good choice.



**Figure 2.** Capacitance vs. voltage curves for Si/SiO<sub>2</sub>/Si structures made by wafer bonding. The varactor structures have 10 nm and 50 nm of SiO<sub>2</sub> at the bonded interface.

In this presentation a detailed analysis on the optimization of the varactor will be given together with experimental results from varactor devices currently under manufacturing.

*Acknowledgements:* Thanks are due to Dr. Jumana Boussey at LPCS ENSERG in Grenoble and to the CIME cleanroom facility of ENSERG.

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