High Performance CMOS on SOI

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This paper descibes the recent progress in the development of high performance CMOS on SOI at IBM. Assaderahi 1999, [1] had reviewed the IBM SOI technology from a global perspective ranging from SOI material selection to curcuit styles adapted for designing in partially depleted (PD) SOI. The focus of this paper will be on the development aspects that support the aggressive scaling of CMOS transistors on SOI.