

## Current Status and Future Direction of SOI Technology

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### 1. Introduction

After a long development history, silicon-on-insulator (SOI) technology is becoming a mainstream technology for CMOS LSIs. Meanwhile, the miniaturization in conventional CMOS technology is becoming very severe year by year due to the repeated acceleration of the technology roadmap. It is evident that the pace of high-k material development is incompatible with the required schedule. Moreover, it is unclear whether alternative MOSFET structures can replace the conventional CMOS. In this talk, the current status and future direction of SOI CMOS technology are discussed.

### 2. Current Status and Next Direction of SOI Technology

Current applications driving SOI technology are MPUs [1] and high-performance ASICs. The technology infrastructure of SOI is becoming mature to cover everything from SOI materials to circuit design tools. The key issue in these applications has been how to suppress and control the floating-body in the circuit design. A number of papers analyzing circuit operation and proposing countermeasures have been published [2], providing useful guidelines to circuit designers. Meanwhile, the device process of partially-depleted (PD)-SOI MOSFETs is expected to continue advancing in line with the progress of bulk Si CMOS technology. From now on, reliability issues, which are somewhat different from those of bulk Si technology [3], will become the main issue of process technology in these applications.

What will be the next application of SOI CMOS technology? As long as PD-SOI technology follows the basic design in bulk Si CMOS, it will face the same scaling crisis as bulk Si CMOS. Considering that functions of LSI will become increasingly complex and system-oriented, system-on-a-chip (SoC) applications are also attractive for SOI. Applications to DRAM [4], RF /analog circuits [5] have been found to offer unique advantages, such as soft-error immunity, high-Q inductors, reduced cross-talk noise. Though the floating-body effect or low drain-breakdown-voltage can hinder straightforward incorporation of other devices like flash memory, imagers and so on, mixed incorporation of these devices as system LSI is worthy of pursuit. If direct transfer of bulk Si technology together with the associated intellectual properties (IP) is preferred, SOI substrate having partially bulk Si structure can be a realistic approach, which was demonstrated as embedded DRAMs [6], CCD image sensors [7] and so on.

### 3. Study of CMOS Scaling Limit by SOI Structures

There have been many reports of efforts to extend the scalability of MOSFET by SOI (-like) structures. Though double-gate-structure is recommended for increasing drain current as well as suppressing the short channel effect, it is unclear whether the scenario is realistic in which it replaces the conventional scaling in terms of continuous performance gain as well as economical gain. Comparison of the candidates on the basis of these criteria is important. Moreover, it should be noted that characterization and engineering of nm-thick silicon film will be central to discussion of the scaling limit of MOSFET.

### 4. Summary

Considering that conventional scaling is in a severe situation, we need to prepare another parameter for improving LSI performance. It is expected that flexibility of SOI will provide unique SoC solutions. Meanwhile, study of miniaturization limit of MOSFETs will be continued by various new device structures. Engineering of partially bulk Si substrate or nm-thick film SOI will play an important role in the future study.

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