

Wafer Bonding Using Low-k Dielectrics as Bonding Glue in Three-Dimensional Integration

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Wafer bonding technology using low-k dielectrics as bonding glue is an attractive approach to three-dimensional (3-D) integration; i.e., forming structures with more than one layer of active devices. This 3-D technology may alleviate future Cu/low-k interconnect bottlenecks and offer the potential of overcoming fabrication and performance limitations of future generations of planar ICs [1]. Highly integrated systems may be realized utilizing this 3-D wafer bonding approach, e.g., hard intellectual property (IP) core-based implementations, high-speed synchronous digital systems such as application specific ICs, and heterogeneous systems, such as MEMS, smart sensors, optoelectronics, and wireless technologies [2].

Figure 1 shows a schematic of our 3-D integration concept that uses wafer bonding. Here, three wafers with ICs are bonded together, either face-to-face (second level to first level) or face-to-back (third level to second level). Device surfaces and multilevel interconnects are also depicted in the figure. Dielectric glue layers are used to enhance bonding adhesion. Short, vertical, high aspect ratio vias replace the long distance interconnects in conventional planar ICs.

Wafer bonding is one of the key processes in this technology. Our wafer bonding process using low-k dielectric polymer glue does not involve very high temperatures, very high pressures or electrical biases; therefore, the required processes are compatible with conventional IC fabrication. The desirable properties of the bonding glue include: good adhesion to the substrate or interlevel dielectrics (ILD) to prevent delamination; high thermal and mechanical stability for subsequent processes; thin layer deposition to minimize the aspect ratio of via etch and fill; a high degree of cross-linking in order to form a rigid chemical structure during bonding; easy to process and integratable into CMOS or other IC processes. The candidates under evaluation presently are spin-on polymers such as Flare™, MSSQ and BCB, and vapor deposited polymer such as Parylene-N.

Figure 2 shows an example result after dielectric glue bonding of a Corning-7740 glass wafer to a prime silicon wafer using Flare. After bonding, visual inspection is possible in evaluating alternative glues and process conditions. The bond strength is evaluated qualitatively using a razor blade to attempt to separate the wafers. Our experiments show that the fraction of bonded area and the bond strength depend on the process temperature, the

applied pressure and the pressure vs. time protocol. Particles and defects also influence the bonding results (see voids on Figure 2).

Experimental conditions, analyses of bonding results and bonding mechanisms for low-k dielectric polymer glues will be presented. Electrical results from via-chain test structures will be also discussed.

References:

1. J.-Q. Lu, A. Kumar, Y. Kwon, E.T. Eisenbraun, R.P. Kraft, J.F. McDonald, R.J. Gutmann, T.S. Cale, P. Belemjian, O. Erdogan, J. Castracane, and A. Kaloyeros, Advanced Metallization Conference (AMC 2000), Oct. 2000, to be published by Materials Research Society (MRS), 2001.
2. R.J. Gutmann, J.-Q. Lu, R.P. Kraft, P.M. Belemjian, O. Erdogan, J. Barrett, and J.F. McDonald, in DesignCon 2001: Wireless and Optical Broadband Design Conference, Santa Clara, CA, Jan. 2001.

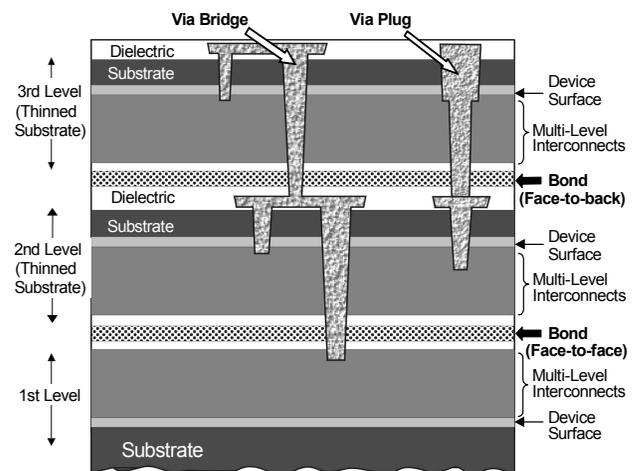


Figure 1. 3D integration concept using wafer-bonding, showing dielectric glue layers as bonding interface, vertical high-aspect-ratio vias, and bonding approaches of "face-to-face" and "face-to-back".

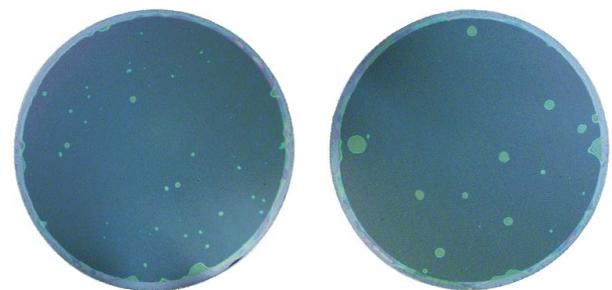


Figure 2. Photos of bonded wafers (200-mm Corning 7740 glass wafer to prime silicon wafer) using Flare. Highly contrast areas show voids.