Title SILICON-DIRECT WAFER BONDING FOR FABRICATION OF RF MICROWAVE DEVICES

Author IQBAL K. BANSAL
Affiliation M/A-COM, A TYCO ELECTRONICS COMPANY
Address 43 South Avenue, Burlington, MA. 01803

Direct wafer bonding is an operation of ultra-fine alignment, joining and thermal bonding of two silicon wafers. The first wafer “handle” substrate is a Czochralski (<CZ>) substrate with N+ arsenic dopant, whereas second wafer “device” is a float-zone (<FZ>) with N- phosphorus dopant. Prior to the join step, surface of the “device” wafer is pretreated using a proprietary process. Each wafer is chemically cleaned in order to minimize sub-micron surface contamination. The surface quality is characterized in terms of light point defects (LPD’s) counts and haze concentration using a laser beam scanning system. The joining step is an automatic operation and is performed under Class 10 or better environment by employing a commercial joiner. The face-to-face joining process first begins at the center of each wafer and then edge-to-edge joining follows. Then thermal bonding or annealing operation is carried out under steam oxidation at elevated temperatures. The effectiveness of the bonding is characterized in terms of degree of surface micro-roughness, hydrophilicity, and flatness as well as orientation of secondary flat. The quality of the interface layer within a silicon-on-silicon (SOS) bonded pair is evaluated in terms of the voided or disbonded region as well as electrical yield. The density of micro-voids within the interface layer is directly dependent upon surface LPD’s counts of the pre-join substrates. A scanning acoustic microscope is employed to determine fractional area occupied by a single largest void as well as entire disbonded regions. A spreading resistivity profile (SRP) system is employed for accurate measurement of doping carrier concentration as a function of the film thickness. The shape of the SRP carrier map is employed as an indicator of the electrical quality of the interface layer. The superior uniformity of a SOS bonded wafer versus an inverse epitaxial silicon wafer substrate is shown in terms of the device performance. Detailed product thruput and yield data are presented in this paper.