

## Bonded Polycrystalline SiC Substrates for the Growth and Fabrication of GaN FETs

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The growth and fabrication of GaN-based microwave FETs has improved dramatically over the past few years with several reports of record power densities at X-band frequencies. The development of inexpensive, large diameter substrates with good thermal and microwave properties has however been nearly non-existent. The large band gap and high sheet charge of GaN heterojunction FETs leads inherently to high voltage and high current density device operation. Coupled with high electron mobility, GaN HFETs are expected to be highly suitable for microwave power applications through the mm-wave region. Sapphire, silicon, and SiC substrates have all been used successfully for the growth and subsequent fabrication of microwave HFETs demonstrating the largely robust nature of heteroepitaxial growth of GaN on widely lattice mismatched substrates. Sapphire and silicon and even GaN provide poor thermal management of high power density devices<sup>1</sup> and presently the best substrate available is semi-insulating 4H SiC which costs approximately \$5000 per 2" wafer. The high cost of such SiC substrates provides the motivation for this work where the goal is to develop a low cost, high performance substrate. The ideal properties of such a substrate are high thermal conductivity, good thermal expansion match to GaN to reduce stress and prevent film cracking, high resistivity for low microwave transmission line loss, large-diameter for scaling, low-cost for wide technology insertion, and good lattice match. This work addresses these requirements through a highly scaleable hybrid substrate approach where, for the first time, thin Si templates bonded to polycrystalline SiC substrates are utilized for the growth of high quality GaN and the fabrication of GaN FETs.

The overall approach is summarized as follows: a thin (111) oriented Si film is transferred by the Smart-Cut technique to a polycrystalline SiC substrate. A similar process was demonstrated previously for the growth of cubic SiC on Si(100)/poly SiC<sup>2</sup>. Once polished the substrate is ready for GaN MBE. The epitaxial GaN was studied by x-ray diffraction, cathodoluminescence, and capacitance-voltage measurements. Finally, GaN MESFETs were fabricated and characterized.

The starting materials for this work were (111) oriented 100 mm Si substrates and 100 mm polycrystalline 3C-SiC substrates. The poly SiC substrates were rendered smooth by an optical polishing process. The Si substrate was implanted with  $4.5 \times 10^{16}$  180 keV H<sub>2</sub><sup>+</sup> ions. Both substrates were cleaned with an SC-1 solution and bonded. The wafer pair was annealed at 250 °C for 4 hours then the temperature was ramped to 500 °C for 10

min to split or cleave the Si substrate at the approximate range of the proton implant. The approximately 800 nm Si(111) film was polished by CMP to a thickness of about 250 nm. AFM showed that the Si surface had a roughness of ~0.2 nm. The 100 mm substrates were cut into 35x35 mm<sup>2</sup> squares (50 mm diagonal) for subsequent MBE growth. AlN (40 nm) and GaN (500 nm) buffer layers were grown by gas source MBE (GSMBE) at a temperature near 830°C. RHEED showed coherent growth throughout. Device layers were grown subsequently in a separate MBE system with solid source Ga and a plasma N source at a growth temperature near 750°C, where approximately 1 μm of undoped GaN was grown followed by 150 nm of Si-doped GaN ( $\sim 5 \times 10^{17}$  cm<sup>-3</sup>). Ni gate MESFET transistors were fabricated with a process similar to that described previously<sup>3</sup>. The devices were isolated from one another by ion implantation of N.

Visual observation of the films at all stages of growth revealed that no cracking of the film occurred up to the total GaN film thickness of ~1.7 μm. Double-crystal XRD characterizations of the thin Si and GaN films were performed at each step. The FWHM of the GSMBE GaN (0002) peak was 1380 arc-sec which improved to about 1000 arc-sec following the second MBE growth. Interestingly, the FWHM of the Si(111) peak was around 100 arc-sec prior to any growth. The broad width was unexpected and is presently under investigation. Additional broadening of the Si(111) peak was observed after a separate growth of just the AlN buffer where the FWHM was ~200 arc-sec. No additional broadening was observed following growth of the two GaN films. It appears that some strain is transferred from the AlN/GaN film to the thin Si layer and this redistribution of strain is presently under investigation.

Initial examination of the MESFETs showed very low transconductance due to large parasitic conduction through the GSMBE AlN/GaN buffer layer. The parasitic conduction was verified by CV measurements. The buffer layers were then rendered insulating by consecutive 100 and 175 keV proton implants which nearly annihilated the parasitic conduction path. The resulting peak transconductance was around 12 mS/mm. The expected absence of self-heating effects could not be verified due to increasing drain leakage at large drain-source biases. Efforts are underway to produce FETs with ideal IV characteristics so as to further characterize the thermal management capabilities of the poly SiC substrates.

Summarizing, a highly scaleable hybrid substrate has been fabricated by direct wafer bonding. Thin Si(111) template layers bonded to robust polycrystalline SiC substrates provide a platform for high power GaN transistors. Growth and fabrication of GaN FETs on such substrates has been demonstrated for the first time.

### References:

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