Advanced Pre-gate Cleans for High Quality Ultra-thin Oxides and Nitrided Gate Stacks

Evanson G. Baiya[1], John Rosato[1], Debra Acock[2], and John Smythe[2]

1. SCP Global Technologies
   400 Benjamin Lane,
   Boise, ID 83704
2. ZiLOG Inc
   1401 N. Kings Rd,
   Nampa, ID 83687

Abstract

The rapid scaling of CMOS device dimensions has lead to an increased sensitivity of device properties on gate dielectric properties. As a result, it has become necessary to revisit wafer surface preparation prior to gate oxidation.[1] Dilute cleans have shown promise as a replacement for the traditional RCA cleans.[2]

In this paper we report on the effect of pre-gate cleaning techniques on the Gate-oxide Integrity (GOI) of ultra-thin oxide and nitrided oxides. An extensive investigation of the effect of pre-gate wet immersion cleans on the GOI of 40-65Å ultra thin oxides and nitrided oxides was conducted. The cleaning efficacy was evaluated by characterizing particle and metal contamination levels, surface roughness, electrical breakdown characteristics, charge to breakdown, and equivalent oxide thickness. Results showed that an ultra-dilute RCA clean performed in an advanced process system that incorporated a combined process/rinse/dry chamber produced the highest quality oxides. Dilute HF-last and ozone passivation cleans were also shown to produce excellent dielectric characteristics. In addition, the effect of the HF concentration used for sacrificial oxide (SACOX) etching on GOI is also reported.[3, 4]
The newly developed dilute RCA pre-gate cleans demonstrated improved overall process performance. Both the surface morphological properties and the electrical (Q_{BD},[5] E_{BD}, and SILC[6]) characterization showed better performances than the conventional concentrated RCA pre-gate cleans. The dilute RCA cleans resulted almost a 10X reduction in particle defect densities, and more than a 30% reduction in surface roughness. The electrical characteristics showed a breakdown field strength of >16MV/cm, and a 50% improvement in SILC, while the Q_{BD} was improved by 10% as compared to a standard RCA clean. The data also showed that the HF last cleans produced similar, but slightly inferior results. Finally, it was shown that the nitrided gate stacks showed less sensitivity to the surface preparation technique compared to ultra-thin oxides.[7]

References

1. E. Bellandi, et al, *Electrochem. Soc. Proc. Vol. 99-36*, 25 (1999)
2. T. Nocolas, et al, *Electrochem. Soc. Proc. Vol. 99-36*, 165 (1999)
3. E. Baiya, et al, *SCP Int. Symp. Proc. Vol. 8 (May 2001)*
4. I Kanshkoush, et al, *Electrochem. Soc. Proc. Vol. 95-20*, 429 (1995)
5. E. Wu, et al, IEEE Trans. On Elect. Dev., Vol. 47, 12, (2000)
6. J. D'Amico, *ASTM Conf. On gate dielectric oxide integrity*, (Jan 1999)
7. E. Wu, et al, *IEEE Trans. On Elect. Dev., Vol. 47, 7*, (2000)

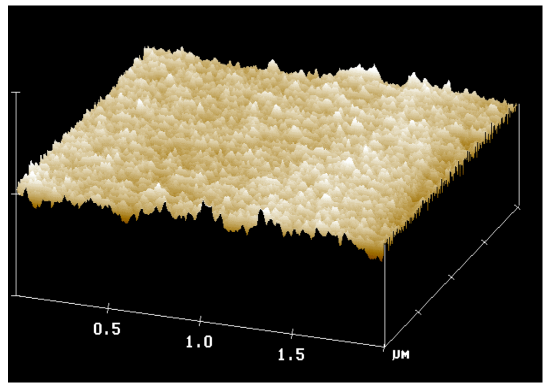

Figure 1: AFM (2X2mm) sample size on a wafer after a dilute SC1 process (100:2:1), RMS = 0.108nm. and Ra = 0.087nm..

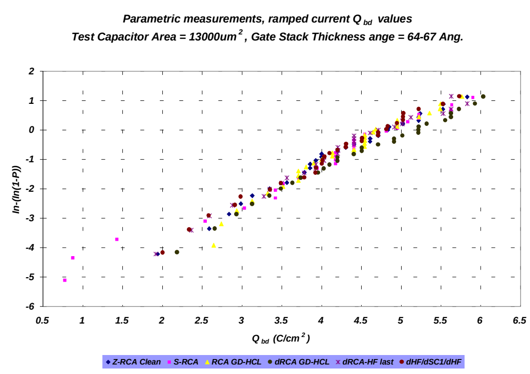

Figure 2: Nitrided gate stacks Q_{BD} values after different pre-gate cleans. The dilute RCA clean shows the best Q_{BD} values.

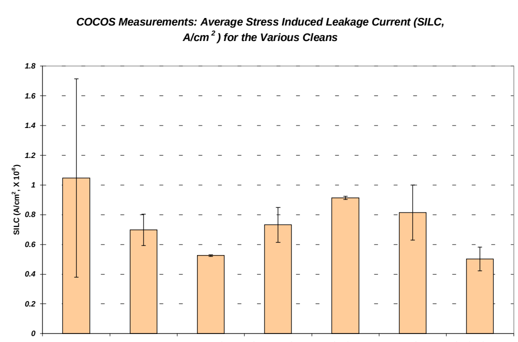

Figure 3: Stress Induced Leakage Current (SILC) measured for the different nitrided gate stacks. Clearly the dilute pre-gate cleans showed better charge trapping than the concentrated ones.