

## Gas-Phase Surface Conditioning in a High-k Gate Stack Cluster

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Due to the critical role an interfacial oxide plays in a high-k dielectric/Si gate stack structure the control of the Si surface condition prior to gate dielectric deposition is of fundamental importance. On one hand with the low dielectric constant of SiO<sub>x</sub> any interfacial oxide will lead to the reduction of the equivalent dielectric constant of the gate stack defeating the purpose of introducing the alternative dielectric. On the other hand, however, a thin interfacial oxide may be needed to reduce the interface trap density and improve electron mobility in the channel of the MOSFET. It has been postulated that an interfacial oxide at least 0.5 nm thick is needed to meet these requirements. In addition, it is highly desirable that such an interfacial oxide be nitrated to increase its dielectric constant and also to minimize possible boron penetration of the oxide from p-type poly-Si gate contacts.

In this experiment conditioning of the Si surface in the gas-phase prior to high-k gate dielectric deposition integrated in a cluster is investigated. The emphasis is on low temperature formation of an interfacial oxide that would meet the requirements outlined above.

The experiments are performed using a cluster tool consisting of a gas-phase surface conditioning module, a Liquid Source Misted Chemical Deposition (LSMCD) module and a low-temperature RTP module (Fig. 1). The surface conditioning module is equipped with UV/O<sub>2</sub>, anhydrous HF/methanol, UV/Cl<sub>2</sub> capabilities. This sequence was demonstrated to leave Si surfaces free from any chemical residues. The last step in the pre-deposition sequence is an UV/NO treatment which forms an ultra-thin layer of nitrated oxide on the surface. The LSMCD method uses liquid metal organic precursors and deposits a controlled amount of liquid onto the surface in the form of a fine mist. Wafers are then annealed in the RTP module (Fig.1) using sequences not exceeding 700 °C. The high-k dielectrics of interest in this study are SrTa<sub>2</sub>O<sub>6</sub> and HfO<sub>2</sub>. Surface characterization is carried out using XPS while thicknesses of the oxides involved are determined by means of both ellipsometry and cross-sectional TEM. In addition, Pt or Pt/Ti-gate MOS capacitors are formed on processed wafers. C-V and J<sub>g</sub>-V characterization is carried out to determine key electrical characteristics of the gate stacks investigated.

As shown in Fig. 2 UV/NO exposure without any wafer heating results in the formation of

an oxide about 1 nm thick. By reducing the irradiation time to 20 seconds an oxide about 0.5 nm thick can be obtained under these conditions. Because of the integration of the surface-prep and deposition process this oxide will not grow thicker during wafer transfer to the deposition chamber. XPS characterization has demonstrated that nitrogen is incorporated into this oxide. The presence of this oxide on the surface during the subsequent high-k dielectric deposition and anneal has an effect on the final thickness of the interfacial oxide in the gate stack. Furthermore, the leakage current across the gate stack was reduced by an order of magnitude when the UV/NO step was incorporated into the process.

Using the methodology employed in this experiment MOS structures displaying equivalent oxide thicknesses of 1.0 nm were obtained using SrTa<sub>2</sub>O<sub>6</sub>. The impact of the surface pre-treatment sequence on the characteristics of MOS devices is discussed in detail in the full account of this work.

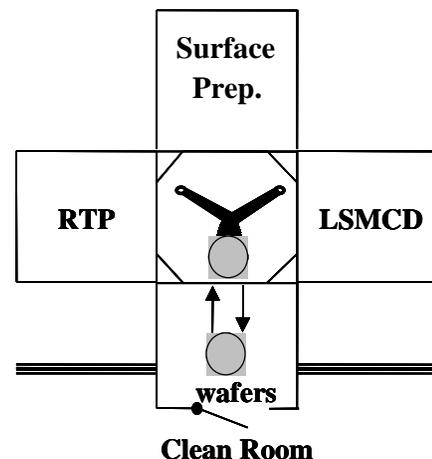


Fig. 1 Schematic of cluster tool.

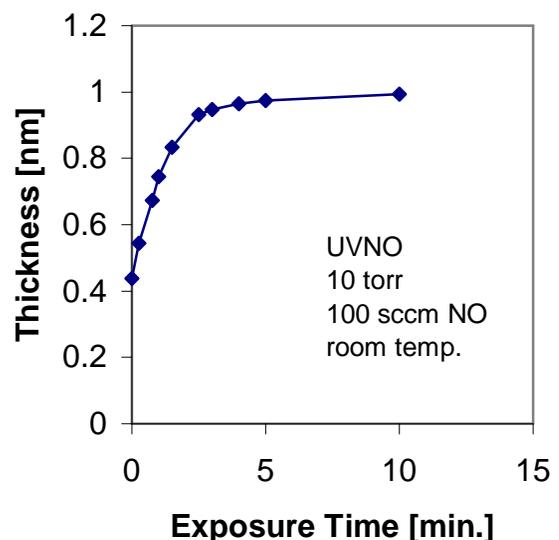


Fig. 2 Kinetics of UV/NO oxidation.