

Vacuum Clustered Dry Cleaning for Pre-Gate Surface Preparation

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INTRODUCTION

As gate dielectric manufacturing progresses towards very thin silicon oxide films or high-k gate dielectrics, it becomes very important to control the silicon surface prior to the gate dielectric step. The surface needs to be clean and free from contamination as well as smooth in order to get the performance needed for 0.1 μ m technology transistors and beyond. We have developed an all dry gas phase pre-gate cleaning process that removes light organic contamination, silicon oxide and metal contamination with minimal roughening of the silicon surface. The process is performed in a cross flow vacuum chamber in which the wafer is stationary and both sides are cleaned simultaneously (Figure 1). The ultraviolet lamps used above and below the chamber initiate the photochemistry inside the chamber as well as provide non-contact wafer heating.

THE DRY CLEANING PROCESS

The starting silicon surface typically has a native oxide or a chemical oxide from a previous wet cleaning process. The pre-gate cleaning process we developed is comprised of three basic steps. There is a pre-treatment step, an oxide removal step and a metal contamination removal step.

The pre-treatment step removes light organic contamination using UV/Cl₂. The UV step is required in order to heat the wafer and the Cl₂ flow during the UV step gives the added benefit of organic contamination removal which results in a more uniform oxide etch process (Figure 2).

The surface oxide is removed with anhydrous HF and an IPA/H₂O catalyst. The oxide removal step is able to achieve $\pm 4\text{\AA}$ uniformity (8 \AA range) for a 30 \AA etch without wafer rotation or a showerhead gas distribution. We have also found the etching rate to be constant after a short "induction" period (Figure 3). The resulting surface is essentially bare silicon with no remaining oxide or etch residue.

After the surface oxide has been removed, another UV/Cl₂ step is performed to complete the removal of any remaining metals. We have developed a 50 second high power UV/Cl₂ processes that can remove 1×10^{11} atoms/cm² Fe contamination to below TXRF detection limits. However, it has been shown that this type of aggressive UV/Cl₂ processes will roughen the exposed silicon surface. We have also developed a 45second low power UV/Cl₂ process that results in $<0.3\text{\AA}$ RMS added roughness (Figure 4) and are currently evaluating its low-level metals removal performance.

In addition, an optional additional UV/O₂ step has been developed to regrow a passivating oxide layer depending on the exact needs of the integrated process. The UV/O₂ step re-grows about 6 \AA of oxide on the cleaned silicon surface.

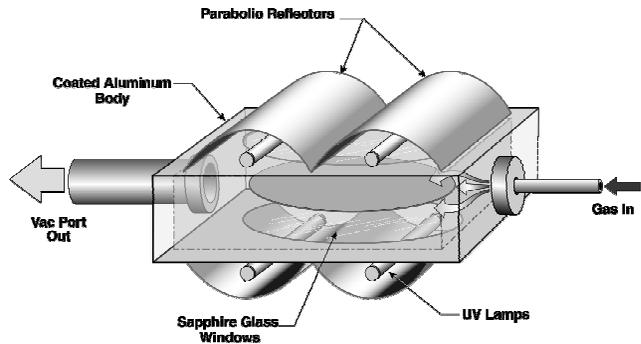


Figure 1. Cross flow vacuum chamber showing the gas inlet port, vacuum outlet port, wafer orientation and ultraviolet lamps.

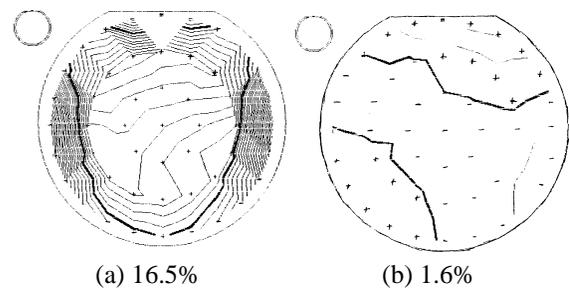


Figure 2. Oxide etch uniformity maps showing the affect of (a) UV only pre-treatment and (b) UV/Cl₂ pre-treatment.

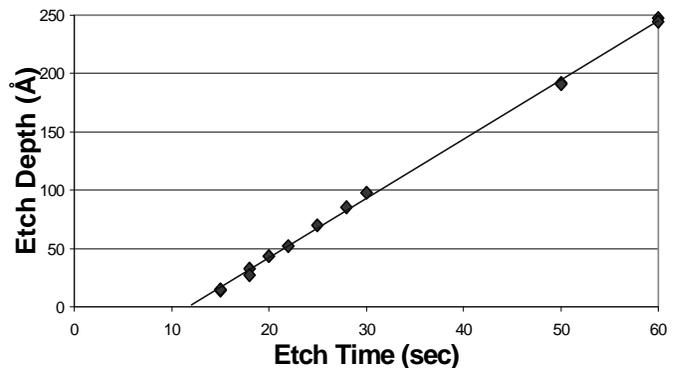


Figure 3. Oxide etch depth as a function of time after initiating the flow of anhydrous HF.

Conditions	Pre	Post
pretreat/etch/reox	0.77 \AA	0.66 \AA
pretreat/etch/ UVC12-hi pwr-30s/reox	0.75 \AA	2.28 \AA
pretreat/etch/ UVC12-hi pwr-10s/reox	0.63 \AA	1.76 \AA
pretreat/etch/ UVC12-hi pwr-4s /reox		1.59 \AA
pretreat/etch/ UVC12-hi pwr-1s /reox	0.70 \AA	0.92 \AA
pretreat/etch/ UVC12-lo pwr-1s /reox	0.75 \AA	0.72 \AA
pretreat/etch/ UVC12-lo pwr-45s/reox	0.67 \AA	0.68 \AA
pretreat/etch/ UVC12-lo pwr-90s/reox	0.81 \AA	3.75 \AA

Figure 4. Silicon surface roughening with various UV/Cl₂ processes.