

Impact of Organic Contamination on Device Performance

Deborah Riley^{1,2}, Jay Guan², Glenn Gale³, Gennadi Bersuker¹, Joe Bennett¹, Pat Lysaght¹, Billy Nguyen¹
¹International SEMATECH, Austin, TX
²Advanced Micro Devices, Austin, TX
³Tokyo Electron LTD, Austin, TX

OBJECTIVE:

Organic contamination of wafer surfaces remains a concern in the microelectronics industry due to the ability of organics to degrade gate oxide integrity. For 180 nm processing, the 1999 ITRS Roadmap indicates that organic contamination after critical cleans should be below $7.3E13$ carbon atoms/cm²; this value drops to $5.3E13$ for 130 nm technologies. These roadmap values are based solely upon an intuitive assumption that 10% carbon coverage on a bare silicon wafer will be tolerable during device fabrication. [1] In the study described here, the validity of these roadmap values is investigated.

APPROACH:

This evaluation of organic contamination impact was carried out using unpatterned test wafers and transistor wafers at International SEMATECH.

Carbon was introduced to wafers by ion implantation through a 15.0 nm sacrificial oxide layer. Four different doses of carbon were evaluated (0, $1E13$, $1E14$, and $5E14$ atoms/cm²) in this study. After the sacrificial oxide was stripped, an oxynitride gate dielectric was grown. On unpatterned wafers used for SIMS profiling, the dielectric was 4.5 nm thick. Transistor wafers used to evaluate device performance had gate dielectrics that were either 2.5 nm or 4.5 nm thick.

To quantify the amount and profile of carbon in the final gate oxide, a SIMS profiling technique was utilized [2]. To evaluate the impact of the carbon on devices, electrical and reliability performance of NMOS transistor structures were tested.

RESULTS:

Using a SIMS profiling technique, the amount of carbon in the gate dielectric was measured for each implantation dose. Table 1 summarizes the collected data; note that precision of the technique improves at higher doses due to a diminishing impact from the background signal. It is also anticipated that some carbon was retained by the sacrificial oxide and lost when that oxide was stripped. The detection limit of the technique is estimated at $1E12$ carbon atoms/cm².

C-V curves for the transistor wafers illustrate some of the device trends observed. Figure 1 is a C-V curve for 10^{-4} cm² capacitors with 2.5 nm dielectric films. The shift in the curve and the change of curve shape at a dosage of $5E14$ atoms/cm² suggests a build up of positive charge in the oxide and the generation of interface traps. A significant V_t shift at doses beyond $1E14$ also suggests charge build-up with high carbon dosage. Transconductance is sensitive to interface states, and a reduced G_m was measured for 2.5 nm devices receiving a high dose implant. Evidence of charge build-up and interface state generation was much stronger for 2.5 nm dielectrics than for 4.5 nm dielectrics in this study, although differences in oxide growth conditions may influence this observation.

Results also indicate that carbon introduction impacts electrical oxide thickness. Suppression of oxide growth is

clearly indicated at higher carbon dosages. Figure 2 illustrates the equivalent oxide thickness measured on devices in this study.

Finally, reliability degradation was found when carbon dosages were high. Charge to breakdown and time to dielectric breakdown both suggest an impact from carbon contamination, with the 4.5 nm devices appearing more sensitive than the thinner devices.

CONCLUSIONS:

This evaluation indicates that carbon contamination can significantly degrade gate oxide quality and reliability. While the primary effect from small doses is suppression of oxide growth, higher doses of carbon show the generation of interface states and positively charged centers in bulk oxide. The quality of thinner oxides appears to be more sensitive to carbon than the quality of thick oxides. Thicker dielectrics, however, appear more susceptible to reliability degradation from carbon. Overall this study suggests that high carbon content is detrimental, but that doses close to $1E13$ have minimal impact. This data indicates that organic contamination values in the 1999 ITRS roadmap are reasonable.

REFERENCES:

- [1] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association (1999)
[2] Guan, J., G. Gale, J. Bennett, *Jpn. J. Appl. Phys.* Vol. 39 (2000) pp. 3947-3954, Part 1, No 7A, July 2000

Table 1: Implant Dose vs SIMS calculated Dose

| Wafers | Implant Dose | Average Measured SIMS Dose | std dev |
|---------------|--------------|----------------------------|------------|
| -01, -02, -03 | 0 | 0 | - |
| -04, -05, -06 | $1.00E+13$ | $3.96E+12$ | $3.68E+11$ |
| -07, -08, -09 | $5.00E+14$ | $3.04E+14$ | $7.73E+12$ |
| -10, -11, -12 | $1.00E+14$ | $4.35E+13$ | $2.63E+12$ |

Figure 1: Capacitance-Voltage for 25 A devices

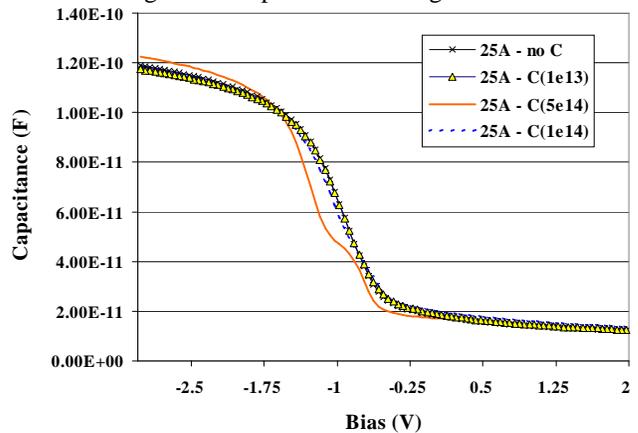


Figure 2: EOT for Transistors

