

Development of Cryogenic Ge JFETs - IV

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We have continued investigation and development of cryogenic Ge JFETs as described at previous meetings [1-3]. The objective of this work is to produce a JFET that will operate down to the lowest cryogenic temperatures (down to liquid-helium temperatures), with very low noise and stable dc characteristics for use in preamplifiers for sensitive cryogenic detectors. Our intent is to develop Ge JFETs to fill the gap that has so far not been filled by available Si JFETs, Si MOSFETs, GaAs MESFETs, or GaAs JFETs.

The Ge JFETs are fabricated as described previously [1-3], with fabrication parameters (epitaxial layer thickness and doping concentration) chosen to provide the desired pinch-off voltage and other characteristics at cryogenic temperatures. We will report results for Ge JFETs made with recently designed photomasks having a wide range of geometries to accommodate the input capacitance and noise requirements of various applications as well as providing improved cryogenic characteristics.

As reported previously, we have obtained good dc characteristics down to liquid-helium temperature for both n- and p-channel Ge JFETs. Measurements of gate reverse-leakage current indicate levels well below our usual measurement limit of approximately $1e-13$ A. We have measured noise over the frequency range 1 Hz to 100 kHz, at temperatures between 4 K and 300 K, and at power dissipations between 10 μ W and 2 mW. Between approximately 30 K and 80 K we have obtained excellent low-frequency noise levels in n-channel Ge JFETs, with gate-referred noise voltages of approximately 30-60 nV/rtHz at 1 Hz and decreasing to below 2 nV/rtHz above approximately 1 kHz for a 40 μ m by 1560 μ m gate Ge JFET with $V_{ds} = 1.2$ V and $I_d = 0.3$ mA. For lower and higher power dissipation the "1/f" noise remains approximately the same, but the white noise increases or decreases. We will report on progress on reducing noise below 30 K down to 4 K in both n- and p-channel Ge JFETs.

[1] R. R. Ward et al., "Development of Cryogenic Ge JFETs," Third European Workshop on Low Temperature Electronics (WOLTE 3); *J. de Physique IV*, Vol. 8, Pr. 3, June 1998, pp. 123-126.

[2] R. R. Ward et al., "Development of Cryogenic Ge JFETs - II," presented at the Electrochemical Society Fifth International Symposium on Low Temperature Electronics, 21 October 1999 in Honolulu, Hawaii, U.S.A.

[3] R. R. Ward et al., "Development of Cryogenic Ge JFETs - III," Fourth European Workshop on Low Temperature Electronics (WOLTE 4), Noordwijk, The Netherlands, 21-23 June 2000, ESA publication WPP-171, pp. 105-111.

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