

Compound Semiconductor Devices for Space-Borne Power Electronic Systems

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A promising material for cryogenic electronic applications is indium gallium arsenide lattice-matched to indium phosphide. $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ possesses a higher peak electron velocity and low field mobility than both silicon and gallium arsenide. It exhibits a low density of interface states when in contact with a deposited insulator. This allows the fabrication of reliable metal-insulator-semiconductor devices. Most importantly, the ionization energy of dopant impurities in $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ is among the lowest of all III-V semiconductors. Less thermal energy is required to excite carriers out of their dopant sites, allowing MIS devices fabricated on $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ to adequately operate at much lower temperatures than similar devices on silicon.

A complete analytical model of an n-channel enhancement-mode $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ power MISFET was investigated in order to study the feasibility of $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ compound semiconductor technology for cryogenic power electronics applications (1). The model was then used to predict the MISFET operating parameters from 300 K to 10 K through Monte-Carlo simulation. Current-voltage characteristics, threshold voltage shift, and on-resistance were determined and compared against a Si MOSFET of the same design. It was determined that the $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ MISFET exhibited a lack of carrier freeze out down to 15 K compared to 50 K for the Si device. In addition, it was found that the use of an undoped or semi-insulating $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ epitaxial layer in the fabrication of the MISFET would greatly reduce the threshold voltage shift from room-temperature to cryogenic temperatures.

The $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ MISFET model was then used in the design of a Buck dc-dc converter with an operational temperature range of 300 K to 20K. The converter was designed to deliver a constant DC output voltage of 5 V at a power of 10W. The input voltage was varied from 5 V to 15 V. The simulation results showed a smaller output voltage variation and a higher efficiency over the entire temperature range than a comparable Si-based converter.

Depletion-mode $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ MISFET's with 1.35 mm total gate widths were then fabricated by a 5-mask, UV photolithography process (2). The $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ layer was grown lattice-matched to a SI InP substrate in a DCA MBE 450 system using pure indium, arsenic, and phosphorus for elemental sources. The layer was doped *in situ* $N_D=10^{17} \text{ cm}^{-3}$ using elemental silicon as the dopant source. A 0.1 μm undoped InP buffer layer was grown

between the InP substrate and $\text{In}_{0.47}\text{Ga}_{0.53}\text{As}$ epitaxial layer.

Devices were first isolated by mesa-etching in a 1:1:38 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution. Ohmic contacts were formed by electron beam evaporation of 12 wt.% Au/Ge followed by Au; both to a thickness of 1500 Å. A 1 min rapid thermal anneal was performed at 450 °C in forming gas (10% H_2/N_2) to alloy the contacts. Gate recess etching was performed in a 1:1:100 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution. Etching of the gate area continued until the desired channel saturation current was achieved ($\approx 250\text{-}300 \text{ mA/mm}$).

After the gate recess etch, the gate insulator was deposited to a thickness of about 900 Å. SiO_2 was deposited by a low temperature PECVD process. An ultrathin silicon interfacial layer was deposited before the SiO_2 . The interfacial layer has previously been shown to lower the density of interface states in PECVD deposited SiO_2 on InP and InGaAs (3). The sample was annealed in pure H_2 for 30 min to improve the electrical characteristics of the insulator. The gate metal was comprised of 250/5000 Å Ti/Au and was next deposited by e-beam evaporation. The gate metal was used as the mask for the selective etching of the gate oxide by RIE. The final step was the evaporation of an additional 5000 Å Au on the source and drain pads to aid in wire-bonding and heat dissipation.

The MISFET exhibited excellent DC performance over the entire temperature range. A drain-to-source DC signal was regulated by a 1 kHz square wave applied to the gate terminal of the device. The voltage waveform generated across an external 20 Ω resistive load was recorded at specific temperatures as the cold head was cooled from 300 K and showed little deviation down to 25 K. Specifically, the waveform was absent of carrier freeze-out induced phenomenon known to plague silicon MOSFETs at such temperatures. Transient behavior in the drain current was not observed at the operating frequency of 1 kHz.

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REFERENCES

- (1) D. Bernardon, 'Theoretical Investigation of Semiconductor-Buck Converter for Low Temperature Applications', M.S. Thesis, University of Toledo (1998)
- (2) C.H. Melkonian, 'Indium Gallium Arsenide/Indium Phosphide MISFETs for Cryogenic DC Switching Applications', M.S. Thesis, University of Toledo (1999)
- (3) M. Shokrani and V.J. Kapoor, 'Silicon Dioxide with Silicon Interfacial Layer for Gate Dielectric in MISFETs on Indium Phosphide', Proc. of ECS, vol. PV 90-9, p. 379, Pennington, NJ (1990)