

Prospects for the Operation of Deep Sub-0.1 μm MOSFETs at Low Temperature

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The low temperature operation of deep submicron MOSFETs, down to 20nm gate length, is reviewed. A particular attention is given to the performance (ON- and OFF-state currents, subthreshold swing, transconductance) and physical mechanisms (short channel and hot carrier effects, transport parameters) of these ultimate silicon devices. Various transistor architectures (with and without halo, n and p-channels, bulk Si and SOI, surface and buried channels, gate oxide down to 1.2 nm) are comparatively evaluated as a function of temperature. The reliability of these deep sub-0.1 μm MOSFETs is also addressed in a wide temperature range.