

# The Impact of the Drain Saturation Voltage on the Multiplication Current Modeling of MOSFETs at Liquid Helium Temperatures

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**Introduction.** The drain saturation voltage  $V_{DSAT}$  is key in the modeling of CMOS transistors and circuits, as it separates the ohmic from the saturation regime. It is also an important parameter for the understanding of hot-carrier and floating body (kink) effects. Several models have been proposed, amongst which:

$$\frac{1}{V_{DSAT}} = \frac{1}{V_{GS} - V_T} + \frac{1}{E_c L_{eff}} \quad (1)$$

provides a good approximation [1]. Hereby is  $V_{GS}$  the gate voltage,  $V_T$  the threshold voltage,  $E_c$  the critical field for velocity saturation on the order of a few  $10^4$  V/cm and  $L_{eff}$  the effective device length. In spite of its simplicity, it is not so easy to calculate  $V_{DSAT}$  from Eq. (1), mainly due to the uncertainty on  $E_c$ . One therefore relies on either numerical simulations or semi-empirical methods to derive this parameter from drain current ( $I_D$ )-drain voltage ( $V_{DS}$ ) measurements. The aim of this paper is to compare different methods of  $V_{DSAT}$  extraction for MOSFETs operated at liquid helium temperatures (LHT). It is shown that the  $R_{out}$  based technique [2] yields the most reliable data. Finally, the impact of the  $V_{DSAT}$  extraction on the multiplication current modeling will be discussed.

**Experimental.** Measurements at LHT have been performed on mounted transistors that have been fabricated in a  $0.7 \mu\text{m}$  CMOS technology. Full details about the different splits can be found elsewhere [3]. The nominal device dimensions  $L \times W$  are  $5 \mu\text{m} \times 10 \mu\text{m}$ ; both n- and p-channel devices have been used in the study.

**Results and Discussion.** One of the most popular techniques to extract  $V_{DSAT}$  is based on the multiplication factor  $M = |I_B/I_D|$  [4], which gives the ratio of the substrate current  $I_B$  and the drain current  $I_D$ . It has also been shown useful at cryogenic temperatures [5]. The method of constant  $M$  (abbreviated by  $M$ ) has also been applied here, as far as the substrate current was measurable. This explains why the  $M$  method is better suitable for n- compared with p-channel

devices. An alternative method ( $K$  method) is based on the observation that there exists a close connection between the drain current kink at 4.2 K and the multiplication factor. As will be shown, the onset of the kink corresponds approximately with a small constant  $M$  in the order of  $10^{-9}$ , which is much lower than the measured values. Nevertheless, it is clear that the  $K$  technique is similar as the constant  $M$  method and has the advantage that it can be applied without the need for measuring  $I_B$ . In order to better define the kink start  $V_{DSK}$  at every  $V_{GS}$  the output conductance is plotted versus the drain voltage  $V_{DS}$  [3]. The locus  $V_{DS} = V_{DSAT}$ , which goes through the origin is then determined by shifting the experimental

$V_{DSK}$ - $I_{DSK}$  curve by a fixed amount, as explained elsewhere [3]. A final method is based on the output resistance [2], whereby the linear part is extrapolated to the  $V_{DS}$  axis, yielding directly  $V_{DSAT}$ . The results of the different  $V_{DSAT}$  extractions will be compared, from which significant differences can be derived. As will be demonstrated, the most reliable data have been obtained from the  $R_{out}$  technique. Finally, the impact of the  $V_{DSAT}$  value on the multiplication current modeling will be investigated. It will be shown that the universal relationship is only approximately found at 4.2 K. In other words, there is marked variation of the multiplication parameters with the gate voltage. The origin of this variation will be discussed and further improvements of the method are pointed out.

## References

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