

Performance and Reliability of Advanced pMOSFET Devices

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This work is focused on advanced surface and buried channel pMOSFETs characterization as a function of temperature in terms of transport parameters, short channel effects and hot carrier degradation [1-7].

The studied pMOSFET devices were processed with a 0.12µm CMOS silicon technology at LETI (Grenoble, France), with various gate lengths ($L=0.05$ to $1\ \mu\text{m}$), gate width $W=10\ \mu\text{m}$ and gate oxide thickness of 2.3nm.

The threshold voltage for various gate lengths of both buried and surface channel pMOSFETs in different temperature ranges is shown in Fig.1. A threshold voltage decrease is observed with the gate length reduction due to charge sharing effect. This effect is more accentuated in surface channel devices than in buried ones, whatever the temperature is. This suggests a better SCE control in our buried channel devices. On the other hand, the threshold voltage of surface channel devices is lower than that obtained for buried ones.

The difference between mask and effective gate length ($dL=L_{\text{mask}}-L_{\text{eff}}$) at different temperatures is shown in Fig. 2. This difference is about $0.01\ \mu\text{m}$ for surface channel devices and about $-0.04\ \mu\text{m}$ for buried channel devices at room temperature. This difference increases for buried channel devices (in absolute values) with reducing the temperature.

The temperature dependence of carrier mobility is illustrated in Fig. 3. We can notice that the carrier mobility is higher in the buried channel devices than in surface channel ones. This difference increases at low temperature.

In the subthreshold mode, the drain-induced barrier lowering (DIBL) causes enhanced source injection resulting in increased leakage current. The DIBL effect is studied by the threshold voltage reduction with increasing the drain voltage. This effect is reduced in surface channel devices as compared to the case of buried channel ones (Fig.4) at room temperature.

The hot carrier stress measurements were performed (for $L=0.1\ \mu\text{m}$ and $L=0.075\ \mu\text{m}$) in order to extrapolate the device lifetime and also the drain bias that can be applied in order to obtain one-year lifetime under static stress. This is supposed to be equivalent with ten years lifetime under circuit operation. Fig. 5 shows typical examples of transconductance degradation for different applied drain biases for $0.1\ \mu\text{m}$ gate length. Increasing stress drain voltage enhances the transconductance degradation. This effect relies upon the dependence of the longitudinal electric field and of the drain-substrate junction field on the drain bias. We have used a logarithmic law in order to extrapolate the device lifetime for a 10% worst-case degradation (in our case transconductance degradation). The maximum drain bias that can be applied in order to obtain ten-year lifetime is shown in Fig. 6. The worst-case aging is obtained for surface channel devices with $L=0.1\ \mu\text{m}$. For $L=0.075\ \mu\text{m}$, the worst-case degradation is observed for buried channel devices. In any case V_{dmax} is much larger than the nominal drain voltage for this technology.

Hot carrier degradations will also be shown down to liquid nitrogen temperature.

References

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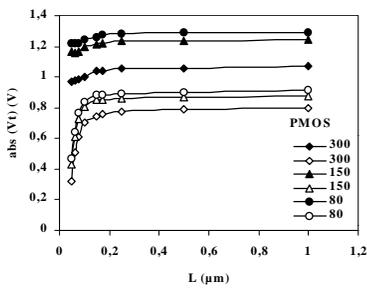


Fig.1 Threshold voltage versus mask length for surface channel transistors (empty box) and for buried channel devices (full box)

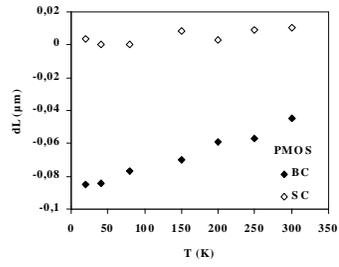


Fig.2 dL versus temperature for buried and surface channel pMOSFETs

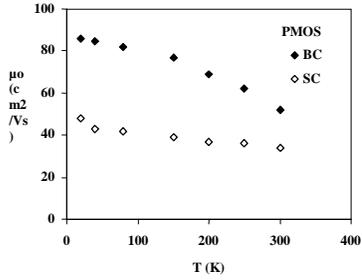


Fig.3 Carrier mobility versus temperature for buried and surface channel pMOSFETs

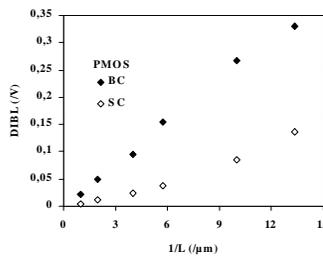


Fig.4 DIBL parameter versus temperature for buried and surface channel pMOSFETs

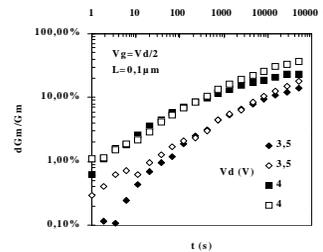


Fig.5

Transconductance

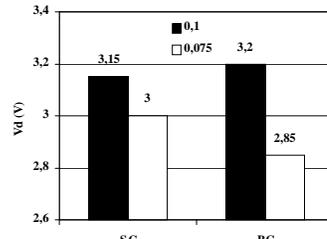


Fig.6 Maximal drain voltage extrapolated in order to obtain 10% transconductance degradation after ten years