

Low Temperature Characteristics of Ultra-short Gate Length Ultra-thin SOI MOSFETs and Si Nanowire Devices

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There has been intensive interest in Si nanoscale devices for possible use in future ULSI circuits. Many challenges to realize ultra-small Si devices for future electronic systems should be continued [1]. One approach aims to realize the ultimate ultra-small MOS device. The other is the approach from an atomic scale to obtain new functional Si nanodevices. In Si nanoscale devices, the fabricability and its stability of the ultra-small device components are indispensable to assure the expected device performance.

Very recently, we reported the high suppression of V_{th} roll-off and S-slope characteristics of the ultra-thin SOI n-MOSFETs in the 40-135 nm gate length regime [2]. The SOI MOSFETs were fabricated by using ELTRAN, SIMOX and wafer-bonding SOI wafers. In the case of the ELTRAN samples, we observed no structures in the sub-threshold characteristics even at 22 K. This result indicates that the uniform ultra-thin (4 nm) SOI MOSFET operates well even at a low temperature without any abnormal behaviors caused by disorders in the channel region. On the contrary, for some SIMOX samples, we observed complicated current oscillation in the I_d - V_g characteristics similar to that in the reference [3]. This behavior should be due to the Coulomb blockade effect. The wafer-bonding SOI samples showed very low device yield. The high uniformity of the SOI layer is essential for the ultra-thin SOI devices.

We have also investigated a Si nanowire nanodot memory transistor as a possible single electron memory [4]. The Si nanowire channel was fabricated by using an inorganic SiO_2 EB resist process after thinning of an ELTRAN SOI wafer. In the fabricated 15-10-nm-wide, 20-nm-thick Si nanowire device, we confirm that the Si nanodevice expectedly works as a single electron or few electron memory as shown in Fig.1 (13 K). However, in the other 5-10-nm-wide Si nanowire device, we observed an unintended Coulomb blockade effect due to the fluctuation of the Si nanowire width. We furthermore reveal the usefulness of the self-limiting oxidation effect to improve in uniformity of the Si nanowire.

In the future Si nanodevices, e.g., an ultra-thin SOI MOSFET and a Si nanowire device, the uniformity of the channel region is quite important to confirm the expected device operation. To solve the problem, proper selection of the starting materials and nanoformation technology such as self-limiting oxidation and utilization of crystallographic properties are required.

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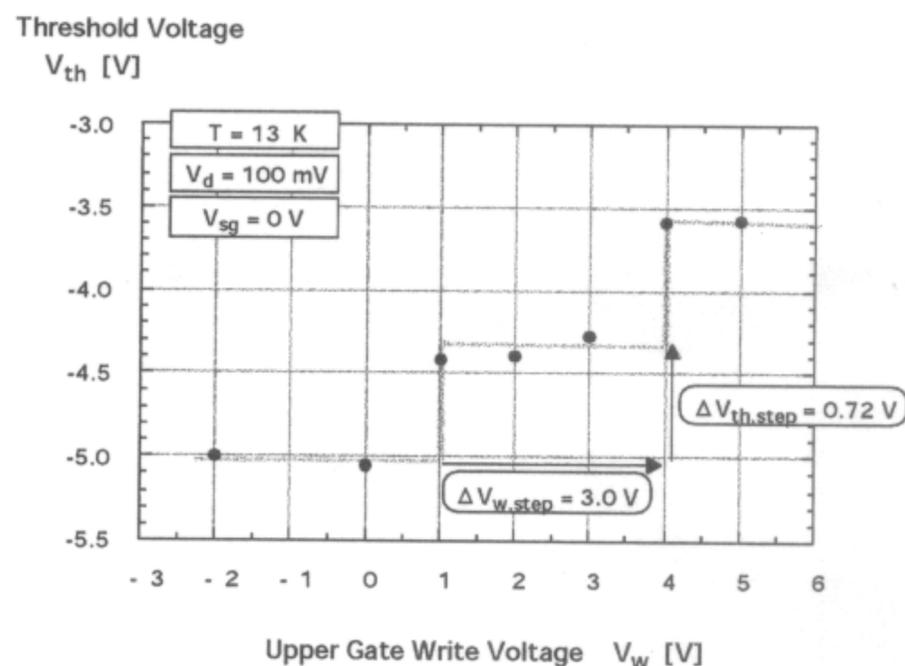


Fig.1 Single electron charging effect of the Si nanowire nanodot memory transistor in the threshold voltage (V_{th}) vs. write voltage (V_w) characteristic at 13 K.