

In_{0.5}Ga_{0.5}P/In_{0.2}Ga_{0.8}As Dual-Gate Pseudomorphic High Electron Mobility Transistors

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The aluminum-free InGaP-based compounds grown on GaAs substrate have recently attracted considerable attention due to the favorable energy band line-up [1-2]. A great number of high-speed electronic devices such as heterojunction bipolar transistors (HBT's) [3] and many kinds of field-effect transistors [4-5] have been intensively studied and reported.

In this letter, InGaP/InGaAs pseudomorphic high electron mobility transistors (PHEMT's) fabricated using single-gate and dual-gate methodologies have been characterized with special emphasis to precisely control the device linearity and the gate-voltage swing.

The InGaP/InGaAs pseudomorphic HEMT structure was grown on a (100)-oriented semi-insulating GaAs substrate by MOCVD. The epitaxial structure is composed of a 8000-Å GaAs buffer layer, a composite channel including a delta doped sheet of $\delta(n^+)=2 \times 10^{12} \text{ cm}^{-2}$ and a 100-Å undoped In_{0.2}Ga_{0.8}As layer, a 50-Å In_{0.5}Ga_{0.5}P spacer, a delta-sheet of $\delta(n^+)=3 \times 10^{12} \text{ cm}^{-2}$, a 300-Å In_{0.5}Ga_{0.5}P Schottky layer and a 100-Å $n=3 \times 10^{18} \text{ cm}^{-3}$ GaAs cap layer.

Concerning with device linearity, we refer to Fig. 1 for the current and transconductance as a function of the gate-source voltage. We find that the g_m - V_{gs} profile for the single-gate PHEMT really displays a broad plateau. The gate voltage swing defined as voltage range with 80% peak value of g_m is even larger than 4.5 V. That is, 90% gate operation voltage exhibit a voltage of 140 ($g_m/g_d=70/0.5$). The output current densities at $V_{gs}=0$ and +2 V are 300 and 480 mA/mm, respectively. Due to the extrinsic linearity obtained in single-gate InGaP/InGaAs PHEMT, the controllable gate voltage swing in g_m versus V_{gs1} is expected by this dual-gate approach. Fig. 2 shows the relation between the gate voltage swing and bias voltage of the second gate. It is found that the variable V_{gs} values are in the range of 0 to 4.5 V.

The detailed fabrication procedure and explanation will be reported.

ACKNOWLEDGEMENTS

This work is partly supported by National Science Council under the contract No. NSC 89-2215-E-019-003.

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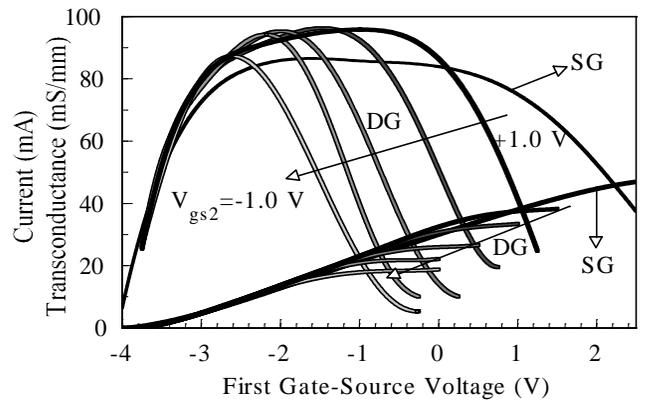


Fig. 1: the current and transconductance as a function of gate-source voltage.

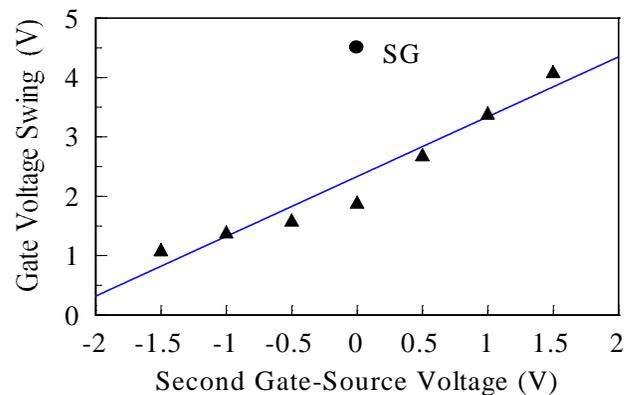


Fig. 2: the relation between the gate voltage swing and bias of the second gate.