# Effective Dual Damascene Process using IMD film Gap Fill Properties for Deep Sub-micron interconnects Technologies.

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Because copper film is extremely difficult to etch by using reactive ion etching (RIE), various dual damascene schemes as alternative process have been reported[1-4]. Damascene process has more advantages than that of RIE, such as excellence on reliability and reduction the number of process steps. One of the major issues for various dual damascene schemes is how to precisely control the concave structure of both a line trench and a via hole in the inter metal dielectric (IMD) film. Therefore, silicon nitride (SiN, SiON) film in damascene structure is very important as etch-stop layer for line-trench etching as well as the absorbent layer in lithography[5-6]. However, the use of silicon nitride film results in increased wire capacitance and also causes decrease of process margin due to limit on etch selectivity (<10) when its aspect ratio is increased.

The purpose of this presentation is report on newly interconnection scheme to obtain enough process margin in dual damascene without improving etch selectivity recipe to nitride film. The key processes on this integration scheme are briefly as follows. Firstly, plasma etching to form via-hole after IMD1 (i.e. PE-TEOS or Low-k films etc) and SiN are deposited simultaneously on a lower aluminum (M1) damascene interconnect. Via etching was performed in HDP C-5300 etching system manufactured by AMAT using $C_4F_8$ based plasma. Secondly, during the IMD2 film (HDP-USG or PETEOS) deposition, void was formed effectively in via hole by using deposition conditions with worse step coverage. Finally, trench etching to form metal line (M2).

Figure.1 shows the cross-sectional microscope (SEM) images when HDP-USG (1.0 ㎛) as IMD2 layers is deposited following the IMD1 (PETEOS: 2.0 ㎛) deposition and via formation (via size: 0.25 ㎛). Using appropriate IMD2 deposition conditions, we obtained successfully uniform void in via hole (i.e. 0.25 ㎛ to 0.60 ㎛). This is achieved by applying appropriate deposition conditions for either HDP-USG or PETEOS film. Due to the these voids formed in via hole, there are no observed significant erosions on trench corner after line-trench etching as shown in Fig.2. In addition, SiN film can be no longer necessary or reduced largely its thickness by using this process scheme. In this work, although PETEOS film used as IMD1 layers, this process scheme can be also applied for inorganic based low-k materials such as HSQ (Hydrogen silsequioxane), FSG (Silicon doped silica glass) and Nanoporous silica. Therefore, In ECS conference, we will announce experimental data for low-k materials as IMD1 layers. We expect that our process scheme will be very useful tools for future devices with high aspect ratio.

**References**

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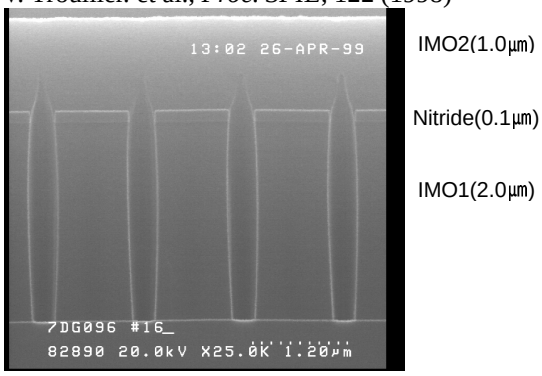


Fig. 1. Cross-sectional SEM images when HDP-USG as IMD2 layers is deposited following the IMD1 deposition and via formation

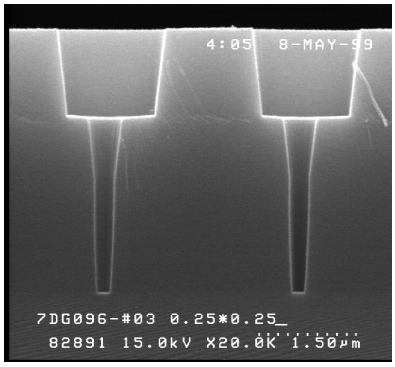


Fig. 2. Cross-sectional SEM images after line-trench etching.