

Quantum Devices and Integrated Circuits Based on Quantum Confinement in III-V Nanowire Arrays Controlled by Nano-Schottky Gates

Hideki Hasegawa

Research Center for Integrated Quantum Electronics and Graduate School of Electronics and Information Engineering, Hokkaido University, N-13, W-8, Kita-ku, Sapporo 060-8628, Japan

Tel: +81-11-757-1163, Fax: +81-11-757-1165

E-mail: hasegawa@rciqe.hokudai.ac.jp

Artificial quantum confinement in semi-conductor nanostructures has opened up exciting possibilities of constructing new quantum integrated electronics based quantum wire transistors (QWRTrs), electron-wave transistors, single electron transistors (SETs) etc. However, in spite of intensive research carried out over 20-25 years, there does not seem to exist, at present, any realistic approach to construct large scale integrated circuits (QLSIs) based on quantum devices.

The purpose of this paper is to present and discuss our novel hexagonal binary decision diagram (BDD) quantum circuit approach for III-V QLSIs[1,2]. In this approach, GaAs and InGaAs hexagonal nanowire networks are systematically controlled by nanometer-scale Schottky gates in order to implement circuits based on the BDD logic architecture [3].

Although quantum switching devices can realize delay-power products near the quantum limit set by the Heisenberg's uncertainty principle, they are "weak" in voltage gain and drivability [4] and "highly structure-sensitive". Thus, they are not suitable for use in the conventional Boolean logic gate architecture with AND/OR gates etc where very "robust and uniform" devices such as Si CMOS Trs are required. This is one of the difficulties encountered in the previous quantum device research.

On the other hand, quantum BDD circuits realize any logic function by wired arrays of BDD node devices each of which sends a single electron or a few electrons coming into the entry branch as the information messenger into either 0- or 1-branch, depending on gate input. Here, no direct output-to-input connection is required. Therefore, no large voltage gain, no precise input-output voltage matching, no large fan-in and fan-out numbers and no large current drivability are required. It is a good architecture for fragile quantum devices operating near the quantum limit of delay-power product.

For hardware implementation, we have paid attention to the basic three-fold branch symmetry of the node device, and have proposed [1,2] to use III-V hexagonal nanowire networks controlled by the Schottky wrap gate structure (WPG) proposed by our group [5]. The present Q-LSI structure is obviously applicable, in future, to molecular nanowire networks.

In this paper, formation of III-V hexagonal nanowire networks is discussed first. In addition to GaAs etched nanowire networks with wire widths of several 100 nm, we have recently grown submicron-pitch sub-10nm-wide InGaAs hexagonal nanowire networks by selective MBE on patterned InP substrates [6]. Here, hexagonal mesa-patterns are formed on (001) InP substrates by EB lithography and wet chemical etching,

followed by MBE growth of an InGaAs ridge structure whose integrity is most crucial for uniform and narrow nanowire growth. Then, nanowires are formed by depositing InAlAs/InGaAs/InAlAs onto the ridge structure by MBE. SEM/AFM/TEM studies have shown that an optimized low-temperature atomic hydrogen (H*) cleaning of InP patterns in the MBE chamber prior to ridge growth and H* irradiation during ridge growth are very powerful in reducing the nanowire width and enhancing the wire uniformity.

Secondly, a brief discussion is given on basic properties of nano-scale Schottky WPG gates. Fermi level pinning the free semiconductor surface surrounding the nano-Schottky gates is shown to have extremely important effects on the gate control characteristics [7]. From gated SdH oscillation and magnetotransport measurements combined with computer simulation, the Schottky WPG structure is shown to have features of tight gate control and strong electron confinement in addition to its simple lateral structure suitable for planar integration with device design flexibility.

Thirdly, various QWTr-based and SET-based BDD node devices formed on GaAs and InP substrates are introduced, and their fabrication process, transport mechanisms and path-switching characteristics are discussed. The devices include a 3-WPG single electron Y-switch [1] and two types of branch switch type BDD device [2] having a 1-WPG QWTr or a 2-WPG SET on each of the exit branches. Each of the node devices shows clear conductance quantization in the case of the QWTr device and clear conductance oscillations in the case of the SET device. With these, clear and sharp BDD path switching characteristics have been obtained.

Finally, small-scale integrated circuits including a GaAs hexagonal BDD two-bit quantum adder [8] are presented in order to demonstrate feasibility of integration. Layout designs without crossovers of nanowires are possible. The adder circuit can be constructed with a much reduced count of devices as compared with the Si CMOS version. It has shown a correct operation from 1.5 K up to at least 120 K by bias adjustments. The latter is due to the fact that, with temperature increase, the circuits show gradual transitions from the real quantum regime with a minimum delay-power product to a few electron quantum regime, and finally to the many electron classical regime. Thus, wire size reduction should lead to room temperature operation in the quantum regime. Key issues for more complex systems and future prospects are also discussed.

[1] S. Kasai, Y. Amemiya and H. Hasegawa, Tech.

Dig. 2000 IEEE IEDM (2000) 585.

[2] H. Hasegawa and S. Kasai, presented at Advanced Workshop on Semiconductor Nanostructures, Feb. 5-9, Queenstown, New Zealand. To appear in PhysicaE.

[3] N. Asahi, M. Akazawa and Y. Amemiya, IEEE Trans. Electron Devices **42** (1995) 1999

[4] S. Kasai, and H. Hasegawa: presented at IEEE DRC 2000 Conf. June 19-21, 2000, Conf. Dig. p.155

[5] S. Kasai, K. Jinushi, H. Tomozawa and H. Hasegawa, Jpn. J. Appl. Phys. **36** (1997) 1678.

[6] T. Muranaka, C. Jiang, A. Ito and H. Hasegawa: Thin Solid Films **380** (2000) 189.

[7] H. Hasegawa, T. Sato and C. Kaneshiro, J. Vac. Sci. Technol. B **17**, 1856 (1999)

[8] S. Kasai, and H. Hasegawa: to be presented at IEEE DRC Conf. June 25-27, 2001