

## The Nano-transistor

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Twenty-six years ago, Gordon Moore astutely observed that the complexity of an integrated circuit (IC), measured by the number of transistors incorporated into it, doubles about every 18 months with unerring regularity<sup>1</sup>. Since 1965 there has been more than a 1,000,000-fold improvement in the complexity of an IC without an increase in the manufacturing cost. About half of the improvement is due to miniaturization of the wires and transistors that are included in the circuit; the other half from factors such as increasing the size of the chip and design improvements. Right now, the semiconductor industry can manufacture logic that incorporates more than 40 million MOSFETs (metal-oxide-semiconductor field effect transistors) into a single circuit. Supposedly, within the next ten years at the same cost the semiconductor industry will manufacture logic chips that will nearly a half billion nanometer-scale MOSFETs (nano-transistors), packing about 5-10 nano-transistors/ $\mu\text{m}^2$ . These nano-transistors (see Figure 1) are expected to have a gate or control electrode as short as 70 nm and a gate oxide, which separates the control electrode from the current-carrying channel, as thin as about 1nm.

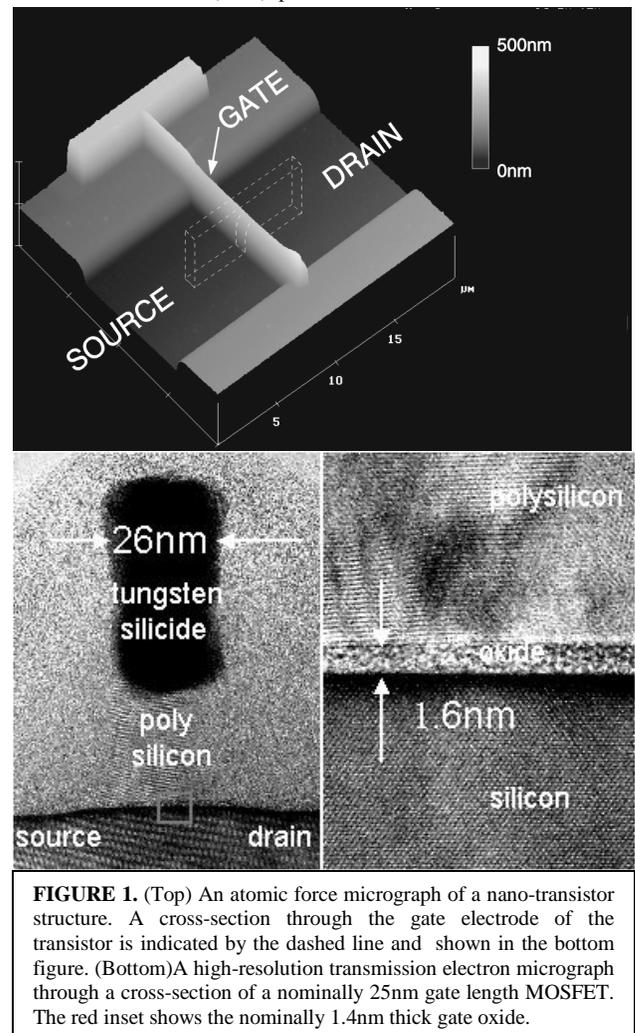
This extrapolation into the future is based on the ITRS Roadmap<sup>2</sup>, which is the current blueprint for the semiconductor industry. Implicit in the extrapolation is the assumption that the economics that currently drives integration will continue to do so, and that the physics governing transistor operation and its incorporation into an IC will permit it. Up to now, higher levels of integration have been economical and physically accessible through miniaturization. In particular, the accuracy of ITRS forecast relies on projected gains in transistor performance and on the reduction in power dissipation expected from miniaturization. But the ability to recover the projected gains by scaling the critical dimensions of the wires and transistors smaller, beyond the 70nm gate length technology node toward 25nm, may now be threatened by a confluence of limitations imposed by circuits, devices, materials and even the size of atoms.

An example of a looming threat to further miniaturization is the  $\text{SiO}_2$  gate dielectric, which is smallest feature in every IC.. The viability of sub-70nm MOS technology is contingent upon improvement in the drive current performance, and right now the thickness of the  $\text{SiO}_2$  gate oxide controls the drive current. Improvements derived from reducing the gate oxide thickness, can be used to lower the power supply voltage, thereby potentially improving reliability and reducing power dissipation. But we have recently shown<sup>3,4</sup> that the quantum mechanical tunneling current through ultra-thin  $\text{SiO}_2$  gate oxides makes thicknesses,  $t_{\text{ox}}$ , less than 1.4nm (a few atomic layers) impractical because the associated stand-by power dissipation becomes too great to remedy with air-cooling. Without corresponding improvements in reliability and reduction in power dissipation accomplished by miniaturization, further integration will be curbed, unless an alternative strategy for improving

performance can be discovered. Alternative gate dielectrics have been proposed to replace  $\text{SiO}_2$ , and pioneering device geometries such as the dual gate FET are being tested as expedient solutions, but neither of these alternatives promises continued unrestricted scaling. Moreover, these alternatives have yet to demonstrate performance that is superior to a planar MOSFET employing the thinnest practical  $\text{SiO}_2$  gate dielectric.

Our experimental results, obtained from nominally sub-40nm, planar nanotransistors indicate that it may be feasible to continue scaling the MOSFET even without continuing to reduce the oxide thickness and power supply voltage by using ballistic transport<sup>3,5</sup> to improve performance. Here, we report measurements of the drive current performance and transmission probability  $T$  of net flux emanating from the source to reach the drain. We demonstrate extremely high drive performance ( $I_{\text{Dsat}}=0.75\text{mA/mm}$  at a 0.6V gate overdrive in a 40nm gate length nMOSFET), which is consistent with numerical simulations of ballistic transport with  $0.8 < T < 0.85$ . The extremely high drive performance is achieved with surface fields in the semiconductor  $>1\text{MV/cm}$ , so that the scattering in the channel is due predominately to interface roughness. We show that to maximize  $T$ , the surface field can be reduced by either increasing  $t_{\text{ox}}$ , reducing the gate voltage or decreasing the interface roughness.

1. G.E. Moore, IEEE IEDM Tech. Dig. (1975) 11.
2. International Technology Roadmap for Semiconductors, published by the Semiconductor Industry Association, San Jose, CA (1999).
3. G. Timp, et al. IEDM Tech. Dig. (1998) 615 and G. Timp et al. IEDM Tech. Dig. (1999) 55.
4. D. Muller et al., Nature, 399 (1999) 758.
5. S. Datta, F. Assad, M.S. Lundstrum, Superlattices and Microstructures, 23, (1998), p 771.



**FIGURE 1.** (Top) An atomic force micrograph of a nano-transistor structure. A cross-section through the gate electrode of the transistor is indicated by the dashed line and shown in the bottom figure. (Bottom) A high-resolution transmission electron micrograph through a cross-section of a nominally 25nm gate length MOSFET. The red inset shows the nominally 1.4nm thick gate oxide.