A novel semiconductor nano-patterning approach using AFM-scratching through thin oxide layers

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Patterned metal layers are incorporated into integrated circuits to provide electrical conductors, junction devices, connection pads, and optical attenuators (in optodevices). These are usually fabricated by depositing the metal (using chemical vapor deposition or electroplating) over the entire surface and then removing the undesired metal by etching the pattern through a mask or by chemical mechanical polishing, or by metal evaporation over a patterned resist and liftoff, or by electroless plating through a mask [1].

An alternative approach to ''patterned'' metal deposition has been presented before [2]. It is based on an electrochemical process, where the ''maskless'' patterning results from the electrochemical sensitivity to intentionally created surface defects using focussed ion beam implantation.

Atomic force microscopy (AFM) is a powerful instrument for surface imaging. But it can also be used to investigate the mechanical properties of surfaces or to nanomachine the surfaces in the micro- and nanoscale [3]. Previously, it has been demonstrated that it is possible to obtain nano-scratches on silicon surface using an AFM equipped with a single-crystalline diamond tip [4]. The present study investigates the use of this AFM-scratching method as surface pre-sensitization for selective metal deposition.

Metal deposition was carried out in metal ion containing electrolyte on *p*-type Si which was previously AFM-scratched. The first results exhibited a high reactivity in the vicinity of the AFM-grooves but the deposition was not sufficiently defined as it is shown on figure 1.

In order to obtain a higher degree of selectivity, AFM-scratching was performed on samples carrying either native oxide layer (15-20 Å thick) or thermal oxide layer (~40 Å thick). Due to their insulator properties, the SiO_2 layers act as mask for the metal electrochemical deposition whereas in the scratched openings metal deposition can take place easily. Nanoscale metal (e.g. copper) lines could be successfully and selectively be plated onto the *p*-type silicon substrates covered by native or thermal oxide but the thermal oxide has two advantages over the native oxide (see e.g. Fig. 2). On one hand the thickness of the thermal oxide is controlled by the heating paramaters. On the other hand it allows the HF treatment (hydrogen termination of the Si within the grooves) without any risk of eliminating the oxide layer on the rest of the surface. The masking effect of the oxide layer was also carried out on *n*-type Si (100).

References

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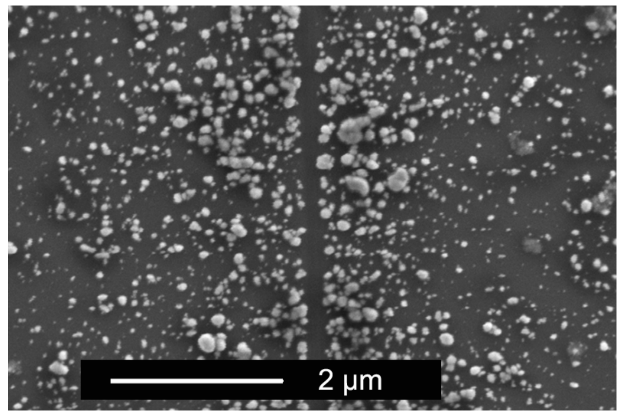

Fig. 1: SEM image of copper deposit on AFM-scratched *p*-type silicon (H-terminated surface). The groove was produced with a force of 15 μN. Deposition was carried out from $CuSO_4$ (0.01 M) + H_2SO_4 (0.05 M) at -400 mV (Ag/AgCl) during 15 s.

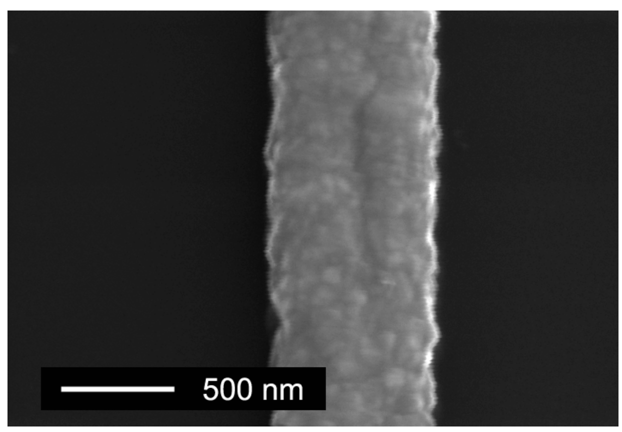

Fig. 2: SEM image of copper deposit on AFM-scratch in *p*-type silicon previously covered by a thermal oxide layer of ~40 Å. The grooves was produced with a force of 15 μN. Deposition was carried out from $CuSO_4$ (0.01 M) + H_2SO_4 (0.05 M) at -500 mV (Ag/AgCl) during 10 s.

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