

Fundamental Aspects of Electrodeposition - Zinc, Bumping and Via filling

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Introduction

I am often asked by Ch.E. colleagues that which field did I major during Ph.D.. I majored statistical mechanics and did not major electrodeposition nor electrochemistry. After my Ph.D., I worked in industry for ten years and this is the place where I learned and taught myself about electrodeposition - **Zinc, Bumping and Via filling**. Good colleagues, good books and careful observation by high resolution SEM really are the origin of my research knowledge on electrodeposition. Another origin of research is the recent developments in electronics and packaging.

Zinc electrodeposition

Zinc and zinc alloy electrodeposited steel sheets are used for anti-corrosion surface treatment for automobile bodies. I did both developments and fundamental research of zinc alloy electrodeposits in industry. I started my fundamental work with classification of inter-metallic compounds and crystal morphologies(1). With TEM and SEM, the zinc alloy electrodeposits are found to grow with lateral growth of macrosteps on the (00· 1)η and the Γ-phase particles dispersely precipitate within the η-phase(2,3). The hexagonal columnar crystals of zinc and zinc alloy electrodeposit grow with stacking(lateral growth of macrostep) of hexagonal plate thin in the direction of c-axis. With having these basic understanding of growth in industry, I was able to develop my research into AFM and zinc composite, etc, at university(4-8).

Bumping

Bumps are used for high density interconnection of liquid crystal display(LCD) and it's driver IC. I also started this research in industry since I was involved in the development of bumped type anisotropic conductive film(9). This is the starting point of my current distribution study. With a collaboration of Professor K.Fukui, numerical computation of fluid dynamics has been studied at the diffusion controlled region. Numerical computations and experimental results coincidence have been examined for bumping with high Peclet numbers, photoresist angles, deep cavity, deep cavity for wafer level CSP(10-13).

Via filling

Copper via filling become indispensable technology for circuit fabrication on chip and also on PCB. I started this research couple of years ago. The via filling can be achieved by both effects of via outside inhibition and via bottom acceleration. The inhibition effect is caused by adsorption of PEG molecules of several ten nms, which we first observed with high resolution FESEM(14). The acceleration effect is caused by SPS. With a patterned cathode, we succeeded in measuring this acceleration effect(15). Copper via filling is the most important topic in my current research and I run many research topics on this.

Recent electronics packaging processes

Fig.2 shows the recent electronics packaging processes. Copper via filling techniques are intensively developed for Damascene, build up PCB and three dimensional packaging. Micro bumping

technologies is developed for higher pitch LCD interconnection and three dimensional packaging. Packaging will become as wafer level and will be involved in semiconductor fabrication process.

To conclude

Electrodeposition technology has been used for packaging and PC board but now intensively penetrating into the semiconductor with copper Damascene. Dry and wet technologies are merging into the other. Electrodeposition is low cost nanometer technology and will be very intensively used for additive method forming circuits – packaging with wafer level, optical electronics and probably quantum mirage effects.

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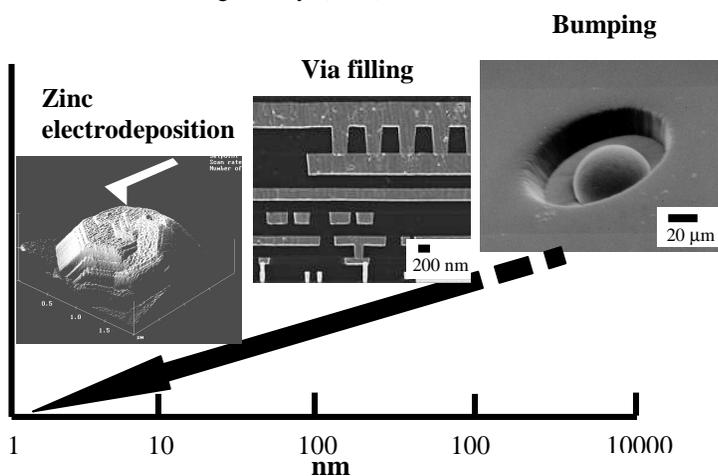


Fig.1 Size scale overview.

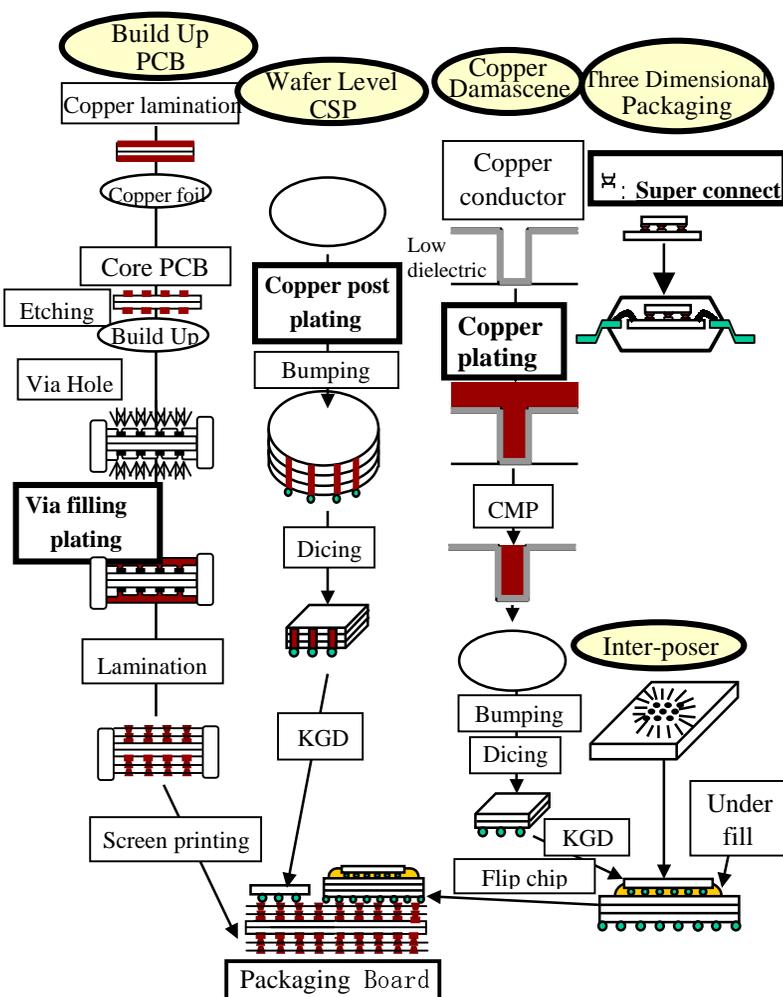


Fig.2 Recent electronics packaging process.