

A new process for silicon field emitter arrays fabrication using HF photoelectrochemical etching

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Integrated field emitter arrays are currently under investigation for vacuum microelectronic applications. Many methods have been reported for fabrication of field emitter arrays; for example, metal tips evaporation into a trench (Spindt type emitter) [1], crystal Si tips formation by isotropic [2] or anisotropic [3] silicon etching. Typical process fabrication of a silicon field emitter array consists of tip fabrication by silicon etching, evaporation or growth of gate oxide, deposition of metal gate and lift-off of the gate insulator to uncover the silicon tip.

In this work, we propose a new fabrication process for gated silicon field emitters, based on photoelectrochemical silicon etching in HF electrolyte solution. The process is able to form silicon tips with high aspect ratio (tip height/tip width ratio) and self-aligned metal gate using only one mask. The metal gate hole width can be lithographically controlled, and it is independent of silicon dioxide lift-off, with advantages in terms of reproducibility of the structure.

Photoelectrochemical silicon etching in HF [4, 5] has already been used for highly anisotropic macropore array fabrication. Under specific conditions, for a flat surface silicon wafer, surface defects act as seeding points for macropore formation. By pre-patterning the wafer surface with defect sites (pyramidal notches obtained by KOH etching) we can pre-determine where the macropores will grow (Fig. 1a). We found that, if the pyramidal notches are not complete, the macropores grow at the corners of the notch (Fig. 1b) and a silicon crystalline pillar is left in the center. Interestingly, the width of silicon tips can be easily controlled by the initial KOH etching, while the tip height can be independently controlled by etching time. A micrograph SEM cross-section of a photoelectrochemical fabricated microtips array is shown in Fig. 2. The height of each tip is 15 μm , while the hole width is 5 μm .

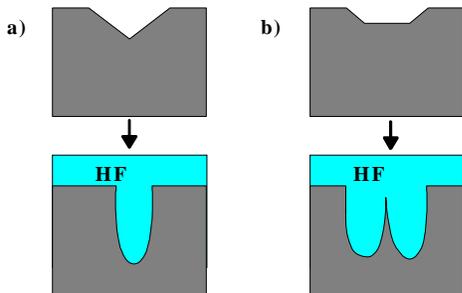


Figure 1: Macropore formation: a) only one macropore grows if the pyramidal notch is complete; b) one macropore at each corner grows if the pyramidal notch is not complete.

The silicon field emitter process fabrication is sketched in Fig. 3. Starting material is a *n*-type silicon wafer (100) oriented, 2.4-4 $\Omega\text{ cm}$ resistivity. A thin oxide layer (2000 \AA thick) is grown on the samples by thermal oxidation. Incomplete pyramidal notches are defined, through the patterned silicon dioxide, by KOH etching (Fig. 3a). Photoelectrochemical etching in HF is used for silicon tips fabrication (Fig. 2b). Thermal oxidation of the sample is then performed in order to grow silicon dioxide as gate insulator (2000 \AA thick) (Fig. 3c). A Cr metal gate (2000

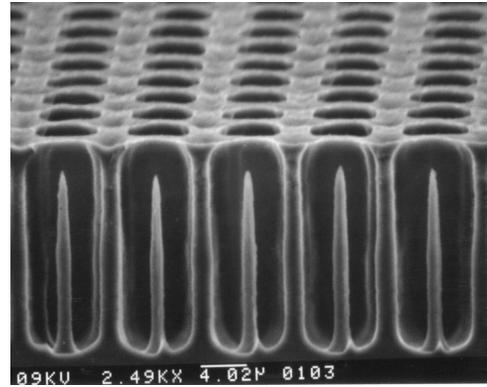


Figure 2: Micrograph SEM cross-section of silicon microtips fabricated by photoelectrochemical etching in HF.

\AA thick) is deposited on the silicon dioxide by thermal evaporation (Fig 3d). The last step of the fabrication process is the metal cap lift-off, which uncovers the silicon tips (Fig. 3e).

Test structures for *I-V* measurements are under fabrication.

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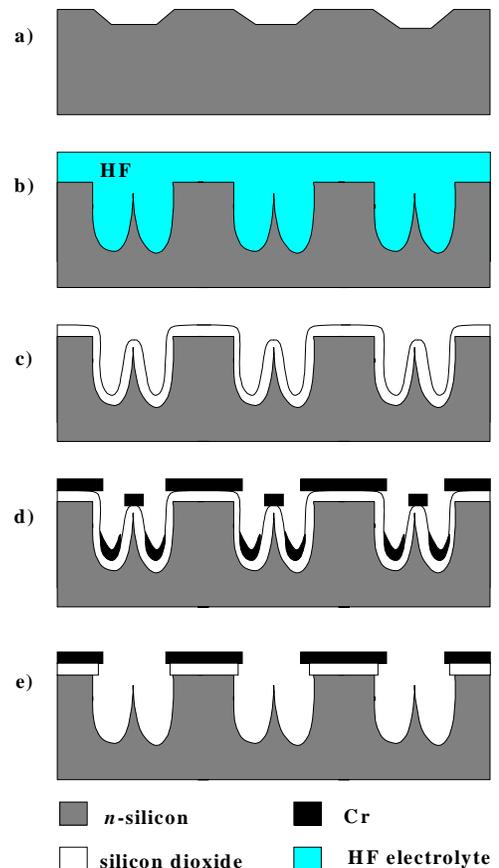


Figure 3: Schematic process of silicon field emitters fabrication by photoelectrochemical etching in HF.