Site Control of Etching Pits in Semiconductor Single Crystals Using Direct Nano-imprinting

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There has been growing interest in the development of novel processes for fabrication of submicron or nanometer-scale structures because of their potential for application in electronic, optoelectronic, and micromechanical devices. In those processes, patterning with high throughput in addition to a high spatial resolution is indispensable. One candidate for such a simple process is the direct imprinting process in which a master mold is used for the preparation of a replicated pattern on the surface of a substrate. In previous reports, we described that the imprinting process is applicable to the patterning of metal (Al) [1] or semiconductor single crystal (InP) [2] on a nanometer scale, and that it is effective for the fabrication of channel array architectures with a high aspect ratio by subsequent anodizing process. In this study, we describe the direct imprinting process for semiconductor single crystals using a master mold made of SiC, and fabrication of highly ordered pore by subsequent anode etching.

The process for nano-imprinting and the post-etching process are shown Fig.1. The mold had a hexagonally arranged ordered array of convexes on its surface with 200nm intervals. The (100)-oriented Si wafer was used as a substrate for nano-imprinting. After the SiC mold was placed on the Si wafer, the mold was pressed using an oil press at room temperature under a pressure of 3300kgcm^{-2}. Through this process, no crack was observed in the Si substrate. Contact was achieved by vacuum evaporation of aluminum (60nm) on the rear side of Si. The etching of Si was conducted under a constant current condition of 5mA/cm^2 in 2% HF for 1 hour.

Figure 2 shows a SEM image of the surface of Si after the direct imprinting. The formation of an array of concaves was confirmed. The interval of the concaves was in good agreement with the convexes in the SiC master mold. Figure 3 shows a SEM image of the Si after the post-etching treatment. The ordered arrangement of straight pores with a high aspect ratio, which was induced by the concaves by direct imprinting, is observed in Fig.3.

Direct imprinting on the nanometer scale at room temperature was achieved on semiconductor single crystal using a SiC master mold. The present direct imprinting process and subsequent etching treatment will be effective for other semiconductor single crystals.

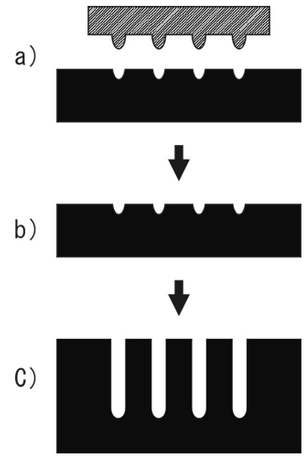

Fig.1 Schematic of direct imprinting and etching of semiconductor substrate: (a) SiC mold and substrate, (b) textured substrate, (c) etched substrate.

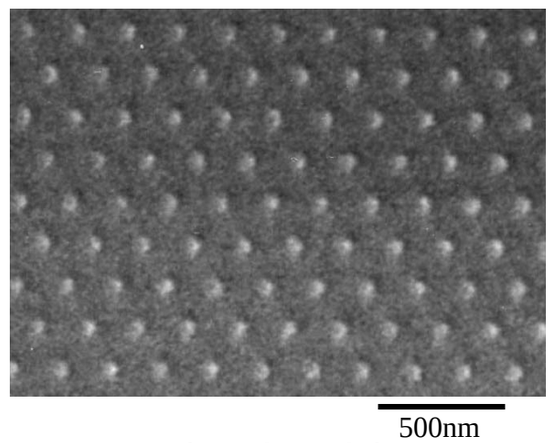

Fig.2 SEM image of Si single crystal after imprinting with SiC mold.

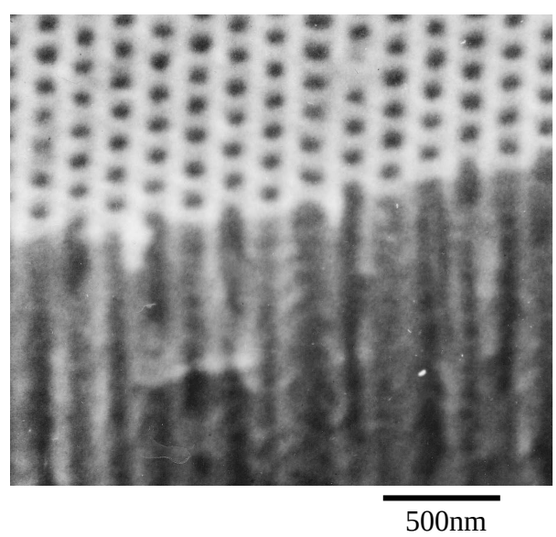

Fig.3 SEM image of the porous Si after the anode etching treatment using the imprinting.

1)H.Masuda, H.Yamada, M.Satoh, H.Asoh, M.Nakao, and T.Tamamura , Appl.Phys.Lett., **71**, 2770(1997)
2)H.Masuda, K.Yasui, T.Yanagishita, M.Nakao, T.Tamamura, and K.Nishio., Jpn.J.Appl.Phys., **39**, L256 (2000)