

TOWARDS PHOTONIC DECODERS

Saied Hemati, Amir Banihashemi

hemati@sce.carleton.ca, Amir_Banihashemi@sce.carleton.ca
Ottawa-Carleton Institute of Electrical and Computer Engineering (BCWS)
1125 Colonel By Drive, Carleton University
Ottawa, Ontario, K1S 5B6, Canada
Tel: +1 613 520-2600 ext. 8026, Fax: +1 613 520-5727

Abstract:

Full optical networks, gradually become a reality and in this regard, there is a burgeoning interest in moving from electronics towards electro-optical and finally full-optical networks. Optical amplifiers and switches, optical routers and DWDM optical components have all been produced on this base. In this paper, we for the first time present the idea of using optical components for decoding very high-speed digital information. In fact, the concept of soft decoding, which uses analog inputs for decoding, has currently found extensive applications for advanced coding schemes and because of their complexity, there is no known method for implementing them in high-speed applications. In this paper, fundamental building blocks of sum-product decoding algorithm are introduced and it will be shown that by using linear Y-fed optical directional coupler, these blocks can be implemented.

Keywords: Directional coupler, Integrated Optics, Soft Decoding, Sum-Product decoding

Introduction:

During the past decade, there has been a rapidly interest in optical signal processing systems for optical communication and optical computing has stimulated a great deal of research. Tunable lasers and filters, optical amplifiers and switches and other optical components have been the topic of lots of researches. Among them, coupled wave-guides are fundamental building blocks of many interesting electro-optical devices including laser diode arrays, optical modulators, switches, beam splitter, wavelength router, passive star coupler and highly frequency selective filters for high speed optical communication networks [1-11].

Currently, a linear Y-fed directional coupler has been demonstrated that is very attractive for analog optical systems [10-11]. This directional coupler has been mainly designed for working as an external analog modulator and has a very good linear performance. This specification as well as high speed and low deriving power made this directional coupler desirable for implementing a new class of decoders, which work on analog input signals for decoding digital information. These decoders could be used for high speed long-haul optical communication networks as well as high speed wireless links.

In this paper, we try to show that the sum _ product algorithm, which is used for decoding, advanced codes, has this potential to be implemented by linear directional coupler.

Channel Coding:

The channel coding is generally required in the optical communication systems to improve bit error rate (BER) performance. Reed _ Solomon and convolutional codes have primarily been proposed as coding schemes in optical communication systems [12]. In particular, the Reed _ Solomon (255,239) code is now commonly used by most submarine systems suppliers. However, for the next generation of high speed DWDM, long haul systems, better coding schemes must be sought [13].

Recently, in the channel coding community, there has been much interest on turbo code, introduced by Berrou et al in 1993 [14] and low-density parity check (LDPC) codes which were invented in 1963, but were only recently discovered to be almost as good as turbo codes [15]. They showed that it was possible to transmit digital information at a rate close to channel capacity as predicted by Shannon in 1948.

The benefits of using advanced coding schemes for optical communication systems have been investigated in the literature [13,16,17], but there is still a serious unsolved problem for implementing the related decoders. In fact, the task of implementing advanced decoders is not a trivial one, especially at very high bit rates.

Advanced decoders are probabilistic rather than algebraic and their inputs are not simply digital numbers, instead they work with real numbers and analog input signals (soft inputs instead of hard inputs) and conversion to digital estimates occurs after the decoding (soft decision instead of hard decision). This approach gives them 3dB additional coding gain [18]. It has been shown that analog VLSI based decoders, which use analog signal processing, have better performance in terms of speed and power and silicon area consumption in comparison with digitally implemented decoders [19-21]. While reported decoders show good performances, but their speed is too slow to be applicable in modern optical communication. In particular, in [19] for a relatively modest coding scheme, the highest bit rate is 100 Mbps and as it

will be shown in this paper, their approach cannot go much further in terms of speed. Some thing that we are going to show that is achievable by using linear optical couplers.

Sum _Product Decoders:

Basically decoding is a decision making process. Based on the received data vector in the receiver, decoder tries to figure out which information bits have been generated by information source. It can be shown that if information source generates different messages with equal probability, the optimum decoder will be a decoder that use likelihood as its decoding rule and decodes the received information to the most likely defined codeword. There are different methods for implementing maximum likelihood algorithm, which for complex codes, most of them become exponentially difficult.

Sum _ product algorithm is a well-known decoding algorithm that for a large category of codes gives the optimum result and for the rest of codes is often assumed to be the most reliable known algorithm. Hopefully, in terms of basic building blocks, sum _product algorithm is relatively simple and its computation rules consist of only multiplication and addition [22-24].

Soft Xor and equal gates are two basic building blocks in sum _ product algorithm that their inputs are real numbers and each input is represented by two nonnegative numbers P(0) and P(1), that add up to one. The value of P(0) is (or interpreted as) the probability that the input bit is zero; P(1) is (or interpreted as) the probability that the input bit is one[20].

Equal gate has two inputs (X, Y) and one output (Z) and its function is as follows:

$$\begin{bmatrix} P_Z(0) \\ P_Z(1) \end{bmatrix} = \gamma \begin{bmatrix} P_X(0)P_Y(0) \\ P_X(1)P_Y(1) \end{bmatrix} \quad (1)$$

where γ is a scaling factor for keeping the values reasonable. The Soft Xor gate does the following operation

$$\begin{bmatrix} P_Z(0) \\ P_Z(1) \end{bmatrix} = \begin{bmatrix} P_X(0)P_Y(0) + P_X(1)P_Y(1) \\ P_X(1)P_Y(0) + P_X(0)P_Y(1) \end{bmatrix} \quad (2)$$

and at the output of decoder, every bit is converted to the most probable state (0 or 1) according to the related probabilities.

These gates work with analog inputs and implementing a large number of high precision full digital multiplier and adder is power and area consuming. Also for iterative decoding each iteration needs at least one time slot for each step that means low speed performance. For these reasons there has been a great interest in analog implementation of these gates. Two separate groups in the last few years tried to implement advanced decoders by analog VLSI, Hagenauer et al [21] and Loeliger et al [19,20]. Both groups worked on modified Gilbert multiplier and BiCMOS technology. They intended to explore the semiconductor properties and use it in an innovative way. Although both groups have had different approaches, their main building blocks are the same. The only difference between these two groups is the way they have used for applying inputs to the Gilbert cell and how they have defined the outputs. While Hagenauer et al defined voltage base inputs and outputs, Loeliger et al defined them as currents. This approach let them to easily add current without any additional block based on Kirchhoff's Current Law at especial nodes, while Hagenauer's group had no choice but construction of voltage adder, which increases the complexity and causes extra delays and lower speed. We here do not intend to compare these two designs and discuss about their profits and constrains but because of similarities between our approach and the design of Loeliger's group, it is worth to introducing their main building block in brief. Fig .1 shows an Emitter Coupled or differential pair circuit that was used in Loeliger's design. P(0) and P(1) are the inputs and I₁ and I₂ are the outputs and I is a constant current and if we neglect Base currents then it is equal to summation of I₁ and I₂. For ideal Bipolar Junction Transistors (BJTs) we have

$$I_C = I_s \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \approx I_s e^{\frac{V_{BE}}{V_T}} \quad (3)$$

Where I_C is Collector current, I_s is reverse saturation current, V_{BE} is the Base-Emitter voltage and V_T is the thermal voltage. For transistors in Fig.1, one can write

$$V_{BEQ1} + V_{BEQ3} = V_{BEQ2} + V_{BEQ4} \quad (4)$$

And easily can show that

$$I_1 = I \times P(0) \quad , \quad I_2 = I \times P(1) \quad (5)$$

So this block with ideal components acts exactly as a splitter with the ratio of P(0): P(1), (let's call this block P-P' splitter for future references) though this ratio is not constant and must be adjusted as fast as the incoming information.

Having this P-P' splitter block, Soft Xor gate can be constructed as shown in Fig.2 , which by the way , is exactly the well known Gilbert cell. Equal gate can also be implemented by P-P' splitter in a similar way but some amplification will be necessary.

By using more soft Xor gates (or equal gates), we can calculate soft Xor (or equal function) of more inputs, and in reality we often need to calculate it for quite a few inputs. The reported analog VLSI decoders have this drawback that, as the number of blocks increases the maximum speed of the circuit decreases. As a rule of thumb, the overall delay will be equal to summation of each block's delay and maximum frequency of operation is divided by the number of blocks. In practice, the final circuit has even a slower frequency response because of nonlinear performance of this circuit, which produces lots of harmonics even for a standard Gilbert cell and limits the maximum frequency of the circuit. Therefore those reported designs are limited to not too complex and too fast applications and cannot be used for high-speed optical applications.

Y-Fed Optical Directional Coupler As A P-P' Splitter:

An optical directional coupler is a very interesting electro-optical component that consists of two optical wave-guides which are brought in close proximity with each other over an interaction length, and coupling occurs between the optical modes of the two wave-guides via their evanescent fields and a Y-fed directional coupler consists of a single mode input wave-guide feeding a symmetric Y-junction connected to a directional coupler as depicted in Fig.3. For no applied modulating voltage, light coupled into the input straight wave- guide splits evenly between the coupled wave-guides but when a non-zero voltage is applied to the electrodes, causes unequal splitting of the light between the outputs. Because of the condition of power conservation the total output power in upper and lower wave-guides is equal to the light power launched into the input wave-guide. The relationship between the applied voltage to the electrodes and the intensity of the output light in one of the output wave guides (that is called modulation (transfer) curve) is often nonlinear. But currently a highly linear Y-fed optical directional coupler has been reported that shows a good linear performance and has an optical modulation depth close to 100% [10,11]. The modulating curve for the reported optical directional coupler can be expressed by the following relationship, with a good accuracy:

$$\frac{L_1}{L} = a \times (V + b) \quad (6)$$

$$\frac{L_2}{L} = a \times (b - V) \quad (7)$$

Where L, L₁ and L₂ are respectively the intensity of light in the input and outputs and V is the modulating voltage. *a* and *b* are two constants that are determined by the geometrical property of directional coupler, for instance in [11] *a* = 0.05 and *b* = 10 volts. Let us set V as a function of P(0) (which is (or interpreted as) the probability that the input bit is zero) as follows:

$$V = \frac{P(0)}{a} - b \quad (8)$$

Then we will have the following relationship for L₁ and L₂.

$$\frac{L_1}{L} = P(0) \quad , \quad \frac{L_2}{L} = 1 - P(0) = P(1) \quad (9)$$

Which are exactly same as (5), when currents are substituted by light intensities. It means that by just amplifying the input voltage (corresponding to P(0)) and adding an offset voltage and then applying it to a linear directional coupler, we can implement a P-P' splitter block which is the basic building block of the sum-product decoders. Here computation in a P-P' splitter is performed by variation of light intensity and addition is performed on the power of light. The speed of this block is just limited by its electrical part and when we build a chain of these blocks, for implementing a complex function; again electrical parts constrain the speed. It is because of very high-speed performance of optical part in comparison with electrical parts that adjust modulating voltages. In fact total optical delay due to a large number of these blocks will be much smaller than the delay due to the electrical parts. So if the voltages of the electrodes are applied simultaneously, the speed of the operation will not depend on the number of blocks, as far as the number of blocks is reasonable. While in the reported analog VLSI decoders, as we discussed before, the speed will be reduced drastically as the complexity increases.

Conclusion:

In the present paper, a preliminary study for implementing advanced decoders by optical blocks was presented. The application of these kinds of decoders does not limit to optical applications, because the inputs are in form of voltages and final outputs will be finally in form of electrical signals (after transferring from light into electrical signals via APDs). The most promising property of such an implementation will be its speed of operation. Hopefully optical

components are now definitely mature and also there are many applications for high-speed decoders. So it is quite probable to see optical decoders in close future though there are still lots of challenging problems to overcome.

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Figure 1. (a) A P-P' splitter block in [19], (b) Symbol of a P-P' splitter block.

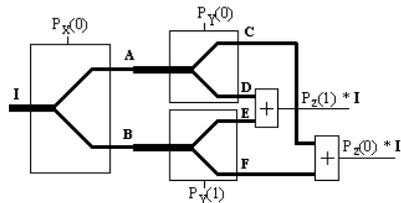


Figure 2. a soft Xor block
 $A = P_X(0) * I$, $B = P_X(1) * I$
 $C = P_X(0) * P_Y(0) * I$, $D = P_X(0) * P_Y(1) * I$
 $E = P_X(1) * P_Y(0) * I$, $F = P_X(1) * P_Y(1) * I$

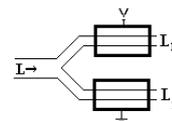


Figure 3. A Y- fed directional coupler