

Thermal stability of Pd/Al_{0.11}Ga_{0.89}N Schottky diodes

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The Schottky barrier height of Pd on n-Al_{0.11}Ga_{0.89}N has been measured to 0.95, 0.98 and 0.93 eV using Current-Voltage (I-V), Capacitance-Voltage (C-V) and Current-Voltage-Temperature (J-V-T) measurements, respectively. I-V barrier height increases and considerably no changes have been observed up to the temperature 450 °C/5 min annealing. C-V barrier height increases (1.68 eV) up to the annealing temperature 250 °C/5 min and decreases for higher temperature annealing. The increase of barrier heights for low temperature annealing is not due to any macroscopic interfacial reaction. Rectifying behaviour has been observed up to the annealing temperature 500 °C/1 hr with the I-V barrier height 1.23 eV, ideality factor 1.35 and the C-V barrier height 1.39 eV. The stable barrier height and ideality factor at high temperature annealing may leads to the interfacial reaction in the Pd and Al_{0.11}Ga_{0.89}N interface.

Apart from opto-electronic devices, III-V nitrides are also appealing because of their chemical, thermal stability, high break down field, and high saturation drift velocity. These properties make the nitrides suitable for high temperature/ high power electronic devices. For high temperature applications Schottky and Ohmic contacts which do not deteriorate high temperature operation. Schottky characteristics of

GaN and Al_{0.11}Ga_{0.89}N using various metals Ag, Ti, Au, Pd and Ni have been investigated and this experimental result indicates that barrier height varies with the metal work function. In this article, we report the Schottky characteristics of Pd/n-Al_{0.11}Ga_{0.89}N Schottky diodes as a function of annealing temperatures. The electrical characteristics were compared with the surface morphology of the annealed diodes using Atomic Force Microscopy (AFM).

Growth of Al_{0.11}Ga_{0.89}N layer and device processing detail has been published elsewhere [1]. Current-voltage (I-V) and capacitance-voltage (C-V) measurements were carried to find out on the fabricated diodes. Current-Voltage measurements with different temperatures (23 to 300 °C with 50 °C increment) were also carried out on the diodes in the nitrogen atmosphere. The capacitance-voltage measurements were carried out at 1 MHz. Atomic Force Microscopy (AFM) was used to measure the surface roughness of the as-deposited and annealed diodes.

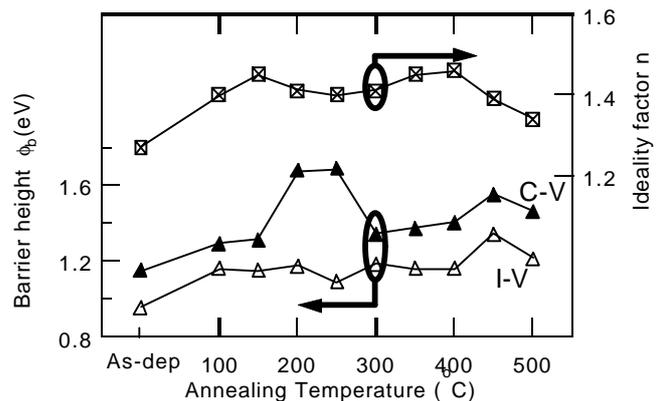


Figure 1. f_b and n vs. annealing temperature

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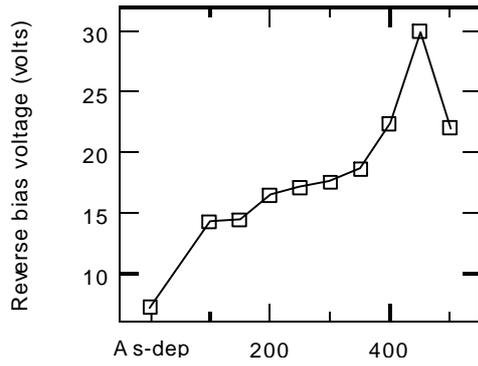


Figure 2. Reverse voltage vs. annealing temperature

I-V, I-V-T and C-V parameters are tabulated in the Table I. The value within the parenthesis is the value of 300 °C treated diodes measured at room temperature. The low barrier height and small Richardson constant (A^*) found by the I-V-T method are the possibility of non-uniform current distribution in the diodes. Enhancement of barrier height with good rectifying characteristics was observed that in 300 °C treated diodes (table I). This may be due to the interfacial reaction between metal and semiconductor contacts. C-V barrier height values are higher than the I-V barrier heights of as-deposited and annealed Schottky

diodes. The reason might be partly due to the image-force barrier lowering effect [1].

Table I. Schottky parameters of as-deposited and annealed (450 – 500 °C) diodes

Temperature (°C)	Reverse Voltage (V)	n	$f_b(I-V)$ (eV)	$f_b(C-V)$ (eV)	$f_b(I-V-T)$ (eV)	A^* (A/cm^2F^2)
As-dep	7.2	1.27 (1.30)	0.95 (1.23)	0.98	0.93	0.0007
450 / 5 min	30.0	1.39	1.34	1.55	-	-
450 / 30 min	24.9	1.38	1.28	1.47	-	-
450 / 1 hr	22.2	1.41	1.24	1.58	-	-
500 / 5 min	16.0	1.34	1.21	1.46	-	-
500 / 30 min	21.0	1.34	1.27	1.38	-	-
500 / 1 hr	21.0	1.35	1.23	1.39	-	-

Increase of I-V and C-V barrier heights with annealing temperatures were observed (figure 1). There was a sudden increase of C-V barrier height of Pd diode for the annealing temperatures 200 °C/5 min and 250 °C/5 min. Increase of C-V barrier height may be due to interfacial changes such as gallium out-diffusion, changes in dielectric constant. Structural point of view, XPS measurements are in progress. I-V barrier height of Pd Schottky diode decreases with annealing time (5 min – 1 hr) increases for 450 °C. However not much changes have been observed on ideality factor and 500 °C. The increase of surface roughness (0.96 nm to 7.2 nm) may be because of gallium out-diffusion and mixing of Pd and AlGa_{0.11}N at the interface due to thermal annealing. Reverse bias voltage (RV) for a fixed reverse leakage current 4 nA gradually increases with annealing temperatures up to 450 °C/5 min and it gradually decreases with higher annealing temperatures (Figure 2 and table I). High reverse voltage 30 V has been observed for 450 °C/ 5 min annealed diodes. In conclusion, Pd/Al_{0.11}Ga_{0.89}N Schottky diode characteristics were carried out at different annealing temperatures. Rectifying behaviour has been observed up to the temperature 500 C for 1 hr annealing. Pd Schottky will be a suitable material for high temperature applications.

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1. S. Arulkumar, T. Egawa, G. Zhao, H. Ishikawa, T. Jimbo and M. Umeno, *Jpn. J. Appl. Phys.*, 39 2000, L351-353.