

A Depth-2 Full-Adder Circuit using the InP RTD/HFET MOBILE

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Abstract:

Negative-differential resistance devices and circuit architectures based on the monostable-bistable transition logic element (MOBILE [1]) are promising candidates for future high-speed low-voltage digital systems. Recent progress in the manufacturability of Resonant Tunnelling Diodes (RTD) [e.g. 2] has initiated the design, layout, and technological realisation of more complex structures. In this contribution we will report on depth-2 full-adder circuit using the RTD/HFET MOBILE concept. The demonstrator circuit is a one-bit full adder on InP-substrate.

Design: Addition is the most frequently used operation in general purpose computing and application specific circuits for digital signal processing (e.g. digital filters). Therefore, the design of an efficient adder is essential for every emerging technology. To obtain a full adder function three digital signals $(a_i, b_i, c_{i-1}) \in \{0, 1\}$, that are the operands of bit position i (a_i, b_i) and the carry from the previous position c_{i-1} are added to compute the sum s_i and the carry c_i . In Fig. 1 a pipelined full adder circuit is presented. To exploit the properties of resonant tunnelling devices a threshold logic style has been chosen so that the addition is performed by:

$$\begin{aligned} c_i &= \text{sign}\{a_i + b_i + c_{i-1} - 2\}, & (1^{\text{st}} \text{ stage}) \\ s_i &= \text{sign}\{a_i + b_i + c_{i-1} - 2c_i - 1\} & (2^{\text{nd}} \text{ stage}) \end{aligned}$$

The arrangement of the adder in a depth-2 circuit composed of two gates is the most compact way to implement a full adder. The evaluation of the logic input signals is initiated by the rising clock edges of V_{CLK1} , and V_{CLK2} . To ensure a correct timing, i.e. the activation of the sum gate s_i after the carry c_i is valid, and to obtain a pipelining, a phase shift of two inverter delays between the rising clock edges is used. This corresponds to an overlapping multi-phase clocking scheme, which is implemented on chip by an SBFL-E/D HFET inverter chain.

Layout and Technology: The layout of the adders has been made with a minimum RTD area of $2 \mu\text{m}^2$ and HFET gate-length of $0,25 \mu\text{m}$. The compact realisation of the circuit is demonstrated using the detail of the basic building block (cf.

detail in Fig. 1) composed of a RTD and two HFET input terminals in Fig. 2. The RTD anode is connected to the supply voltage by means of a polyimide bridge. The cathode of the RTD and the out terminal of the building block are drain and source of a dual gate HFET where one gate is for the clock and the 2nd gate for the data. The supply voltage for this circuit is as low as $V_{DD} = 0.7 \text{ V}$.

Epitaxial layers are grown on s.i. InP:Fe substrate in a single MBE run such that the RTD layer is staggered on top of the HFET. Device fabrication is done using direct write e-beam lithography and all wet chemical etching. The device processing started with the evaporation of the RTD anode metal which also serves as a mask for the following etch step forming the RTD's. In a second etch step the HFET-mesas are defined while the RTD interconnection fingers are under-etched. After the evaporation and alloying of the HFET-source and drain contacts the depletion-type gates are fabricated. Polyimide is patterned for the following final metal step completing the connection of the circuit and forming the enhancement-type gates. The effective RTD anode area is less than $2 \mu\text{m}^2$ leading to a peak current of 0.40 mA per input stage. The extrinsic transconductance of the HFET is 510 mS/mm .

Evaluation and Comparison: The performance of the adder in terms of circuit delay, output rise times, and power dissipation, is evaluated using SPICE simulation (Table I). The operation of the circuit and has been verified for $f_{\text{clk}} = 1 \text{ GHz}$ considering all possible logic input combinations. Using an optimised clocking scheme and scaled devices with higher peak current density the clock frequency can be increased about 20 GHz .

- [1] K. Chen, K. Meazawa, M. Yamamoto: InP Based High Performance Monostable-Bistable Transition Logic Elements (MOBILE's) Using Integrated Multiple-Input Resonant-Tunnelling Devices, IEEE Electron Dev. Lett., Vol. 17, No. 3, March 1996, pp. 127-129.
- [2] W.Prost, U.Auer, F.-J.Tegude, C.Pacha, K.F.Goser, G.Janßen, T. van der Roer; Manufacturability and Robust Design of Nanoelectronic Logic Circuits based on Resonant Tunnelling Diodes, accepted J. Circuit Theory and Applications, Special Issue on Nanoelectronic Circuits, Vol 28.

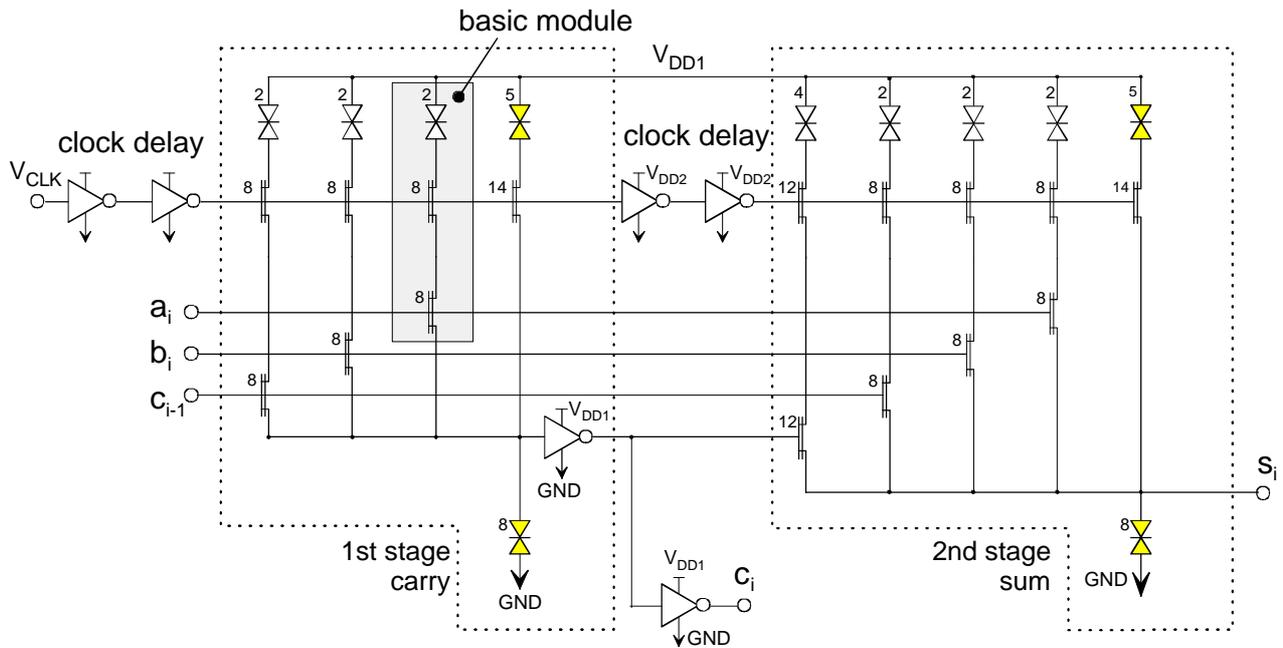


Fig. 1: Design of a Depth-2 One-bit Pipelined Threshold Logic Full Adder with local clock generation and delay by an E/D HFET Super-Buffer inverter chain. The "basic module" of a series connection of a RTD-HFET-HFET is given in detail in Fig. 2. The numbers at the devices indicate RTD area in $[\mu\text{m}^2]$ or HFET gate width $[\mu\text{m}]$.

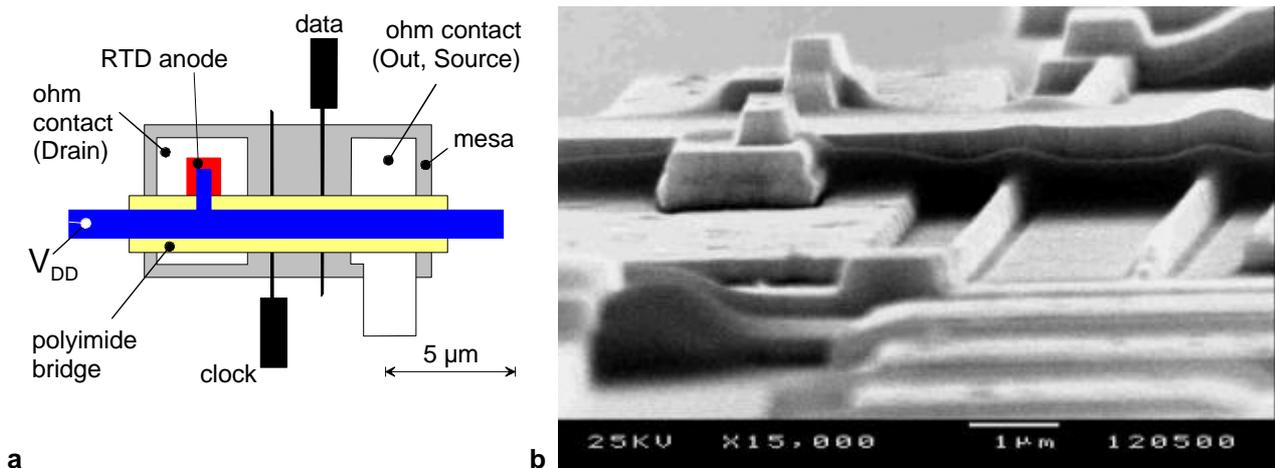


Fig. 2: Layout (a) and SEM micrograph (b) of a RTD-HFET-HFET input stage module of the threshold logic full adder composed of a self-aligned directly contacted RTD and $0,25 \mu\text{m}$ gate length HFET gates of the clock and input transistor. The V_{DD} -line is led on polyimide bridges over the gates

Table I: Simulated performance and specifications of the pipelined full adder ($V_{DD}=0.7\text{V}$ and $f_{CLK}=1 \text{ GHz}$)

Logic level:	high $V_H=0.63 \text{ V}$	low $V_L=0.08 \text{ V}$
Power dissipation:	Average $P_{ave}=725 \mu\text{W}$	Maximum $P_{max}=1.55 \text{ mW}$
Output rise times:	carry $t_r(c_i)=250 \text{ ps}$,	sum $t_r(s_i)=145 \text{ ps}$
Delay:	output $t_d(c_i)=144 \text{ ps}$, $t_d(s_i)=270 \text{ ps}$	Clock Phase $t_{CC}=145 \text{ ps}$
Circuit Area:	$65 \mu\text{m} \times 35 \mu\text{m}$	