Understanding the Degradation of InP/InGaAs Heterojunction Bipolar Transistors Induced by Silicon Nitride Passivation

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Deposition of silicon nitride (SiN) using plasma-based technology for passivating InP-based HBTs has been intensively studied in the last few years. However, the use of the SiN for InP/InGaAs HBT passivation still suffers from a number of limitations such as degradation of electrical performance, lack of reproducibility, etc.. Ouacha *et al* [1] has reported that the degradation of current gain could be associated with the increase in the surface recombination due to surface damage. However, Sachelarie *et al* [2] suggested that the crystal deformation due to shear stress produced by SiN may play an important role to decrease the current gain. A fundamental understanding of the root cause for the degradation of the electrical properties due to SiN passivation is still lacking. In this work, the effect of SiN passivation on the electrical characteristics of InP/InGaAs HBTs has been investigated comprehensively. The major degradations of I-V characteristics identified in our devices are: (1) the decrease of current gain due to a significant increase in the forward base leakage current and (2) large increase of base-collector (B-C) and base-emitter (B-E) reverse leakage currents. We have found that different physical origins should be attributed to these two degradation behaviors.

The devices used in this work were grown by GSMBE on semi-insulating (100) InP substrates and fabricated using a triple-mesa isolation process [3]. The SiN passivation study was carried out in a PLASMATHERM 790 system.

Fig.1 shows the current gain (β) versus collector current (I_C) for a device before and after SiN deposition. To lower the SiN induced stress, a very thin SiN layer (50 nm) was used. It can be seen that a significant degradation of current gain is induced for the passivated device. The drastic increase of β in the low current region is due to the B-C junction reverse leakage current. The shift of the drastic increase in β after passivation in this plot is due to a large increase in B-C leakage current. The increase in B-C leakage also affects the device output conductance and I_{CEO}, which can be seen in the common-emitter I-V characteristics (inset of Fig.1).

The degradation of β is mainly caused by a large increase of the base leakage current and its ideality factor (Fig.2). This is believed to be due to the preferential etching of phosphorous resulting in a very leaky indium rich surface, which can be illustrated by a Gummel plot obtained from a device after NH_3 plasma treatment at 300^{o}C for 30 second. (During the NH_3 plasma treatments, N_2 was used instead of SiH_4 and all other parameters were kept exactly the same as those for SiN deposition.) The NH_3 plasma treated device shows a similar increase of base leakage current with almost the same ideality factor as the one for SiN passivated HBTs. The loss of P atoms resulted by the preferential etching is shown in the inset of Fig.2. A rough surface can be observed in the InP region. EDX measurement also confirms a much higher indium composition in the InP region.

However, it seems that preferential etching does not induce very high B-C and B-E junction reverse leakage currents. Unlike SiN passivated HBTs, no obvious changes on output conductance and I_{CEO} are observed on the HBT after NH_3+N_2 plasma treatment (Fig.3). This may imply that the increase in B-C and B-E leakage due to SiN passivation cannot be directly linked to the surface damage caused by the preferential etching.

Fig.4 compares the B-C junction reverse leakage currents between the HBT passivated by SiN and the one treated with NH_3 plasma. The high reverse leakage current with less sensitivity on bias voltage suggests that the dominant mechanism for junction reverse current is related to the Shockley-Read-Hall (SRH) generation-related process [4]. A possible explanation could be the change of device surface potential due to the incorporation of fixed charges into SiN or at the InP/SiN interface during SiN deposition. This may affect the generation process at the surface. Further studies are being carried out to identify its physical origin.

In conclusions, the degradation of electrical characteristics of InP/InGaAs HBTs due to SiN passivation has been investigated comprehensively. Two major degradation behaviors are identified: (1)

decrease of the current gain due to a significant increase in the forward base leakage current and (2) large increase of B-C and B-E junction reverse leakage currents. It has been found that the increase of forward base leakage current can be attributed to the preferential etching of phosphorous during SiN deposition. However, experimental evidence indicates that the increase of junction reverse leakage current does not relate to the surface preferential etching. It is found that the dominating mechanism for the increase of junction reverse current may be related to the Shockley-Read-Hall (SRH) generation-related process. The understanding of physical origins for the degradation of electrical characteristics of InP/InGaAs HBTs induced by SiN passivation reported here is important for further optimization of the passivation process.

References:

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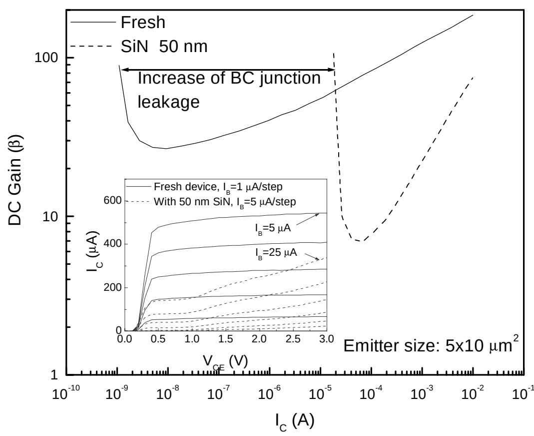

Fig.1 Current gain (β) versus collector current (I_C) for a device before and after SiN deposition. Inset: common-emitter I-V characteristics for the device before and after SiN passivation.

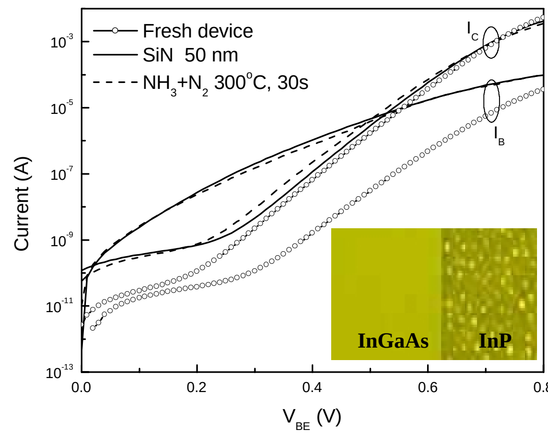

Fig.2 Effect of SiN passivation and NH_3 preferential etching on the Gummel plots for InP/InGaAs HBTs with 5×10 μm^2 emitter. Inset: Normarsky interference optical microscopy of InP/InGaAs surface after NH_3 preferential etching.

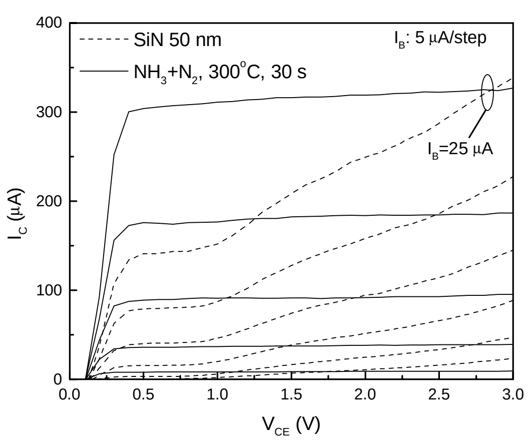

Fig.3 Comparison of common-emitter I-V characteristics for the InP/InGaAs HBTs after SiN (50 nm) passivation and NH_3 plasma treatment.

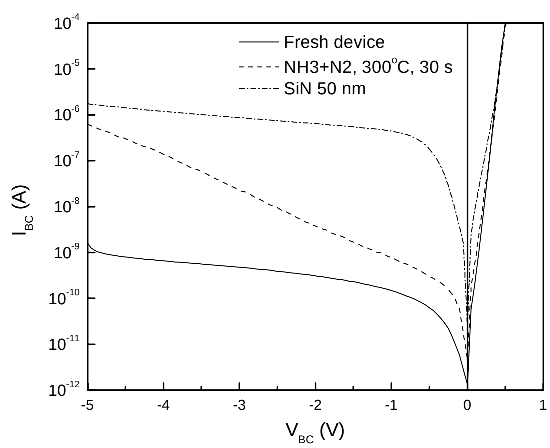

Fig.4 Comparison of B-C junction reverse leakage currents between the HBT passivated by SiN and the one with high loss of P due to preferential etching.