

A numerical analysis to study the effects of process related variations in the extrinsic base design on dc current gain of InAlAs/InGaAs/InP DHBTs

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Abstract

The 2-D simulation program DESSIS was used to simulate InAlAs/InGaAs/InP DHBTs and compare the calculated behavior with measurements from experimental devices employing the same structure. DHBTs generally display a peak in dc current gain, β , with collector current owing to high current-density effects in the intrinsic device [1]. Behavior of experimental devices is further complicated by process related variations in the extrinsic device; in our devices two of these variations arise from the placement of base contact, both laterally and vertically (Fig. 1). Lateral placement of base contact gives the distance W_{bl} between the base metal and emitter edges that can vary due to processing. Vertical placement into the base layer is relevant in device designs that incorporate a low-doped or un-doped spacer between the base and the emitter. While the aim is to place the contact on the base layer, process variations may leave a residual spacer layer, t_{sp} , between the base metal and base layer. Simulations reported here show that a combination of bulk recombination in the intrinsic device and lateral diffusion of minority carriers to the base contact, as depicted in the 2-dimensional current density plots in Fig. 2, limit the peak β of these DHBTs. These observations are consistent with the work of Lee [2] who discussed the effect of lateral placement of base contact, and of Ito [3] who reported the role of spacer layer in enhanced space charge recombination (SCR). Results in Figs. 3 and 4 show that the lateral diffusion of minority carriers, and hence β , is strongly related to both the lateral and vertical placement of base contact. Figure 3 is a plot of peak β and electron and hole components in the base as a function of emitter-edge to base-contact distance, W_{bl} . For W_{bl} as low as 200nm the lateral diffusion component of the base contact is essentially negligible and peak β is limited largely by bulk recombination. Conversely, for short W_{bl} of 20nm, which would be typical of self-aligned devices, lateral diffusion is the dominant part of base current and hence, is the main factor affecting peak β . Peak β of the experimental device is consistent with a base contact placement within 20nm-30nm from the emitter edge in the absence of a residual spacer layer ($t_{sp}=0$) in the extrinsic device. Figure 4 is a plot of peak β as a function of t_{sp} for different values of W_{bl} . Presence of a residual spacer layer, t_{sp} , in the extrinsic device is shown to accentuate the gain degradation through enhanced space charge recombination and lateral electron diffusion in the extrinsic device. This effect can be seen clearly in Fig.4 where the largest t_{sp} results in largest spreading of electron current in the extrinsic device. In conclusion, process related variations in the placement of base contact were shown to be strongly related to variations in β of InAlAs/InGaAs/InP DHBTs. Lateral placement of base contact affects the spreading of minority carriers in the extrinsic device and a residual spacer layer in the extrinsic device leads to enhanced diffusion of minority carriers to the base electrode and limits the peak β to low values.

References

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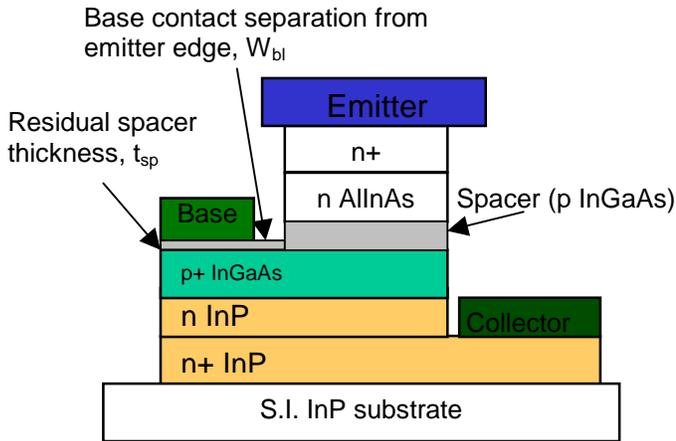


Figure 1 Schematic cross section of the DHBT

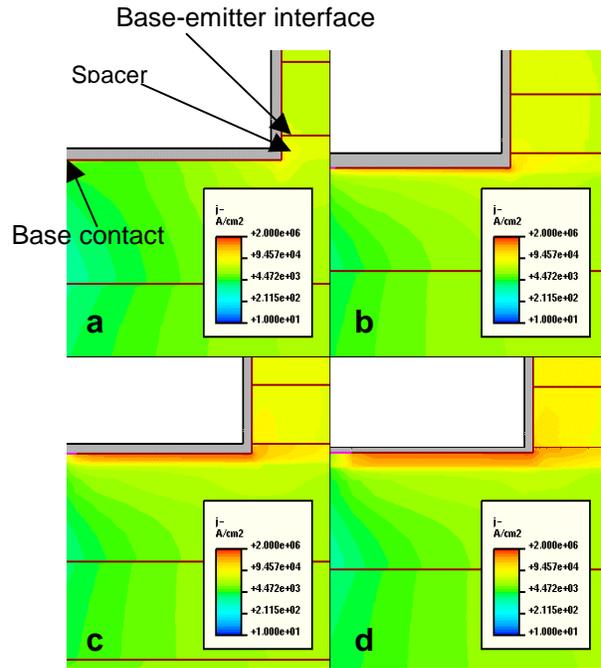


Figure 2 Electron current density in the extrinsic device for different residual spacer layer, t_{sp} , a) 0nm, b) 2.5nm, c) 5.0nm and d) 7.5nm

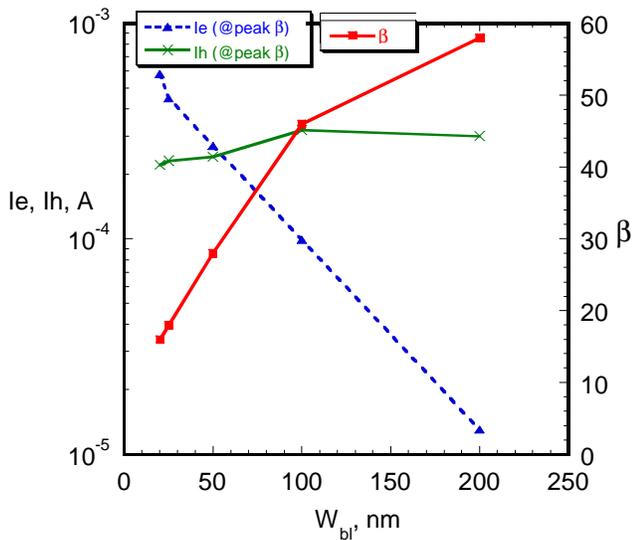


Figure 3 Variation in peak beta and corresponding hole and electron currents in the base terminal plotted as a function of base contact distance from the emitter edge (for $t_{sp}=0$).

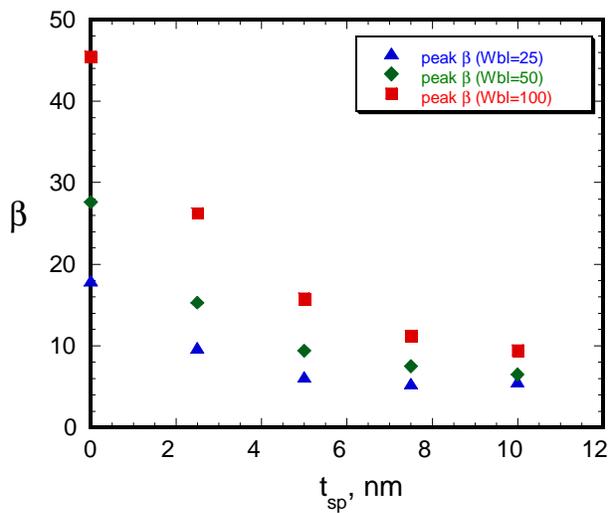


Figure 4 Peak dc current gain, β , plotted against residual spacer layer thickness in the extrinsic device, t_{sp} for different emitter to base contact separation, W_{bl} .