

0.1 μm Enhancement-Mode Pseudomorphic InGaAs/InAlAs/InP HEMT

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Abstract

We present state-of-the-art performance of 0.1 μm enhancement-mode (E-mode) pseudomorphic InGaAs/InAlAs/InP HEMTs. The HEMTs have a cutoff frequency of 210 GHz, transconductance of 1180 mS/mm, and less than 1 mA/mm I_{DSS} (drain current at a gate bias of zero volts), measured at a drain bias of 1V. The device characteristics make the E-mode HEMTs suitable candidates for ultra-high-speed digital and analog applications. Integration of the E-mode HEMTs with depletion-mode (D-mode) HEMTs allows simplified circuit configuration, smaller circuit area, and lower power dissipation, when compared to circuits designed with D-mode devices only.

InP HEMT epitaxial layer structures were grown by molecular beam epitaxy on 3-inch semi-insulating InP substrates. The structures were grown with electron channel density, n_s , varying from 1.5 to $3.5 \times 10^{12} \text{ cm}^{-2}$. The E-mode wafers were processed using the baseline TRW InP (D-mode) HEMT production process [1]. The E-mode HEMTs, however, required a lower drain current target at gate recess etch, and different gate metallization compared to the standard D-mode InP HEMTs. The E-mode HEMTs utilize a Pt/Ti/Pt/Au gate metal [2]. The devices and circuits are fully passivated with silicon nitride, and upon completion of frontside processing, wafers are thinned to a thickness of 75 μm . Table 1 shows the wafer average DC and RF device performance (22 sites per wafer) of the E-mode HEMTs with various n_s . Figure 1 shows the drain current and transconductance as a function of gate voltage for an E-mode HEMT with n_s of $3.5 \times 10^{12} \text{ cm}^{-2}$. The E-mode HEMT with n_s of $3.5 \times 10^{12} \text{ cm}^{-2}$ is best suited for high-speed applications due to the superior f_T compared to the HEMTs having lower n_s .

To date, nine 3-inch E-mode HEMT wafers with n_s of $3.5 \times 10^{12} \text{ cm}^{-2}$ have been fabricated over three separate 'pilot' fabrication runs in the InP production line at TRW in order to investigate the reproducibility. The E-mode HEMTs demonstrated tight wafer-to-wafer distribution of the device figures-of-merit as shown in Table 2. The distribution of device performance on each individual wafer was also tight; for example the typical standard deviation in pinchoff voltage over a 3-inch wafer was 35 mV. The results show reproducible device performance of E-mode HEMTs fabricated in the production environment. Low noise amplifier circuit performance will be shown which further demonstrates the reproducibility, and also high yield, of the E-mode HEMT process. The HEMT structure with n_s of $3.5 \times 10^{12} \text{ cm}^{-2}$ is the baseline TRW 0.1 μm D-mode HEMT structure, and therefore, integration of E-mode HEMTs with D-mode HEMTs on the same wafer in the production environment will be possible by simply performing two separate gate lithography and metallization steps.

References

- [1] R. Lai, M. Barsky, R. Grundbacher, L. Tran, T. Block, T.P. Chin, V. Medvedev, E. Sabin, H. Rogers, P. H. Liu, Y.C. Chen, R. Tsai and D. Streit, "0.1 μm InGaAs/InAlAs/InP HEMT Production Process for MMW Applications from 2-200 GHz," *Proceedings 1999 International Conference on Gallium-Arsenide Manufacturing Technology*, May 1999.
- [2] A. Mahajan, M. Arafa, P. Fay, C. Caneau, and I. Adesida, "0.3- μm Gate-Length Enhancement-Mode InAlAs/InGaAs/InP High-Electron Mobility Transistor," *IEEE Electron Device Lett.*, vol. 18, pp. 284-286, June 1997.

n_s (cm ⁻²)	Gm (mS/mm)	Idss (mA/mm)	f _T (GHz)
1.5x10 ¹²	720	0.3	140
2.5x10 ¹²	910	0.8	165
3.5x10 ¹²	1180	1	210

Table 1. E-mode HEMT transconductance (Gm), drain current at 0V gate bias (Idss), and cutoff frequency (f_T) as a function of electron sheet charge density in the channel (n_s). Each value represents a wafer average of 22 sites measured over the entire wafer. Measurements were made at drain bias of 1V.

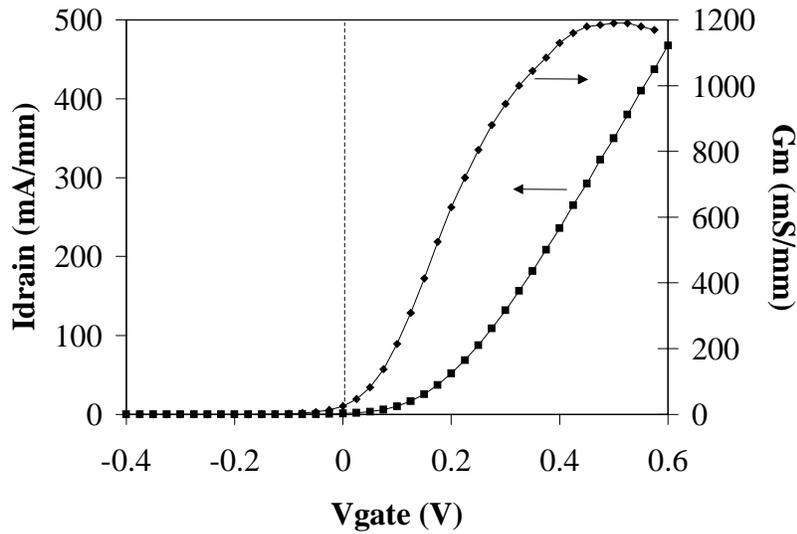


Figure 1. Drain current (Idrain) and transconductance (Gm) as a function of gate voltage of an enhancement-mode HEMT biased at a drain voltage of 1V.

Wafer number	Gm (mS/mm)	Idss (mA/mm)	f _T (GHz)
1	1096	2.4	200
2	1220	0.13	195
3	1196	0.65	195
4	1176	0.31	205
5	1180	1	210
6	1142	2	210
7	1290	6	205
8	1169	5.3	195
9	1148	1.8	190

Table 2. E-mode HEMT transconductance (Gm), drain current at 0V gate bias (Idss), and cutoff frequency (f_T) of nine 3-inch wafers fabricated over 3 different production runs. Each value represents a wafer average of 22 sites measured over the entire wafer. Measurements were made at drain bias of 1V.