

A Model for Hydrogen-Induced Piezoelectric Effect in InP HEMTs and GaAs PHEMTs

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Hydrogen degradation has been identified as a serious reliability concern in III-V FETs in general and InP HEMTs in particular [1]. In applications demanding hermetically-sealed packaging, such as satellite or fiber-optic systems, exposure occurs when H out-gasses from the packaging material and becomes trapped inside the package cavity. Eventually H diffuses into the transistor and alters the electrical characteristics of the FETs leading to parametric module failure.

Recent research has shown that H exposure results in the formation of TiH_x in Ti/Pt/Au gates [2]. This produces compressive stress in the gate, which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge causes a threshold voltage shift. Literature reports of the sign and magnitude of the V_T shift in InP HEMTs and GaAs PHEMTs seem contradictory. While all reports on [011]-oriented GaAs PHEMTs show a positive V_T shift [3], [011]-oriented InP HEMTs have been found to display positive [4], negative [3], and even negligible V_T shifts [5]. When all the data are graphed together, however, a compelling picture emerges (Fig. 1). It appears that for GaAs PHEMTs, ΔV_T is always positive and increases as the gate length is reduced. In contrast, for long gate length InP HEMTs, ΔV_T is negative and increasing in magnitude with decreasing L_g . At a certain L_g , however, there is a sign turn around and H-induced ΔV_T becomes positive.

In this work, we present a model for H-induced piezoelectric effect in InP HEMTs and GaAs PHEMTs that explains this peculiar behavior of ΔV_T and provides design guidelines for minimizing H sensitivity. Our modeling approach involves i) performing two-dimensional mechanical stress simulations in typical heterostructures, ii) computing the resulting piezoelectric charge, and iii) estimating its effect on V_T . Our results are consistent with the data of Fig. 1 and illuminate the key dependences of ΔV_T on heterostructure design. They also explain the fundamental difference between GaAs PHEMTs and InP HEMTs.

As a model device, we have selected a double heterostructure transistor with a 300 Å insulator layer and a 200 Å channel. First, a 2D finite-element simulation tool, ABAQUS, was used to calculate the mechanical stress in the device layer structure introduced by an expanding gate. This simulation yields the atomic displacements everywhere in the heterostructure (Fig. 2). Second, from the atomic displacements and using the piezoelectric constants of the various materials in the layer structure, the polarization vector field and the polarization charge distribution are computed throughout the device [6] (Fig. 3).

The final step is to compute the effect of the polarization charge on V_T . For simplicity, we assume a 1D model in which ΔV_T is calculated at the center of the gate. In this model, we assume that the Fermi level is pinned at the bottom of the buffer layer. The input to this calculation is P_z , the piezoelectric polarization normal to the surface. This is shown in Fig. 4 for 1 μm devices. Our model suggests that ΔV_T is proportional to the *difference* between the average of P_z above the channel and in the buffer layer. Because of this, the heterostructure design plays a key role, including the thickness of the buffer layer.

Figs. 5 and 6 show, respectively, calculations of ΔV_T for InP HEMTs and GaAs PHEMTs of different L_g and buffer thickness. For InP HEMTs it was found that long devices exhibit a negative V_T shift, while submicron devices show a positive V_T shift. This stems from the relative polarization constants of InAlAs and InGaAs that for the same stress yield a polarization in the channel that is much smaller than that in the buffer and insulator. As a result, for medium and long gate lengths when the stress in the vertical direction of the structure exhibits a fairly soft distribution in depth, the average polarization in the buffer layer is higher than that of the insulator/channel layer structure. In consequence, ΔV_T is negative. For short channel devices, the stress sharply peaks directly underneath the gate, and the polarization in the buffer becomes less relevant. ΔV_T becomes positive.

For a GaAs PHEMT, ΔV_T is found to always be positive, also in agreement with the data of Fig. 1. The reason for this is that for the same stress, the polarization in the InGaAs pseudomorphic channel is higher than in the AlGaAs barrier and insulator. In consequence, for most designs the average polarization in the buffer cannot exceed that of the insulator/channel composite.

This work not only explains the puzzling sign behavior of hydrogen-induced ΔV_T in InP HEMTs and GaAs PHEMTs but it provides a tool to help minimize the impact of hydrogen on FET characteristics. In InP HEMTs, in particular, our work suggests that it is possible to select a heterostructure design that is insensitive to hydrogen at a certain gate length.

[1] J. del Alamo et al., TWHM 2000. [2] R. Blanchard *et al.*, *Electr. Dev. Lett.*, 20, 8 (1999). [3] P. Chao et al., *IEEE Electr. Dev. Lett.*, 15, 5 (1994) [4] R. Blanchard et al. IPRM 2000. [5] M. Chertouk et al., *IEEE Electr. Dev. Lett.*, 21, 97 (2000). [6] P. Asbeck et al., *IEEE Trans. on Electron Dev.*, 31, 10 (1984).

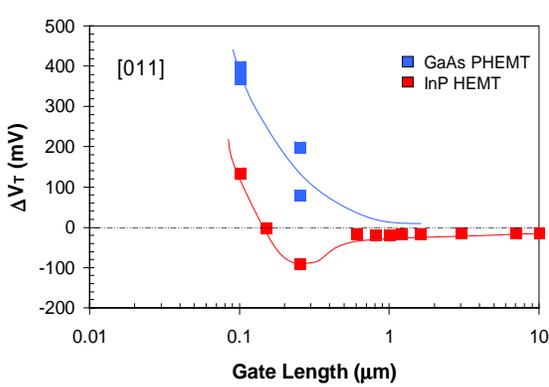


Fig. 1: Reported ΔV_T caused by hydrogen degradation as a function of gate length for InP HEMTs and GaAs PHEMTs [2-5].

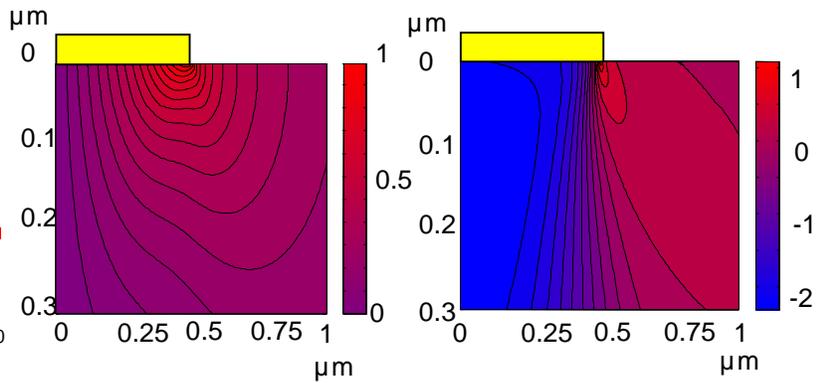


Fig. 2: Relative displacement parallel (left) and perpendicular (right) to the gate produced by an expanding gate in a 1 μm gate length HEMT. Calculations by ABAQUS. Only half of the structure is simulated.

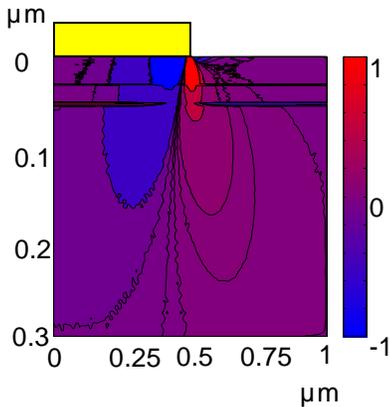


Fig. 3: Relative 2D piezoelectric charge distribution in a 1 μm HEMT stressed by an expanding gate.

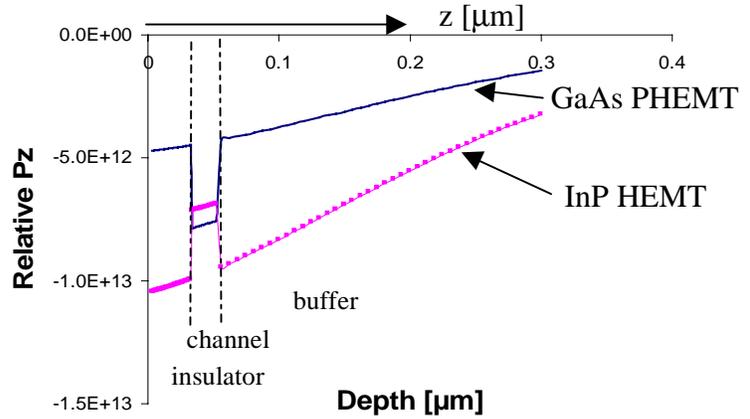


Fig. 4: Piezoelectric polarization vector in the direction perpendicular to the gate, P_z for an InP HEMT and a GaAs PHEMT with 1 μm gate length.

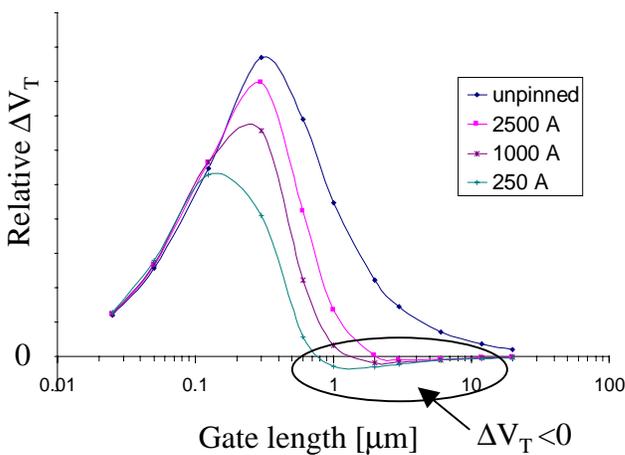


Fig. 5: Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths. The different lines are calculations for different buffer layer thickness, as well as for an unpinned buffer/substrate interface.

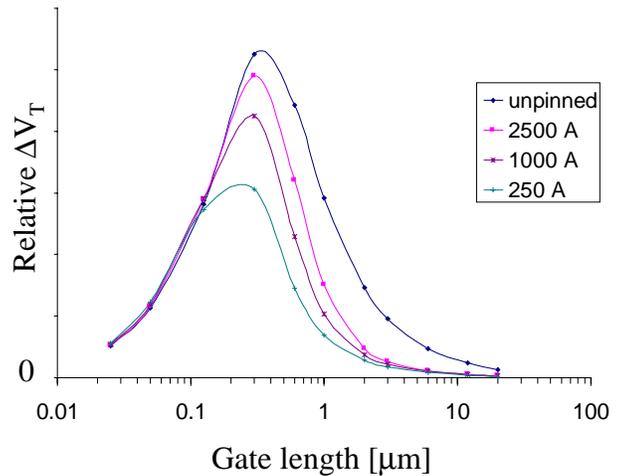


Fig. 6: Relative hydrogen-induced ΔV_T for GaAs PHEMTs of different gate lengths. The different lines are calculations for different buffer layer thickness, as well as for an unpinned buffer/substrate interface.