Novel RTA technique for large diameter GaAs wafers managing to minimize both dopant diffusion and slip formation

Takashi Sakurada, Makoto Kiyama, Shigeru Nakajima, Masami Tatsumi

5114

Sumitomo Electric industries, Ltd.

1-1-1, Koya-kita, Itami,Hyogo, 664-0016 Japan

Telephone : (0727) 72-4581, Fax: : (0727) 72-2440, E-mail : sakurada-takashi@sei.co.jp

In relation to device performance and fabrication cost of GaAs-related devices, there are two trends, one of which is devices with shallow channel, and another is fabrication on a large diameter wafer. Shallow and abrupt doping channel can be realized by means of low energy implantation with high dosage and rapid activation annealing to avoid dopant diffusion. RTA is useful for shallow channel devices, and has advantages not only in through-put but also in facility space compared to conventional furnace annealing, since the latter requires large area for large diameter wafers. The shallower the channel becomes, the more rapid sequence is needed. More rapid sequence of RTA may require direct irradiation of a wafer without the use of lid over susceptor, in which case the way of heating-up and cooling-down directly affects the uniformity of temperature within a wafer. Temperature distribution inevitably causes slip formation due to thermal stress, which is more serious in the case of large diameter wafers. The purpose of this work is to investigate a method to maintain the abrupt doping profile without slip generation during RTA.

$^{29}Si^{+}$ ions were implanted into 4 inch-ϕ S.I.-LEC wafers at the energy of 10 KeV with a dosage of 1.5e13cm^{-2}. After the implantation, wafers were encapsulated with 800Å-thick Si_3N_4 films and annealed using Heatpulse 8800 ; steag RTP systems. The condition of RTA was typically at 890℃ for 10 seconds in a flowing N_2 atmosphere. To eliminate slip formation, at first, we examined when slips generated by monitoring temperature distribution using a specially-prepared GaAs substrate, which was embedded with thermocouples at the center and peripheries on the surface. We found that slips generated mostly in the cooling process because power supply to the lamp was cut during cooling-down in order to realize high cooling rate and the peripheries were more easy to cool down than the center (Fig.1(a)). Thus, a short period step was inserted around 750℃ in the cooling sequence, and temperature differences between the center and periphery ($|T(0)-T(R)|$) was controlled smaller than the critical temperature difference (ΔTc) [1)] throughout the process (Fig.1(b)). The step should be short enough to maintain the doping profile steep. In the sequence with a step, residual strain measured using a scanning infrared polariscope was smaller and slip didn't generate, furthermore doping profile measured by SIMS was almost the same as the without-step case, as shown in Fig.2 and Fig.3.

In conclusion, in order to optimize a RTA sequence, we investigated when slip generated by monitoring temperature distribution within a wafers, and found that slip generated usually in the cooling process and newly sequence with a short step is effective in maintaining the abrupt doping profiles without slip formation.

1) : Kiyama et al., in Proc. 23rd Int. Symp. on Compound Semiconductors, St. Petersburg, Russia, 1996 (IOP Publishing, 1997) P 945

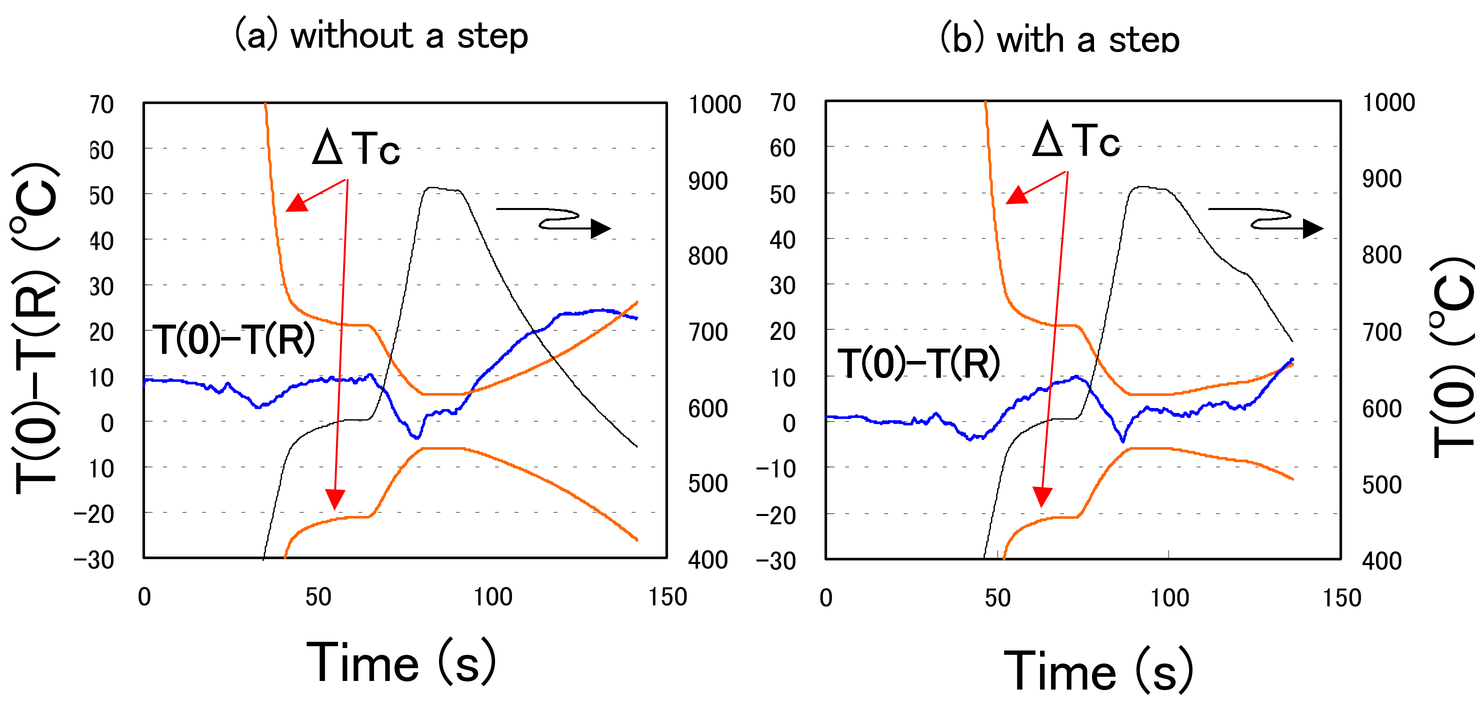

Fig.1. Temperature difference between the center : (T0) and periphery : T(R) of the wafer, and RTA Sequence.

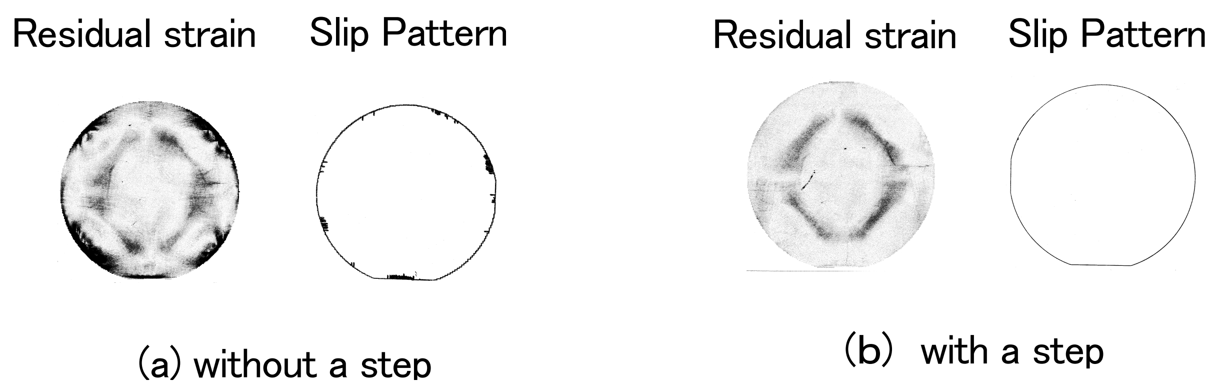

Fig.2. Residual strain and Slip pattern after RTA.

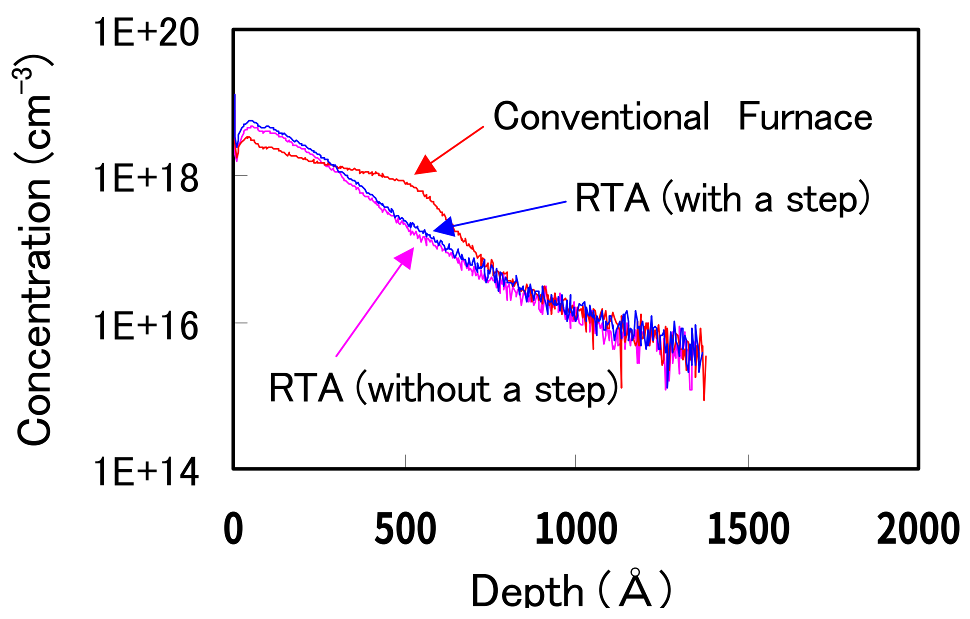

Fig.3 .^{29}Si Profile (SIMS)