

Isolation degradation of InAlAs/InGaAs/InP HEMTs due to bias stress depending on passivation films formed by PCVD

H. Moriguchi, S. Hoshi, T. Ohshima, T. Izumi, M. Tsunotani and T. Kimura

*III-V Devices Department, Components Division, Oki Electric Industry
550-1 Higashiasakawa, Hachioji, Tokyo 193-8550, Japan*

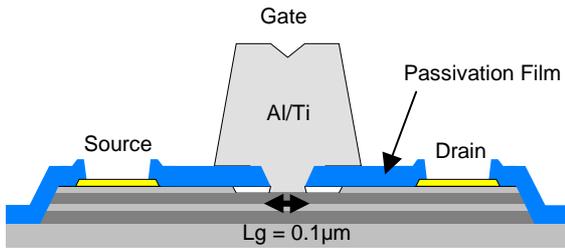
Phone: +81-426-62-6669, Fax: +81-426-62-6616, E-mail: moriguti324@oki.co.jp

An improvement of reliability is one of the most important issues in InP-based HEMTs. We have observed the degradation of pinch-off characteristics of InAlAs/InGaAs HEMTs after the bias stress test, which was resulted from an increase of the leakage current on semi-insulating InP substrate. A stability of the isolation characteristics for InP substrates was strongly affected by the surface passivation films formed by plasma-enhanced chemical vapor deposition (PCVD).

Figure 1 shows a cross-section of the lattice-matched $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ HEMT used in this study. All the layers were grown on a Fe-doped semi-insulating InP substrate with a resistivity of $3 \times 10^7 \Omega\text{cm}$. The device isolation was achieved by mesa etching down to InP substrate using H_3PO_4 based wet-chemical etching. After the Au-based ohmic electrodes were deposited on InGaAs cap layer, 100 nm thick SiN or SiO_2 passivation film was formed by PCVD at 250 °C. The mixture of $\text{SiH}_4/\text{NH}_3/\text{N}_2$ and $\text{SiH}_4/\text{N}_2\text{O}/\text{N}_2$ were used for the deposition of SiN and SiO_2 , respectively. Next, the 0.1 μm gate opening was fabricated by electron beam lithography and reactive ion etching. Then the selective wet recess etching was performed and the 0.1 μm T-shaped gate electrodes were formed. Typical device performance of those devices was the transconductance (g_m) of 900 mS/mm and the current gain cut-off frequency (f_T) of 215 GHz.

In order to investigate the stability of the device performance, high-temperature bias stress tests were performed at 200 °C with a drain voltage (V_{ds}) of 2 V and a gate voltage (V_{gs}) of 0 V. Figure 2 shows the $I_{ds}^{1/2}$ vs. V_{gs} plots before and after the stress test for the devices with SiN and SiO_2 passivation films. As shown in the figure, it was found that the pinch-off characteristics of the device with SiN remarkably degraded after the stress test, while the change was negligibly small for the device with SiO_2 . Figure 3 shows the change of the sub-threshold current (I_{th}) during the stress test. The I_{th} was defined as a drain current at the threshold voltage (V_{th}), which measured by extrapolating the $I_{ds}^{1/2}$ vs. V_{gs} plot. As shown in Fig. 3, the I_{th} for the device with SiN drastically increased during the stress test. Because the difference of those devices was only the passivation film which cover the InP substrate under the mesa region, we have attempted to investigate stability of the isolation characteristics of passivated semi-insulating InP substrates. The test was performed at 200 °C using the two ohmic electrodes of 80 μm wide separated by 2 μm gap on the semi-insulating InP substrate at the apply voltage of 10 V. Figure 4 shows the change of the leakage current of InP substrates with SiN and SiO_2 passivation films during the test. As shown in Fig. 4, it was found that the isolation characteristic of InP with SiN passivation film was drastically degraded by the stress, and the leakage current increased beyond 1 mA within 20 hours, which is 5 times larger than the initial value. On the other hand, the isolation characteristic of InP with SiO_2 was quite stable during the stress test. This result clearly shows that the degradation of pinch-off characteristics for the InAlAs/InGaAs HEMT with SiN passivation film after the stress test was caused by the increase of the leakage current between the contact pads formed on a semi-insulating InP substrate. In order to investigate the difference between the interfaces of SiN/InP and SiO_2 /InP, the surface morphologies over the films were measured. Figure 5 shows the surface roughness of SiN/InP and SiO_2 /InP measured by surface profiler. As shown in the figure, it was found that the surface of SiN/InP was rough compared with that of SiO_2 /InP. During the deposition of passivation films by PCVD, InP surface under the mesa region is exposed to the source gases. Because NH_3 plasma using for the deposition of SiN attacks the InP, the degradation of surface morphology occurs due to the phosphorus desorption. The loss of stoichiometry at the SiN/InP interface is believed to result in the instability of the isolation characteristics of InP.

It was found that the stability of the isolation characteristics of passivated semi-insulating InP substrates were strongly affected by the passivation films deposited by PCVD. Suppressing the isolation degradation of InP substrates is important to improve the reliability of InAlAs/InGaAs/InP HEMTs.



Cap Layer	InGaAs	20nm	$1 \times 10^{19} \text{cm}^{-3}$
Schottky Layer	InAlAs	15nm	
Donor Layer	InAlAs	9nm	$4 \times 10^{18} \text{cm}^{-3}$
Spacer Layer	InAlAs	2nm	
Channel Layer	InGaAs	15nm	
Buffer Layer	InAlAs	250nm	
Substrate	InP		

Fig.1 Cross section of InAlAs/InGaAs/InP HEMT

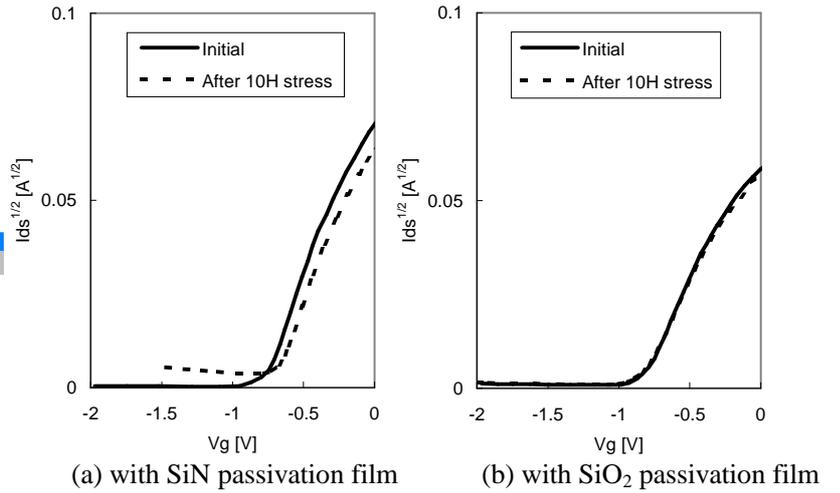


Fig.2 Change of I-V characteristics before and after the stress.

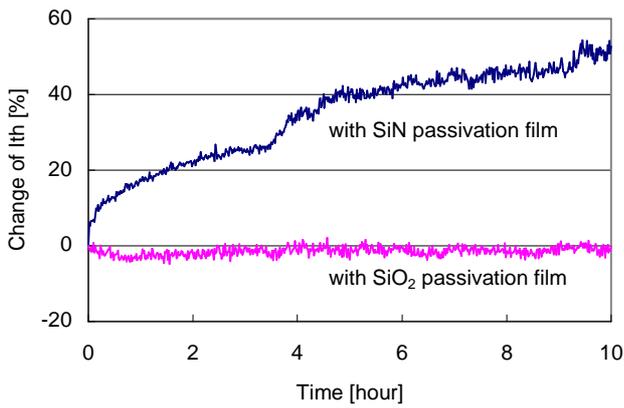


Fig.3 Change of the sub-threshold current (I_{th}) during stress test.

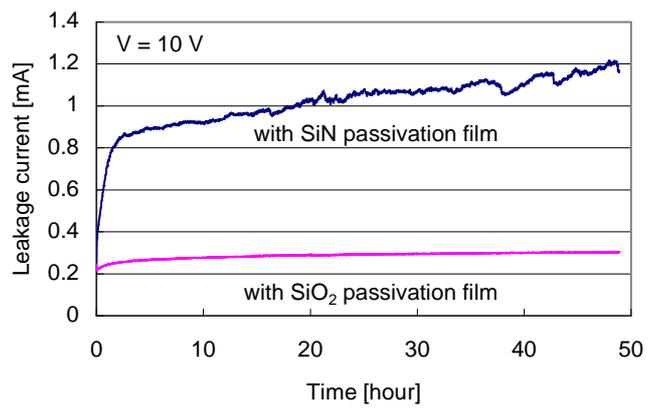
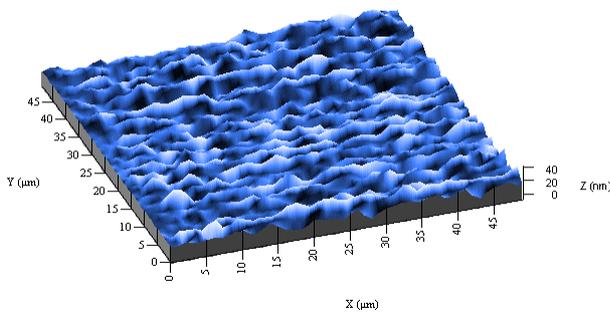
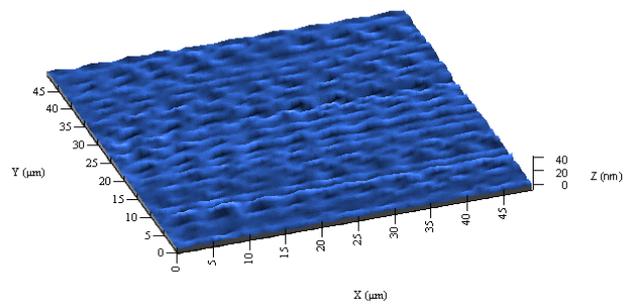


Fig.4 Change of leakage current for InP substrate at 200 °C.



(a) SiN passivation film on InP



(b) SiO₂ passivation film on InP

Fig.5 Roughness of the passivated surface