

Optimization of Novel Oxide-Free Insulated Gate Structure for InP Having An Ultrathin Silicon Interface Control Layer

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Abstract

Attempts were made to clarify the cause for the poor reproducibility of successful processing accompanied with a low the transconductance in the previous oxide-free InP MISFET having an ultrathin Si interface control layer(Si ICL). A detailed in-situ XPS study made for each step of processing indicated that deficiency of P on the InP surface took place by the irradiation of high energy Si beam during the growth of Si ICL. Then, a modified passivation structure having an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer was proposed and investigated. In-situ XPS study indicated that the novel gate structure prevents desorption of P from the InP surface. In-situ contactless C-V method showed a low and wide interface state density distribution with a minimum of $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. A long-gate InP MISFET test device with a gate length of $2 \mu\text{m}$ exhibited a maximum g_m of 123 mS/mm and a high drain current of 389 mA/mm.