High Performance, High Yield InP DHBT Production Process for 40 Gbps Applications

D. Sawdai, E. Kaneshiro, A. Gutierrez-Aitken, P.C. Grossman, K. Sato,
W. Kim, G. Leslie, J. Eldredge, T. Block, P. Chin, L. Tran, A. K. Oki, D.C. Streit

TRW Inc, Space & Electronics Group, D1/1302, One Space Park
Redondo Beach, CA 90278

ABSTRACT

High speed digital logic is essential in diverse applications such as optical communication, frequency synthesizers, and analog-digital conversion. Current research efforts indicate that technologies utilizing heterojunction bipolar transistors (HBTs) are the preferred approach for systems operating at clock frequencies of 40 GHz and above. This need for higher performance electronics for space and defense applications has driven the development of InP HBTs at TRW. Consistent and continuous improvements from the baseline MBE structure and process technology have enhanced frequency performance, breakdown voltage, producibility, yield, and device reliability such that InP HBTs are being successfully used for many commercial, space, and defense applications (1,2). This paper describes our optimized high-yield production InP DHBT process which simultaneously combines high f_T, high f_{max}, and high breakdown voltage.

The DHBT structure is grown in a solid-source molecular beam epitaxy (MBE) system equipped with a valved phosphorus cracker (3). The structure is grown on a semi-insulating InP substrate and consists of an *n*+ InP sub-collector, a 3000-Å *n*- InP collector, a linearly graded *n*- InGaAlAs layer at the collector-base interface to minimize the current blocking due to the InGaAs/InP conduction band discontinuity, a 400-Å 4×10^{19}-cm^{-3} *p*+ InGaAlAs graded base, an *n* InAlAs Emitter, and an *n*+ InGaAs cap layer. The collector layer structure was optimized for high speed and improved breakdown voltage. The InP HBT frontside process is very similar to TRW's flight-qualified one-micron GaAs HBT process (4), with minor metal and etch chemistry differences, and has essentially the same high yield. Process highlights include wet-etched mesas, a self-aligned base metal, silicon nitride passivation, integrated Schottky diodes, 100Ω/❑ or 20Ω/❑ NiCr thin-film resistors, MIM capacitors, and two layers of gold interconnect metal with airbridge crossovers. Our robust high-yield backside process includes thinning, dry-etched vias, and plated backside gold. Figure 1 shows the cross-section of our InP HBT IC technology.

InP DHBTs with $1.5\times10\ \mu m^2$ emitters from this technology demonstrate β ~ 100, J_{Cmax} ~ 150 kA/cm^2, and BV_{CBO} (at 1 μA) ~ 7 V. A typical forward common-emitter I-V plot is shown in Figure 2. Peak f_T and f_{max} are 172 and 197 GHz, respectively, at I_C = 24 mA and V_{CB} = 0.75 V (Figure 3). This process also offers high circuit yield of fully functional MMICs on each wafer: >80% for circuits with 1000 HBTs and ~ 60% for circuits with 4000 HBTs. Line yields are ~ 95%, as shown in Figure 4. This combination of performance characteristics, voltage breakdown, and yield enable the production of chip sets for the next generation 40 Gbps optical communications systems.

Bibliography

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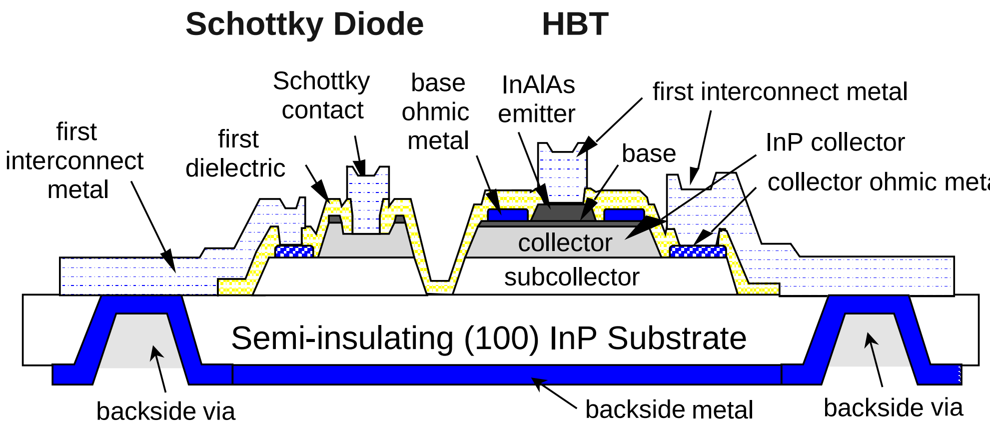

Figure 1. InP HBT device and IC technology

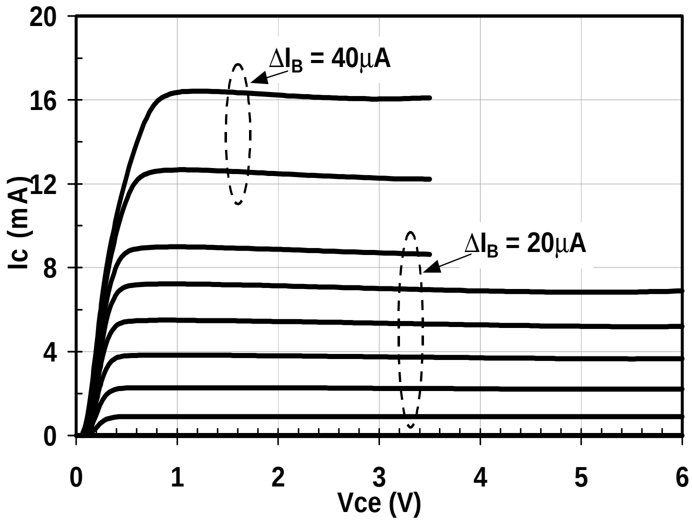

Figure 2: Common-emitter I-V of $1.5{\times}10\mu m^2$ DHBT.

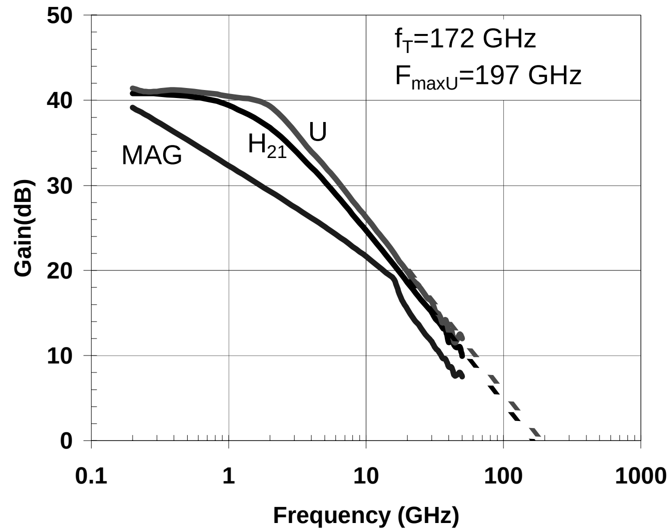

Figure 3: Frequency performance of $1.5{\times}10\mu m^2$ DHBT at I_C = 24 mA and V_{CB} = 0.75 V.

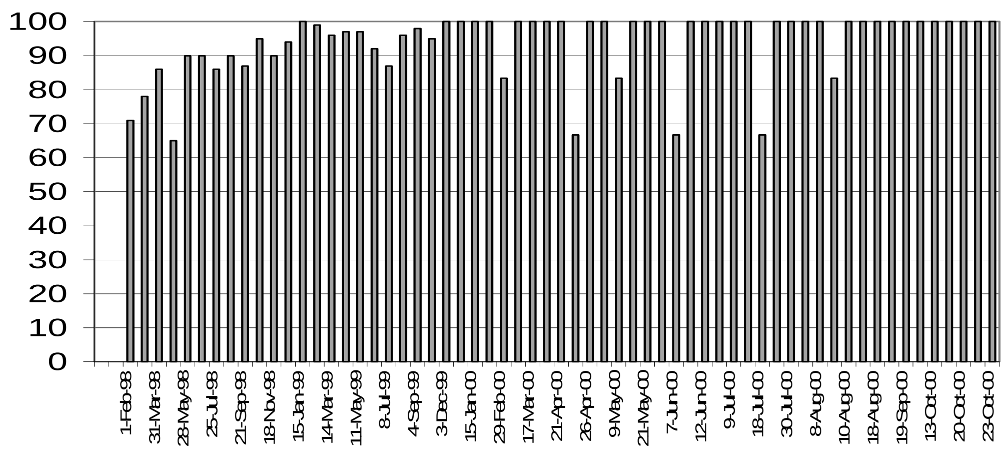

Figure 4. InP HBT wafer line yield over a period of approximately 2 years. Note the high yield (~95% average) after process optimization in early 1999.