

## Submicron Buried Metal-Heterojunction Bipolar Transistors - Fabrication and $C_{BC}$ dependence on buried growth conditions -

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Buried metal-heterojunction bipolar transistors with 0.5  $\mu\text{m}$  wide emitters were fabricated by using electron beam lithography. Three tungsten wires with 100 nm width, 100 nm height and 200 nm periods buried in InP had a function of a collector electrode. Total base-collector capacitances were estimated from measured RF characteristics and dependence on the buried growth temperature was observed.

In HBTs, size reduction of emitter is significantly effective for high-speed operation when extrinsic base-collector capacitance can be reduced [1,2]. We reported the reduction of total base-collector capacitance ( $C_{BC}$ ) by buried metal heterojunction bipolar transistors (BM-HBT), in which conventional sub-collector layer was replaced by tungsten wires in semiconductor, when emitter width was 2  $\mu\text{m}$  [2]. However, reduction of extrinsic  $C_{BC}$  is more effective when emitter width is finer.

In this report, we describe fabrication of submicron BM-HBT by using fabrication process with electron beam lithography [3]. We observed DC and RF performance of the devices with 0.5  $\mu\text{m}$  wide emitter. Calculated  $C_{BC}$  from RF measurement shows dependence on the buried growth conditions.

In the past fabrication process [2], collector resistance was high due to high resistivity and thin thickness of tungsten wires. Thus we changed fabrication process of tungsten film from evaporation to sputtering and the thickness was increased from 40 nm to 100 nm. As a result, sheet resistance of tungsten wires became 5.8  $\Omega/\square$ , that is fifth-fold reduction from the reported one. Fine wires were formed by  $\text{CF}_4$  reactive ion etching (RIE) from tungsten films. We inserted 10 nm-thick GaInAs layer between semi-insulating substrate and tungsten film to prevent RIE damage of the substrate. The GaInAs layer was etched off just after RIE. Figure 1 shows SEM picture of the tungsten wires with 100 nm height, 100 nm width and 200 nm period on InP substrate. Rectangle tungsten wires on flat InP surface were observed. Then the tungsten wires were buried in a 300 nm-thick InP layer by metalorganic vapor phase epitaxy. The buried growth temperature was 585°C. By successive growth, a 60 nm-thick GaInAs collector layer, a 50 nm-thick GaInAs base layer, a 50 nm-thick InP emitter layer and a 50 nm-thick GaInAs emitter-cap layer were formed. Cross-sectional SEM view around buried tungsten was shown in Fig.2. Flat hetero-interface was observed above the wires. The thickness of the buried InP layer on wires was 200 nm. After the growth, emitter electrode, emitter mesa, base electrode and base mesa were formed. When base mesa was formed, we exposed the buried tungsten wires and made a collector electrode on the wires. Figure 3 shows SEM picture of the device with 0.5  $\mu\text{m}$  wide emitter when the collector electrode was formed on the wires. We could confirm the alignment between wires and the emitter from the position of exposed wires. Interconnection by air-bridge structure and formation of insulating BCB layer were followed, finally.

Figure 4 shows common emitter I-V characteristics of the device with 0.5 $\times$ 2.5  $\mu\text{m}^2$  emitter area. In this device, three wires was used as collector electrode. Current gain was about 48 when collector current was 1.2 mA and collector voltage was 5 V. Observed RF characteristics are shown in Fig. 5. Observed cutoff frequency was 86 GHz when emitter current was 3.5 mA and collector voltage was 5 V. In the range of observed frequencies, U did not show the dependence of 20dB/oct. Estimated  $f_{MAX}$  from the gain at 30 GHz was 135 GHz. Figure 6 shows total  $C_{BC}$  calculated from observed  $Y_{12}$  in the devices with 0.5 $\times$ 2.5  $\mu\text{m}^2$  emitter area and 0.7 $\times$ 3.5  $\mu\text{m}^2$  emitter. Differences from theoretical total  $C_{BC}$  calculated by physical dimensions were less than 1 fF. Total  $C_{BC}$  from the devices when the buried growth temperature was 600°C were also shown in the figure. The difference from theoretical one is around 3 fF. Difference between two samples with different buried growth temperature can be explained by conductive grown interfaces around tungsten wires. To explain the difference of 3 fF, estimated width of conductive region around the wires was about 1.0  $\mu\text{m}$  as shown in the figure. Although the difference at 585°C can be explained by the conductive region with 0.25  $\mu\text{m}$  width, more precise measurement is necessary because the difference was close to the our measurement error. For higher speed, reduction of extrinsic resistance by modification of the interconnection is essential as the next step.

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