75 GHz ECL Static Frequency Divider in InAlAs/InGaAs Transferred Substrate HBT Technology.

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We report 75 GHz static frequency dividers in InAlAs/InGaAs transferred substrate HBT technology. This is the highest reported frequency of operation for a static frequency divider. The circuit has 60 transistors, and dissipates 800 mW. The circuit, shown in Fig. 1, is similar to the 66 GHz static frequency divider reported by Q. Lee *et al* [1] in the same technology. The improved performance over 66 GHz is due to improved base resistance, reduction in transistor and IC layout parasitics, and modification in layout to enable access to clock inputs using microwave wafer probes having waveguide rather than co-axial inputs. The output waveform measured at a 75 GHz clock input is shown in Fig. 3.

The maximum clock rate of operation of static frequency dividers have been used to benchmark the speed of an IC logic technology. SiGe bipolar technology and InP HBT technology have demonstrated static frequency dividers with clock rates well over 40 GHz [2,3]. Transferred substrate HBT technology has demonstrated excellent RF performance with 300 GHz f_t [4] and 800 GHz f_{max} [5]. This process [5] follows most of the mesa HBT processing steps, including emitter and base mesa isolation, contact metallization, polyimide device passivation, and interconnect metallization. After these steps benzocyclobutene (BCB) is spun on, and gold plating is carried out. The InP wafer is then flipped and bonded to a GaAs carrier wafer and the InP substrate in etched away to expose the collector layer. Collector definition and metallization completes the process. A key component of gate delay, C_{cb} x $(\Delta V_{logic}/ I)$ is minimized through the small collector junction area associated with transferred substrate HBTs. Further, the thin 2 kÅ fully depleted collector permits the HBTs to operate in this divider at 1.8 x 10^5 A/cm^2 current density without base push out.

The MBE layer structure is similar to that in [1], with key parameters being a 400 Å base at 4.0 x 10^{19} cm^{-3} doping and 52 meV band gap grading. The collector is 2.0 kÅ thick and doped at 1.0 x 10^{16} cm^{-3}. RF measurements (Fig. 3) on a 6.0 x 1.0 μm^2 emitter and 7.0 x 2.0 μm^2 collector yielded a f_t = 165 GHz, and f_{max} = 220 GHz, at J_e = 1 x 10^5 A/cm^2 and Vce = 1.0V. This is shown in Fig. 3. Divider measurements used a 2 – 26 GHz frequency synthesizer to drive a 2:1 frequency doubler producing outputs in the 26 – 40 GHz frequency range. For 50 – 75 GHz measurements, the 2 – 26 GHz synthesizer directly drives a 3:1 frequency tripler with the output delivered on-wafer with a V-band waveguide coplanar probe. Here the available signal power is + 2.0 to + 6.0 dBm over the band, including probe losses. The IC was also tested in the W band (75 – 110 GHz) through use of a cascaded frequency doubler and frequency tripler and a W band waveguide-coupled probe. Here, unfortunately, the available multiplier output power (-1.0 dBm to + 2.0dBm, including probe losses) was insufficient for IC operation. The divider operated at all the tested frequencies from 5.0 to 75.0 GHz, (Fig. 3 – Fig. 5). The static divide-by-2 output at 75 GHz shows a 6.0 GHz modulation due to a 6.0 GHz subharmonic (Fig. 6) present in the 2.0 – 26.0 GHz frequency synthesizer output.

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