

Poster Session VI

Comparison of 4H SiC pn, Pinch and Schottky Diodes for the 3 kV Range

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Nanoscale Electrical Characterization of 3C-SiC Layers by Conductive Atomic Force Microscopy

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A JBS Diode with Surge Current Capability and Controlled forward Temperature Coefficient

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Electronic Structure of the UD3 Defect in 4H and 6H SiC

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Homoepitaxial Growth of 4H-SiC Thin Film below 1000°C by Microwave Plasma Chemical Vapor Deposition

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X-ray Photoelectron Spectroscopy Studies of Post Oxidation Process Effects on Oxide/SiC Interfaces

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Replication of Defect from 4H-SiC Wafer to Epitaxial Layer

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Homoepitaxial Growth of Cubic Silicon Carbide by Sublimation Epitaxy

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Electron-irradiation-induced Amorphization in 6H-SiC by 300 keV Transmission Electron Microscopy Equipped with a Field-emission Gun

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A Simple Mapping Method of Elementary Screw Dislocations in Low-Doped Hexagonal SiC Epitaxial Layers

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The Investigations of 4H-SiC/SiO₂ Interfaces by Optical and Electrical Measurements

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Growth and Characterization of Three-Dimensional SiC Nanostructures on Si

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Characterization of 2 inch as Grown SiC Bulk by SWBXT at SPring-8

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The Neutral Silicon Vacancy in SiC: Ligand Hyperfine Interaction

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Growth of AlN Films by Hot-Wall CVD and Sublimation Techniques: Effect of Growth Cell Pressure

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A Method of Reducing Micropipe Using Metal Mask by the Sublimation Growth

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Atomic Steps Observation on 6H and 15R-SiC Polished Surface

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CVD SiC Powder for High Purity SiC Source Material

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PLD BN as an Annealing Cap for Ion Implanted SiC

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Growth Characteristics of SiC in a Hot-Wall CVD Reactor with Rotation

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On Shallow Interface States in n-Type 4H-SiC Metal-Oxide-Semiconductor Structures

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The Effect of CVD Growth on Warp of SiC Wafers

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Infrared Investigation of Implantation Damage in 6H-SiC

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TCAD Optimisation of 4H-SiC Channel Doped MOSFET with p-Polysilicon Gate

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Theory of Super-Junction Structure forward Characteristics in Comparison of 4H-SiC and Si

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Comparison of 4H SiC pn, Pinch and Schottky Diodes for the 3 kV Range

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This paper investigates the static and dynamic performance of 4H SiC pn, pinch and Schottky diodes designed for 3 kV, with identical active area (1.0 mm²) and prepared on the same wafer in order to reduce technological fluctuations. The p⁺ emitters are Al implanted (2x10¹⁹ cm⁻³) covering the full anode area in case of the pn diode whereas patterned in 4.5 μm p⁺ squares of equal distance for the pinch diode (see Fig. 1). The grid area in between these p⁺ squares forms a Schottky contact (ideality 1.05). Both kinds of contacts are simply prepared with the same contact material. The Schottky diodes are equipped with or without a surrounding p⁺-ring covering 20% of the anode area, respectively.

Results: All diode types block 3 kV (Fig. 2). The Schottky diodes exhibit the highest leakage current, the pn diodes the lowest. The pinch diodes are situated in between since the p regions reduce the field strength at the Schottky contact. Avalanche breakdown occurs at 3.7 kV but is overlapped by the higher leakage through the Schottky barrier in case of pinch and Schottky diodes. In context with the reverse and forward characteristics (Fig. 3) the pinch diode turns out to be the best choice:

- In normal operation (forward current I_F ≤ 2 A) its voltage drop is less than that of the pn diode, similar to the Schottky diode and comparable to ultrafast silicon diodes. The voltage drop is hardly effected by the reduced Schottky area.
- The progressive IV characteristics even at high currents (I_F >2A) improve the pinch diode's inrush current stability. Please note the contrast to the (normal) Schottky diode without any p⁺ region.
- Turn-on and turn-off experiments show the dynamic behavior to be Schottky like with very little influence of the storage charge and a recovery time of 30 ns.

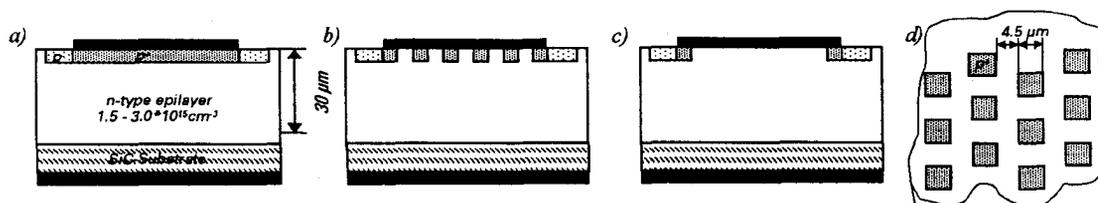


Fig. 1: Cross section of a) pn, b) pinch c) Schottky diode and d) pinch diode cell layout.

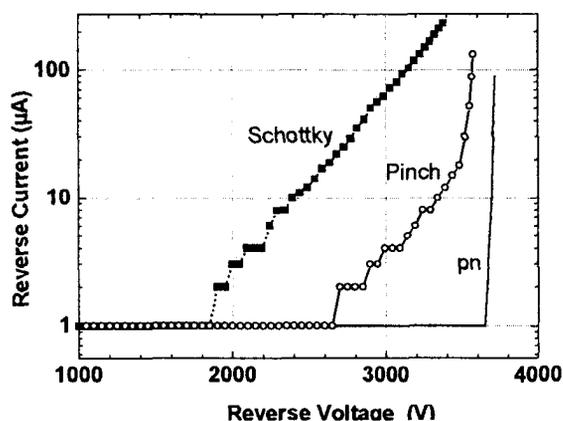


Fig. 2: Typical reverse characteristics

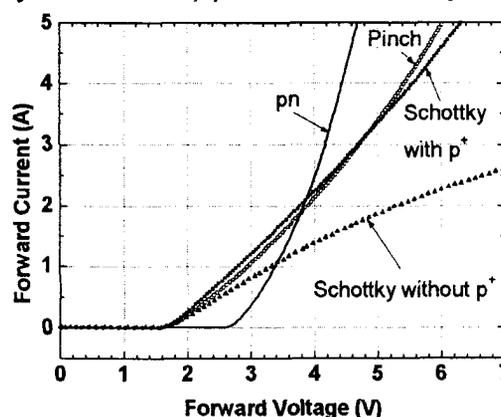


Fig. 3: Typical forward characteristics

Nanoscale Electrical Characterization of 3C-SiC Layers by Conductive Atomic Force Microscopy

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Although a great deal of work has been done on 3C-SiC epitaxial growth, high voltage device fabrication has yet to be successfully performed. We fabricated Schottky diodes on n/n+ 3C-SiC layers grown on undulated (100) Si substrates, but obtained ohmic I - V characteristics. To understand the mechanism, we simultaneously carried out topography and conductivity measurement on the 3C-SiC films by using conductive atomic force microscopy (C-AFM).

The C-AFM measurements were carried out in the contact mode with a Au-coated Si_3N_4 probe, where the conductive probe serves as a nanoscale electrode. The current measurement was carried out with a forward bias of the Schottky junction applied across the sample and the probe; therefore the current image reflects the local conductivity distribution and the Schottky barrier information. Examples of simultaneously obtained topography and current images are shown in Fig. 1(a) and (b), respectively. The sample is forwardly biased at -2.2 V. The AFM topography (a) shows several faceted planes encountered at edges, with an RMS of 4.62 nm. The current image (b) shows localized distribution with highly conducting sites existed corresponding to the edges or crystalline boundaries of the topographic image, whereas other areas show almost uniform current level reflecting Schottky characteristics. It is clarified that the Schottky barrier is obtained on most area of the film, the exceptions being some ohmic leak sites due to topographic factors, crystalline defects or/and roughness.

Films with improved smoothness were also investigated and the ohmic sites decreased but leaky points still existed. It is revealed that the crystalline defects account for the highly conducting sites, which consequently caused macro ohmic characteristics. It is also proven that C-AFM is an effective tool for microscopic characterization.

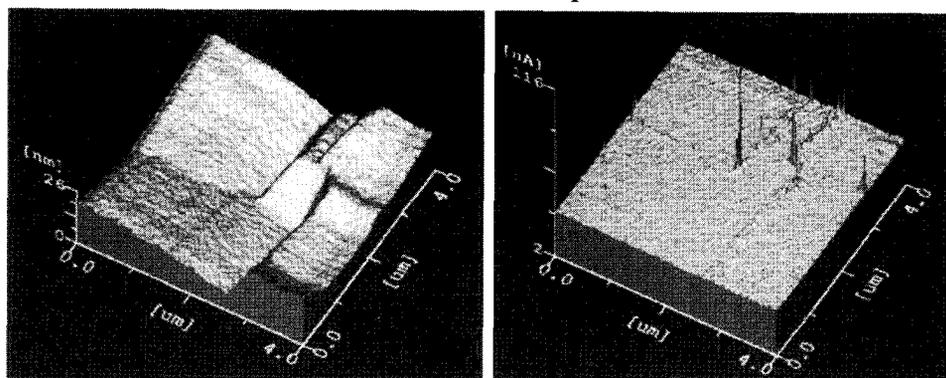


Fig.1
(a) $4\ \mu\text{m} \times 4\ \mu\text{m}$,
topographic
image,
(b) current
image,
bias $V = -2.2\text{V}$.

A JBS diode with surge current capability and controlled forward temperature coefficient

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The Junction Barrier Schottky (JBS) diode in SiC is a competitor to both Si PiN diodes and SiC Schottky diodes in the 600-3300V blocking voltage range. JBS diodes according to Figure 1 were processed on wafers with epitaxial layer designs for 1500-3300V. In a trade-off comparison of several designs with SiC Schottky diodes the JBS diode concept shows significant advantages in blocking voltage, blocking yield, forward temperature coefficient and surge current. These will be discussed in this contribution.

For blocking voltages up to 1700 V, negative forward voltage temperature coefficients were measured at current densities of about 100 A/cm² for Schottky diodes for a ΔT of 125-30 °C=95 °C (Figure 2). In this case the negative temperature dependence in the Schottky contact voltage drop dominates since the drift resistance (with an inherent positive temperature coefficient) is comparatively small (3 mOhmcm²). For paralleling and packaging of devices a positive temperature coefficient is desired in order to have uniform current sharing. In this paper we show how the inflexion point where the temperature coefficient changes from negative to positive can be controlled in the JBS diode, thereby giving an advantage in specifying operating current density. It is the resistive contribution from the p+ grid that lowers the current density inflexion point. In Figure 3 experimental results for the inflexion points are shown for a Schottky diode in comparison with JBS diodes with different p+ grid dimensions (Schottky spacing of either 4 μm or 6 μm). The increase in

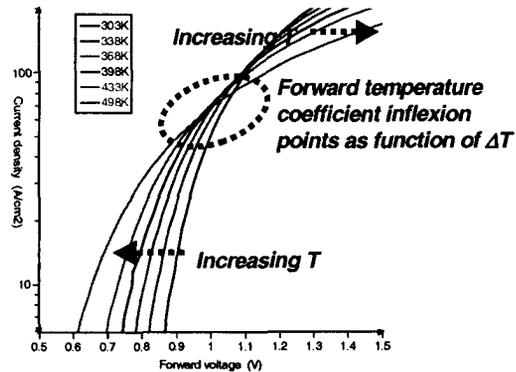


Fig. 2 Semi-log forward characteristics plot of an 1100 V Schottky diode for temperatures 303K-498K.

forward voltage due to the grid resistance is justified by the fact that higher blocking voltages are reached for the JBS diodes (1500 V compared to 1100 V for the Schottky devices on the same epi). This results in a more aggressive epi design in the JBS diode compared to the Schottky offsetting the added grid resistance. The better blocking behavior giving this lower on-state loss and the forward temperature coefficient optimization will be further discussed at the conference.

Surge current capability, i.e., that the device can sustain very high current pulses without damage, is another important issue in most diode applications. The JBS diode would show better high current characteristics than a Schottky diode if the p+ grid

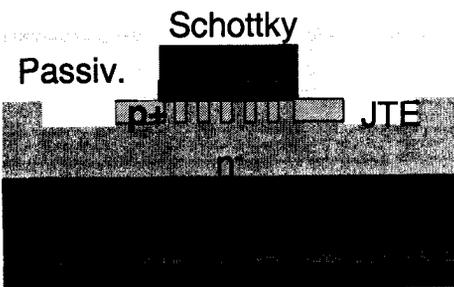


Fig. 1 Schematic cross-section of a JBS diode structure.

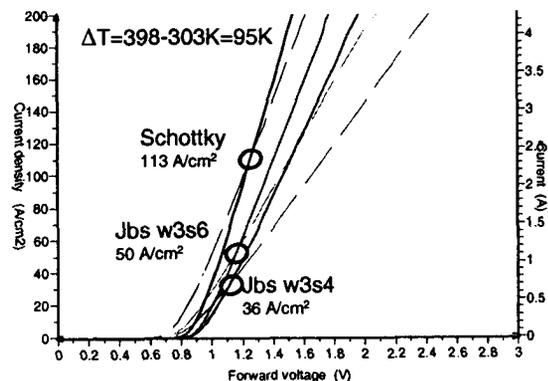


Fig. 3 Forward characteristics at 30°C (solid lines) and 125°C (dashed lines) showing the change from negative to positive temperature coefficient for a Schottky diode in comparison with two JBS designs.

Elastic and Vibrational Properties of Single-Crystal SiC as a Function of Temperature and Pressure

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We report here the first measurements of the five single-crystal elastic constants (C_{11} , C_{33} , C_{44} , C_{12} and C_{13}) for α -SiC (hexagonal, $P6_3mc$ symmetry) to 1000°C, using Brillouin light scattering technique. The results are in excellent agreement with theoretical prediction of the dC_{ij}/dT values reported by Li and Bradt (1987). The isotropic moduli and their temperature dependences, deduced from the single-crystal elastic data from Brillouin spectroscopy, are compared with the high-precision ultrasonic measurements on fully dense polycrystalline specimens of α -SiC and β -SiC (synthesized by CVD process). Except for shear moduli, the elastic moduli and their temperature derivatives for β -SiC measured to $\sim 900^\circ\text{C}$, are higher than those for both single-crystal and polycrystalline specimens of α -SiC.

The pressure dependences of bulk and shear moduli of polycrystalline α and β SiC composites, determined by ultrasonic interferometry to 2 GPa, are reported. The results are in good agreement with high-pressure x-ray diffraction measurements in a diamond-anvil cell to 50 GPa. The Raman scattering measurements on 4H and 6H were made to 32 GPa. The linear positive pressure dependences of Raman shift for the TO and LO modes in the high wavenumber region ($770 - 974 \text{ cm}^{-1}$) and corresponding mode-Grüneisen parameters, calculated from $\gamma_i = -(\partial \ln \nu_i)/(\partial \ln V)$, are in good agreement with previous studies. In contrast, the pressure dependences of the low-lying TA and LA modes in ($100 - 270 \text{ cm}^{-1}$ range), are mostly negative (especially for the 4H type), resulting in lower averaged values of the Grüneisen parameter (0.6). Implication of this is discussed in light of the different elastic properties and compressional behavior in the 6H and 4H polytypes.

Incorporation of Boron and the Role of Nitrogen as a Compensation Source in SiC Bulk Crystal Growth

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P-type doping during PVT growth of bulk SiC is a difficult task because of the lack of a suitable gaseous doping source. Despite recent efforts to solve this problem by applying an additional gas flow where the dopant can be introduced directly into the growth chamber [1], still the most favorable technique implies adding solid sources to the starting material. For example, adding boron carbide to the SiC powder source leads to p-type material with charge carrier concentrations p up to 10^{16} cm^{-3} [2]. This may be used for compensation with a deep donor level like vanadium to obtain semi-insulating behavior [3]. Therefore dopant incorporation homogeneity is crucial, i.e. the concentration $N_A - N_D$ should not vary throughout the crystal.

From previous experiments it is known that nominally undoped crystals exhibit n-type behavior originating from nitrogen as residual impurity. The nitrogen content in the crystal was measured to be $N_D = 2 \times 10^{18} \text{ cm}^{-3}$ at the beginning and below $N_D = 1 \times 10^{17} \text{ cm}^{-3}$ at the end of growth, leading to charge carrier concentrations at 293 K as low as $n = 8 \times 10^{15} \text{ cm}^{-3}$.

Several SiC crystals were grown with different boron concentrations in the source and with different polarity of the seed. Boron is incorporated with a transfer coefficient (ratio of B content in the top of the crystal to initial B content in the source) of about 0.22 for growth on the silicon face and about 0.1 for growth on the carbon face. Chemical analysis shows that during growth the B content in the source slowly depletes, while the B content in the crystal roughly remains constant. At the end of growth, the B concentration in the source is virtually the same as in the crystal. As a result, boron incorporation is segregation-related.

The concentrations of boron acceptors and compensating donors were investigated using Hall effect measurements at 120...700 K. Solving the charge carrier neutrality equation, N_A and N_D were determined in dependence of the growth time for SiC crystals doped with B of various amounts. N_A remains constant during growth, while N_D strongly decreases. Detailed analysis shows that, especially for low compensation ($N_A/N_D \geq 10$), the onset of the freeze-out range strongly depends on N_D , which in turn leads to an almost exponential rise of the hole concentration with growth time, even though $N_A - N_D$ remains constant.

As a conclusion, boron is incorporated homogeneously into SiC when added as a solid source, but nitrogen contamination strongly influences the charge carrier concentration below 300 K. To achieve high homogeneity of $N_A - N_D$, impurity control is decisive especially for low-doped growth. Finally, a decrease in the hole concentration around faceted areas, which is observed in p-type SiC growth, is found to be related to the step height on the growth surface. A model for the dopant incorporation on different step heights is proposed.

- [1] T.L.Straubinger, P.J.Wellmann et al., oral presentation #72 at the conference
- [2] M.Bickermann et al., Journal of Crystal Growth 233 (2001) 211
- [3] M.Bickermann et al., oral presentation # 79 at the conference

New and Improved Quantitative Characterization of SiC using SIMS

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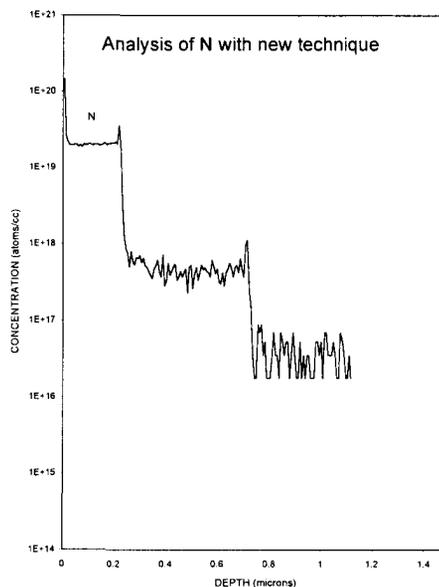
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SiC is a very important material for high-power, high-temperature, and high-radiation devices. Dramatic progress in SiC power transistors, LEDs, and sensors have made it imperative to accurately control the dopant and impurity levels. Due to its unique capabilities of high detection sensitivity for a variety of elements under depth profiling mode, Secondary Ion Mass Spectrometry (SIMS) is an essential tool for characterization of dopants and impurities in SiC material.

Over the past few years, we have made significant progress performing quantitative SIMS analysis for dopants and impurities in SiC with high sensitivity, excellent depth resolution and long term reproducibility. In this paper, we will present our development in the following areas:

(1) **Analysis of N with much improved precision:** A new N analysis technique was developed by monitoring atomic ions of nitrogen. This new technique provides a much improved precision and depth resolution at reasonable detection limit (see figure).

(2) **Improvement of detection limits:** We have modified the hardware on our commercial SIMS instruments. We are now able to achieve detection limits of 2×10^{13} at/cm³ for B and Al, and 1×10^{16} at/cm³ for N, routinely. This represents an improvement of 5 to 10 over the “typical” detection limits obtained on a SIMS instrument. We have also developed a new analytical protocol for transition metals. For example, we are able to achieve detection limit of 2×10^{14} at/cm³ for Fe and 5×10^{13} at/cm³ for Cr – a factor of 10 improvement over what can be achieved a few years ago.



(3) **Surface contamination analysis:** We have developed new protocols to provide accurate surface contamination measurement on SiC surfaces.

In addition, we will present the long term analysis precision studies on N, B and Al analysis. All these analyses are based on carefully prepared SiC implant standards.

Characterization of SiC Epitaxial Wafers by Photoluminescence under Deep UV Excitation

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We demonstrate that photoluminescence (PL) under deep UV light excitation is advantageous for characterizing thin epitaxial layers of 4H- and 6H-SiC crystals because of the short penetration depth of the light. We used the 266 nm light from a quadruple YAG laser as an excitation source. The penetration depths of the light are about 1.2 and 1.0 μm for 4H- and 6H-SiC crystals, respectively, which are significantly shorter than the corresponding values of 7.5 and 4.3 μm for the 325 nm light from a conventional He-Cd laser [1].

Samples were obtained from a commercial source and were heavily doped *p-on-p* 4H- and 6H-SiC epitaxial wafers with a carrier concentration in the range of $1 \times 10^{19} \text{ cm}^{-3}$ and with an epitaxial layer thickness of about 5 μm. We performed PL spectroscopy at temperatures from 4.2 to 295 K, and PL wafer mapping at 295 K. The PL was excited by a quadruple YAG and He-Cd lasers using a back-scattering configuration.

Figure 1 shows PL spectra of a 4H-SiC epitaxial wafer at 295 K. The spectrum (a), obtained under the 266 nm excitation from the front surface (the epitaxial layer side), represents the PL from the epitaxial layer. The near band-edge emissions at 3.20 and 3.00 eV are due to free exciton and free-to-acceptor (AI) recombination, and the 1.80 eV band has not yet been identified. Deep-level emission was below our detection limit. In contrast, the spectra (c) and (d), excited by the 325 and 266 nm light from the back surface, respectively, are the PL from the substrate. The 1.80 eV band and deep-level emission lines at 1.40, 1.12, 1.06 and 0.97 eV were observed, while no band-edge emission appeared. These deep-level emission lines have not yet been identified except for the V-related 0.97 eV line. The appearance of the band-edge emission and the disappearance of the deep-level emission in the epitaxial layer and *vice versa* in the substrate indicate the superiority of the crystalline quality of the epitaxial layer. The spectrum (b), excited by the 325 nm light from the front surface, contains both band-edge and deep-level emissions, indicating that the long penetration depth of the 325 nm light excites the substrate as well as the epitaxial layer. The 325 nm light excitation is, therefore, not suitable for the characterization of the epitaxial layer. Essentially the same results were obtained in most epitaxial 4H and 6H SiC wafers.

We performed wafer mapping of the intensity of the respective PL lines. The 1.80 eV band from the substrate shows a circular pattern, which we believe originates from the facet growth. A similar pattern was observed in the deep-level emissions. The 1.80 eV band from the epitaxial layer shows a substantially different pattern with bright spots in the central area. An opposite intensity contrast was observed in the band-edge emission. These findings suggest that the defects responsible for the 1.80 eV band in the epitaxial layer were not transferred from the substrate but were generated during the epitaxial growth.

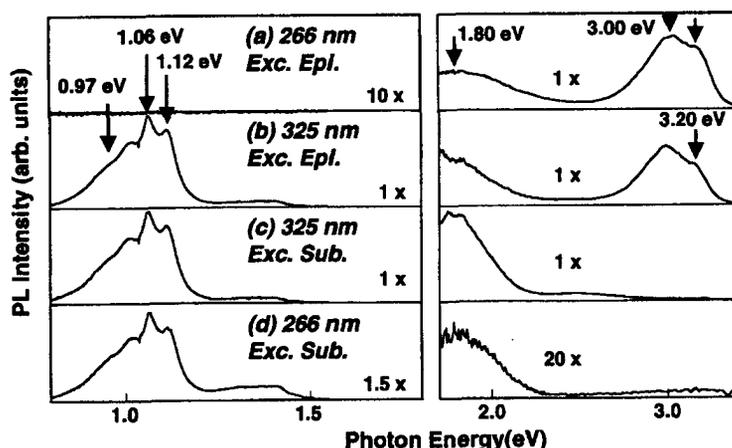


Fig. 1. PL spectra of *p-on-p* 4H-SiC epitaxial wafer at 295 K.

[1] S. G. Sridhara *et al.*: Mat. Sci. Eng. B61-62, 229 (1999).

Direct synthesis and growth of SiC single crystal from ultrafine particle precursor

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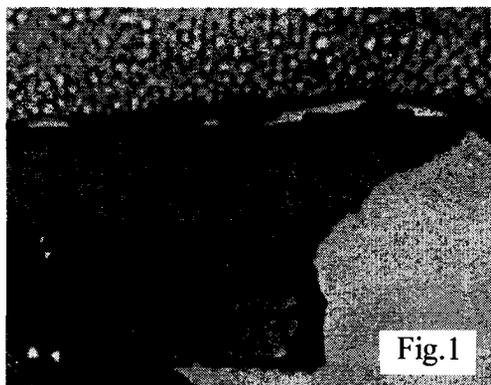
In the present study, we tried to grow 6H-SiC single crystals by feeding with SiC nutritious species which were synthesized on the surface of 6H-SiC seed crystals through carbothermal reduction of SiO₂ ultrafine particles by C ultrafine particles, and found that rapid epitaxial growth of the seed crystal happened.

The precursor for SiC synthesis was prepared by compounding SiO₂ and C of approximately 1 to 3 molar ratio. SiO₂ source(fumed silica) and C source(carbon black) were mixed and diluted by pure water and ball-milled with polyethylene ball and jar, for longer than 24 hours. The slurry after milling was dried and comminuted to fine particles less than 100 μm in diameter by ball-milling. The prepared precursor powder was charged on the surface of 6H-SiC seed crystal, put on the bottom of the graphite crucible with a lid.

The experiments to grow the 6H-SiC single crystal in the graphite crucible were conducted in an electric furnace with graphite heating elements, under Ar ambience of atmospheric pressure. The crucible was heated up to the target temperature of 2300°~2500°C at the ramping rate of 30°~40°C/min. and held at the top temperature for 20min., before the start of cooling down by switching off the heater current.

The photograph of cross section of the single crystal grown at 2300°C is shown in Fig.1. About 500 μm thick layer was grown on the seed crystal of 250μm thickness. Its morphology shows a single crystal epitaxially grown on the seed crystal, regardless of included many voids and pipes in the grown layer. Fig.2 is a cross sectional view of the single crystal grown at 2400°C. An apparent difference in number and size of visible crystal defects, exists between Fig.1 and Fig.2. The thinner grown layer of Fig.2, compared with Fig.1, implicitly shows that its surface temperature was higher than the sublimation temperature of SiC single crystal, because it had to be fed with a larger amount of SiC nutritious species, as it was grown at higher temperature than in case of Fig.1.

Based on this result we concluded that ultrafine particle precursor enabled to grow SiC single crystal at high enough temperature exceeding the sublimation temperature of seed crystal.



Ultrafast electron relaxation processes in SiC

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The ultrafast electron relaxation dynamics in SiC is studied by using the pump and probe transient absorption technique. It is well known that SiC has appreciable absorption band in the visible region as reported by Biedermann [1]. These absorption bands are ascribed to the inter-conduction band transition from the lowest conduction band. Instead of the valence to conduction band transition, these inter-conduction band transitions are used to probe the electrons in the lowest conduction band. The light sources employed in this experiment were a 1 kHz regenerative amplifier (Spectra Physics, Spitfire, 120 fs, 800 nm) and a tunable wavelength conversion system (SP, OPA800F). The samples used were 6H-SiC and 4H-SiC single crystals with the faces parallel to the c-axis. The electron doping levels was about $1.2 \times 10^{18} \text{cm}^{-3}$ for 6H and $1.0 \times 10^{18} \text{cm}^{-3}$ for 4H sample, respectively.

In 6H-SiC, the bleaching with a time constant of 1.25 ps was observed between 1.82 and 2.38 eV. The spectral profiles of this bleaching are compared with those of Biedermann bands for each polarization configurations, and this bleaching is ascribed to reflect the decrease of electron population in the lowest conduction band. The electrons in the lowest conduction band are supposed to be excited to the higher conduction band, and are speculated to relax to the lowest conduction band via inter-conduction band electron-phonon scattering, electron-electron scattering, and intra-band cooling processes. The observed relaxation time of the bleaching is concluded to reflect the inter-band scattering time [2]. In 4H-SiC, the sub-picosecond bleaching and induced absorption are also observed. Probably, this transient behavior corresponds to the shift and bleaching of Biedermann bands. We tentatively assigned the observed relaxation time to the electron-phonon scattering time in 4H-SiC.

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[2] T. Tomita, S. Saito, T. Suemoto, H. Harima, and S. Nakashima, Appl. Phys. Lett. **79**, 1279 (2001)

Optimized P-well profile preventing punch-through for 4H-SiC Power MOSFETs

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In order for SiC power MOSFETs to provide high breakdown voltage, punch-through that occurs in the P-well must be prevented. For that purpose, it is necessary to form a deep P-well, but that is hard to accomplish especially in SiC. Moreover, the surface concentration of the P-well should be at a low level for the channel formation. In this work an attempt was made to optimize a retrograde P-well profile. Fig. 1 shows the 4H-SiC power MOSFETs structure used. Fig. 2 shows the carrier concentration distributions of the P-well at the dashed line in Fig. 1. The carrier concentration at a depth of $0.8 \mu\text{m}$ was high and the surface concentration was low. The optimized P-well profile was obtained by a 2-dimensional numerical simulation with *Dessis (ISE-TCAD)*.

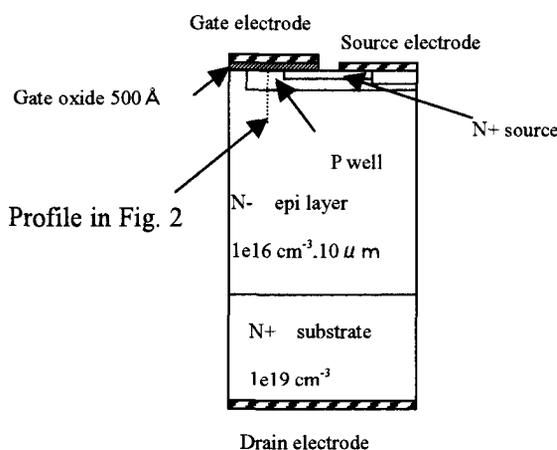


Fig. 1 Schematic cross-section of SiC-power MOSFET. Channel length= $2 \mu\text{m}$, N-epi layer = $1\text{e}16 \text{ cm}^{-3}$, $10 \mu\text{m}$.

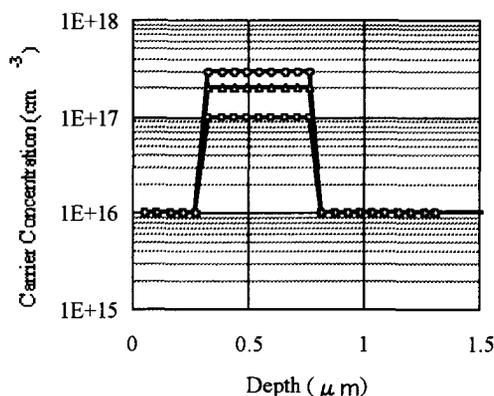


Fig. 2 P-well profile used in this work

This is the first detailed analysis of a P-well profile without punch-through. Fig. 3 shows the simulation results for the reverse blocking characteristics of this device. When the peak concentration of the P-well was over $3\text{e}17 \text{ cm}^{-3}$, the ideal avalanche breakdown was obtained even though the P-well depth was only $0.8 \mu\text{m}$. This result is practical and the device can be fabricated by normal ion-implantation techniques.

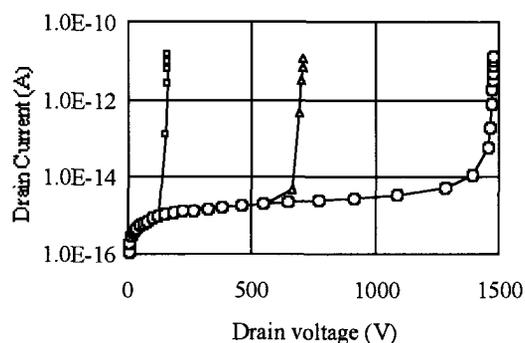


Fig. 3 Reverse blocking characteristics of SiC power MOSFETs obtained with *Dessis-ISE*. P-well peak concentrations are (□): $1\text{e}17 \text{ cm}^{-3}$, (△): $2\text{e}17 \text{ cm}^{-3}$, (○): $3\text{e}17 \text{ cm}^{-3}$.

Compatibility of VJFET technology to MESFET fabrication and its interest to system integration : fabrication of 6H and 4H-SiC 110V lateral MESFET.

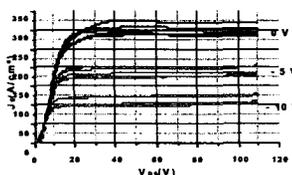
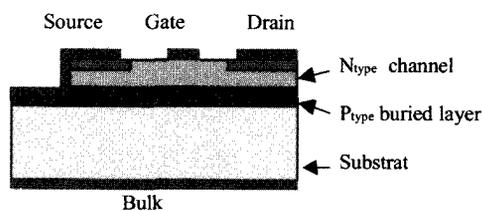
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Introduction : Integration of Power devices with their control circuitry is a usual challenge in Si and SiC technologies to increase efficiency of power switch and systems. The purpose of this article is to evaluate the integration compatibility of lateral MESFETs within a Vertical power JFET fabrication technology. The interest of this method is to allow to make control circuitry based on MESFET devices to get both power devices and control circuits on the same die. Several possibilities can be usually foreseen for the realisation of lateral SiC-MESFET [1], using conductive substrate or semi-insulated wafer. Other possibilities, more compatible with a vertical power device process, are P and N wells formation by ion implantation to form the lateral channel. The description of the fabrication process presented below is a part of the fabrication process of a VJFET designed for high voltage current limitation [2]. High energy implantation, RIE etching adjustment and metal contact annealing are the critical steps of the fabrication of this device, and will be developed, such as electrical characterization of fabricated MESFET.

Process fabrication : 6H and 4H SiC wafers with a N epitaxial layer doping concentration in the range of $5.10^{15} \text{ cm}^{-3}$ (15µm) from Cree INC were used for the devices fabrication. A high energy Al implantation (2MeV, dose of 10^{14} cm^{-3} @400°C) has been performed to form the P buried layer. A N-type box profile was formed at the surface of the wafer by multiple N implantation ($9.8.10^{12} \text{ cm}^{-2}$). N was then implanted (10^{15} cm^{-2}) for contact zones of drain and source. The wafers were annealed at 1700°C/30min. A deep RIE etching (1,2 µm), adjusted in relation with simulated profile of Al implantation [3], was performed to contact the P buried layer. A cross section and a top picture of the fabricated MESFET is presented below.



Electrical characteristics

Picture of the fabricated MESFET

Thermal oxidation followed by an oxide deposition was realized to form the passivation layer. Ni or W layers were deposited and then annealed at different temperatures for gate and ohmic contacts. Both ohmic and Schottky contacts were simultaneously realised using one mask level for metal patterning.

Electrical characterization :

The extracted contact resistivity is in the range $4.6.10^6 \text{ } \Omega \cdot \text{cm}^2$ for the Ni 6H-SiC samples (annealing time: 3 min at 900°C) and $7.7.10^5 \text{ } \Omega \cdot \text{cm}^2$ for the 4H-SiC, values in the state of the art [4]. The PN rectifier formed between the P buried layer and the epitaxial layer (Source/Bulk) exhibits a blocking voltage around 950V @ 1.10^{-3} A/cm^2 . The 4H-SiC MESFET specific on-resistance is $38 \text{ m}\Omega \cdot \text{cm}^2$ in linear region and the transconductance is $0,4 \text{ mS}\cdot\text{mm}^{-1}$. This low value is mainly due to high reverse leakage current of Schottky contact. This is the main point to improve in the next generation of devices. Two

mask levels for metal deposition and patterning should be envisaged. In addition, on-state current density of 300 A/cm^2 @ 110V in limitation mode have been reached as shown in the figure above.

[1] Nilsson & al , "Characterization of SiC MESFET on conducting substrate", p1255-p1258, ICSCRM 99

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[3] E.Morvan, "Modelisation de l'implantation ionique dans alpha-SiC et application a la conception de composants de puissance". Th Doct Lyon Instn Nat Sc Appl 1998 298p

[4] J.Crofton, et al."High temperature ohmic contact to n-type 6H-SiC using nickel". J. Appl. Phys., 1995 vol 77, No 3, p 1317 131

Conclusion : The full compatibility of MESFET realisation with VJFET process fabrication technology has been studied and demonstrated. The interest of high energy implantation to form deep junction is applied to the elaboration of a VJFET and lateral MESFET. Process elaboration of the MESFET will be developed, such as electrical characterization (ohmic and schottky contact study). Key points for the amelioration of the performances of the MESFET will be underlined in the final paper, as few technological adaptations will allow to improve characteristics of MESFET.

Influence of Gate Finger Width on RF Characteristics of 4H SiC MESFET

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Conventional mesa isolated SiC MESFETs with different gate finger width 100, 200, 500, 1000 μm were fabricated on epitaxial layers grown on semi-insulating 4H-SiC substrate purchased from CREE Inc. The epitaxial layers consists of a highly doped layer, channel layer with doping density of $3.0 \times 10^{17} \text{cm}^{-3}$ of 0.25nm thickness and lightly doped p buffer layer. Only one gate electrode of 0.5 μm length was drawn on each MESFETs by using electron beam lithography.

Figure 1 shows the gate finger width dependence of cutoff frequency (f_t) and the maximum frequency of operation (f_{max}). With increasing the gate finger width, cutoff frequency rose from 4.8GHz to 11GHz. This improvement will be caused by reduction of the influence of extrinsic capacitance of MESFET on cutoff frequency. Because lager gate finger width will increase intrinsic gate-source capacitance and transconductance of MESFET, without increasing extrinsic capacitance generated by connecting pads and lines. On the other hand, the value of f_{max} was decreased with increasing the gate finger width. Increasing input losses due to the large gate resistance will cause this decline.

Figure 2 shows output power characteristics measured with load-pull method at 1.0GHz. Output power increased in proportion to the gate finger width. Output power over 2W can be obtained with the gate finger width of 1mm. The maximum output power density of 2.6W/mm can be obtained with the gate finger width of 200 μm .

Acknowledgment: This work is performed under the management of FED as a part of the METI Project(R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

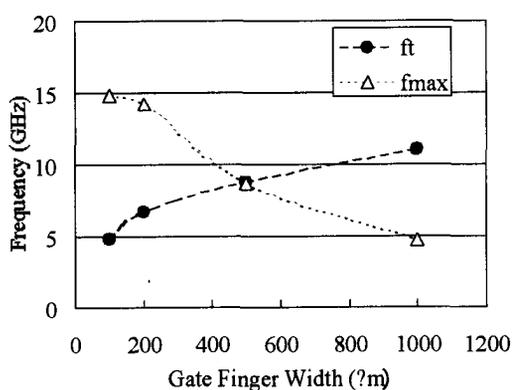


Fig.1 RF characteristics of SiC MESFET with different gate finger length.

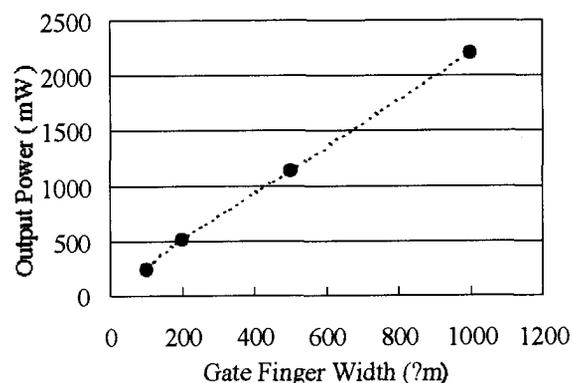


Fig.2 Output characteristics of SiC MESFET with different gate finger length.

Traveling self-confined-solvent method: A novel LPE growth of 6H-SiC

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The growth of high quality SiC without defects is an urgent target for high power device applications. The growth from liquid phase has been considered to be advantageous to improve the material quality due to the process under thermal equilibrium. In the case of SiC, however, the lack of stoichiometric liquid phase has restricted the choice of proper solvents to Si, which allows only a small solubility of C [1,2]. Thus the use of Si-solvent requires extremely high processing temperature to reach high growth rate, which induces thermal instabilities.

In this study, we propose a novel liquid phase epitaxial growth of 6H-SiC(0001) employing a new sandwich configuration with no temperature gradient. It consists of a polycrystalline SiC source platelet and a seed substrate with the 20 μ m thick extremely thin Si-solvent layer in-between, which is formed by the self-penetration of surrounding Si liquid at temperatures above 1450C. The use of this particular thickness of the Si-solvent layer guarantees the stable growth of SiC up to 2300C, without being obstructed by thermal instabilities including thermal convection. As a result, a 300 μ m-thick 6H-SiC single crystal of single domain was successively grown in 30 min at 2300°C (Fig.1). The structural and optical properties of the grown layer were characterized by optical microscopy, AFM, X-ray topography, TEM, and cathode luminescence.

It is revealed that the growth front preserves smooth surface with an atomically flat terrace of 50 μ m width terminated by a few nanometers height bunched step. This is a clear evidence showing the reduction in the thermal instabilities. The growth mechanism is directly attributed to the difference in surface energy between the substrate and the source resulting in the difference in the equilibrium concentration of C.

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[2] A. E. Nikoleav, V. A. Ivantsov, S. V. Rendakova, M. N. Blashenkov, V. A. Dmitriev, J. Crystal Growth 166 (1996) 607

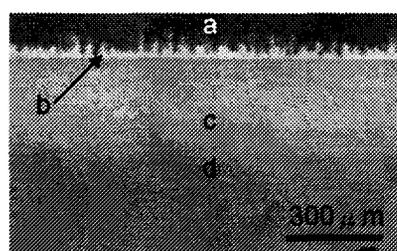


Fig. 1. Cross sectional view of grown layer. a : substrate, b : grown layer, c : Si layer, d : polycrystalline plate.

Optical and electrical characterization of free standing 3C-SiC films grown on undulant 6-inch Si substrates

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Recently, Nagasawa *et al.* of the HOYA R&D Center, Japan have announced successful CVD growth of high quality 3C-SiC films of up to a few hundred micron thick with a very small density of defects ($10^4/\text{cm}^2$) [1]. The new 3C-SiC epilayers have been grown on so-called undulant Si(001) wafers of 6-inch in diameter by CVD method to have planar defects collide and cancel out each other within the first $\sim 50 \mu\text{m}$ from the Si/SiC hetero interfaces. Defects present in the region more than $50 \mu\text{m}$ away from the interface are dominantly twin boundary planes being parallel to each other with approximate separation distances of $3 \mu\text{m}$.

In this work we report on the electrical and optical characterization of the free standing 3C-SiC made by the HOYA R&D Center. Two series of samples have been studied; nominally undoped samples and intentionally nitrogen doped samples of the concentration 10^{18} and 10^{17}cm^{-3} , respectively.

The electrical properties have been investigated by variable temperature Hall effect measurements for the temperature range $T=10\text{-}400\text{K}$. The large improvement in the low temperature free carrier mobility has been observed when the near interface heavily defected region has been lapped away.

The optical properties have been investigated by photoluminescence (PL) spectroscopy at $T=3\text{-}300\text{K}$. The PL spectrum at 3K shows sharp features of nitrogen donor bound excitons. Above 50K, broad peaks due to the free exciton recombination were observed for undoped sample (Fig.1) indicating a high quality of the sample. The free exciton luminescence, which is a good measure of the quality of the sample, has been observed before for homoepitaxially grown 3C-SiC [2] but never in as grown samples. Our result is remarkable considering the fact that the film has been hetero-epitaxially grown directly on Si with the growth speed of $50 \mu\text{m}/\text{hour}$.

We would like to thank H. Nagasawa of the HOYA R&D Center for kindly providing us the samples and K. Kojima for helpful discussions.

[1] Hiroyuki Nagasawa *et al.*,
to be published in Journal
of Crystal Growth and
www.hoya.co.jp/eng/news/index5.html

[2] Katsushi Nishino *et al.*,
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pp. 6405-6410

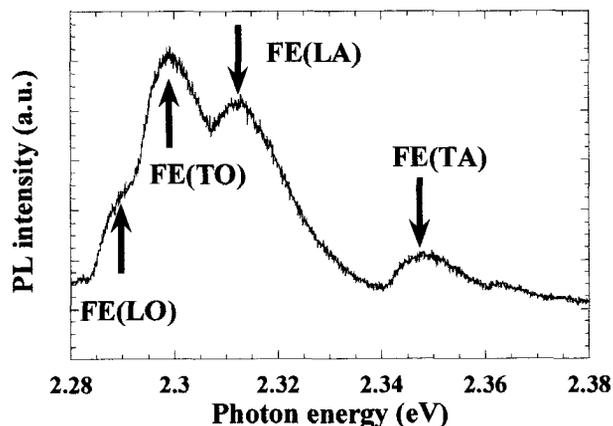


Fig.1 Free exciton luminescence of nominally undoped 3C-SiC at 80K

Study on Metamorphosing Top Si Layer of SOI Wafer into 3C-SiC Using Conventional Electric Furnace

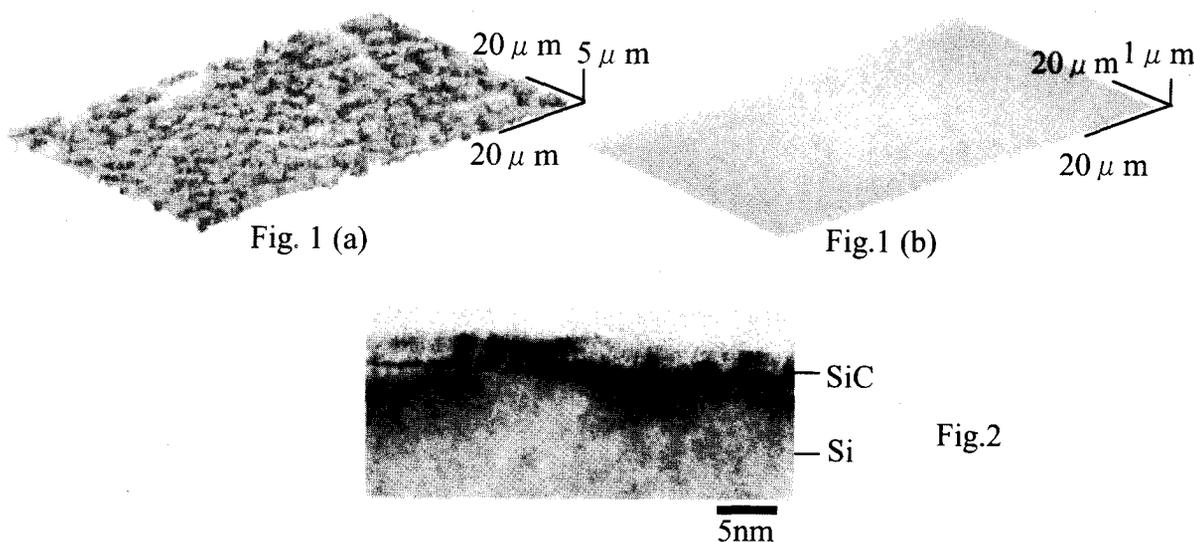
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Based on Silicon-on-Insulator (SOI) technology, we have a plan to develop electron-photon-merged devices. This plan calls for CMOS-LSI/SOI and LED-array/GaN to be monolithically fabricated on one chip. In order to reduce the lattice mismatch between Si and GaN, we are attempting to form a GaN/SiC/SOI structure. We are using a conventional electric furnace, without any vacuum system, to metamorphose the top Si(111) layer of the SOI substrate into 3C-SiC(111) under the atmospheric pressure of propane gas in hydrogen at about 1250°C. This method of forming a SiC-on-Insulator (SiC-OI) substrate is inexpensive and makes it easy to enlarge the wafer size. In addition, the SiC-OI substrate can be applied not only to SiC devices but also to extensive substrate materials of GaN devices.

Figures 1(a) and (b) show the surface morphologies of specimens after carbonizing the top Si layers of SOI substrates, measured with a laser microscope. Figure 1(a) corresponds to an image of carbonization in hydrogen and propane after temperature elevation to about 1250°C under a pure hydrogen ambient, while (b) corresponds to an image of carbonization by temperature elevation to about 1250°C under a hydrogen and propane ambient. The surface micro-roughness of specimen (b) is greatly reduced compared to that of specimen (a). It is supposed that, in the case of (a), the bare Si layer reacts with such impurities as water in the hydrogen gas during the temperature elevation, leading to the increased surface micro-roughness of the specimen. In the case of (b), in contrast, the SiC layer is gradually formed at lower temperatures, which prevents impurities from reacting with the Si layer. For both specimens, however, 3C-SiC(111) peaks ($2\theta = 35.6^\circ$, Cu-k α) are clearly observed from X-ray diffraction measurements. This finding indicates that the formed SiC layers have good crystallinity.

Figure 2 shows a cross-sectional TEM image of the specimen in 1(b). The Si surface of the SOI wafer is metamorphosed into 3C-SiC(111) with the thickness of 3nm. We can therefore expect the whole 100 nm top Si layer of the SOI substrate to be metamorphosed into a uniform SiC layer by optimizing the reaction time, flow rates of gases, and so on.



Radiation response of 6H-SiC MOSFETs fabricated using pyrogenic condition

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Electron-hole pairs are liberated in the silicon dioxide when exposed to ionising radiation. Subsequently most of the initially generated electron-hole pairs recombined, a fraction of them remains in the oxide layer. Under favourable biased conditions, the electrons are swept out of the oxide and the positively charged holes are trapped within the oxide and near the interface of the SiO₂/SiC system. These trapped holes degrade the channel mobility of MOSFET and pose oxide reliability issue. For this reason, many studies on the radiation effects on Si MOSFETs have been performed. Few works show the effects of gamma irradiation on SiC MOSFETs. In this paper, we present new electrical response of p-channel MOSFETs when exposed to gamma ray irradiation. Our results are also compared to the irradiated n-channel 6H-SiC and Si devices. The oxides are grown using pyrogenic condition and irradiated at zero applied bias to all the electrodes.

Fig. 1 shows the shift of the threshold voltage of the irradiated devices. The n-channel threshold voltage decreases initially due to the buildup of positive oxide trapped charge. Above 10⁵Gy(SiO₂), the threshold voltage rebounds. In the case of the p-channel, both the formation of oxide trapped charge and interface traps are positively charged, and contributed to the large negative voltage shift. Fig. 2 depicts the normalised mobility as a function of absorbed dose for both the n-channel and p-channel devices. Interestingly, the initial mobility of the p-channel devices increase up to 1.3 times of its pre-radiation value before decrease on further irradiation. This increase in the hole mobility is attributed to the passivation of the interface states and reduces the scattering of the channel holes. Further irradiation results in an increase in the oxide and interface charge traps, and therefore reduces the hole mobility. At low irradiation doses, the mobility of the Si MOSFET has reduced substantially. Unlike the Si device, the electron mobility of the n-channel SiC device remains unchanged up to a dose of 3×10⁵Gy(SiO₂). All these influences of gamma irradiation on the devices and device fabrication steps will be given in details in the paper.

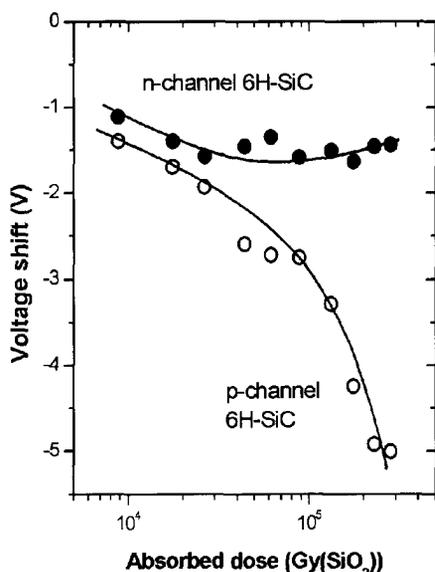


Fig. 1 The threshold voltage shift of n-channel and p-channel devices as a function of absorbed dose.

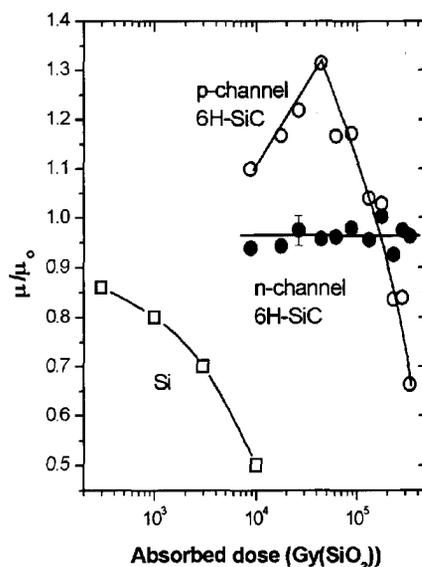


Fig. 2 The normalised mobility of the Si and SiC MOSFETs as a function of absorbed dose.

Abstract

submitted to the International Conference on Silicon Carbide and Related Materials 2001

October 28 - November 2, 2001

Tsukuba International Congress Center (Epochal Tsukuba) in Tsukuba, Ibaraki, Japan

Electrical properties of 4H-SiC thin films reactively ion-etched in SF₆/O₂ plasmas

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Effects of dry etching process on the electrical properties of 4H-SiC were investigated. Au Schottky barrier diodes(SBD's) were fabricated on the reactively ion-etched surface of 4H-SiC thin films. The surface roughness, residues and defects, which were produced during dry etching could deteriorate the electrical properties of Schottky diodes. Such harmful effects were determined by current-voltage(I-V) and capacitance-voltage(C-V) measurements. The Auger electron spectroscopy(AES) was also performed to reveal the species of residues on the etched surface after RIE process. The surface roughness before and after etching process was evaluated by the atomic force microscopy(AFM).

The I-V characteristics of SBD's on the etched surface were found to be deteriorated compared with that of the SBD's on the unetched surface from the measurement of Schottky barrier height, ideality factor and reverse leakage current. However, an increase of oxygen content in gas mixtures made an improvement in the performance of Schottky diodes. It might be ascribed to the faster removal of carbon-excess surface layers with etching-induced damage and the smoother etched surface. The RMS roughness of etched surface with AFM scan area of $5 \times 5 \mu\text{m}^2$ was actually improved from 8.5 \AA to 5.7 \AA with an increase of the oxygen content in the reactant gases from 0% to 50%. And the AES analysis revealed that the RIE etched surfaces had the residual contaminants, of which the species were fluorine and oxygen, regardless of etching conditions. These results indicate that the SBD's fabricated with higher oxygen percentage in the etchant gases had better device performance than that with lower oxygen contents in spite of residual contaminants on the surface.

Acknowledgement

This work was done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

Keyword : Reactive ion etching, Schottky barrier diode, Etching-induced damage

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Influence of Excited States of Deep Acceptors on Hole Concentration in SiC

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Experimental acceptor levels ΔE_A in SiC, measured from the valence band E_V , are reported to be deeper than 150 meV. Moreover, the ground and first excited state levels of acceptors in SiC, calculated by hydrogenic acceptor [$\Delta E_r = 13.6(m^* / \epsilon_s^2 r^2)$ eV], are 136 meV and 34 meV, respectively. The experimental ΔE_A is deeper than ΔE_1 , because of central cell corrections, while ΔE_r ($r \geq 2$) are considered to be reasonable, and should affect the hole concentration $p(T)$. Using three kinds of distribution functions, we theoretically and experimentally investigate the influence of the excited states on $p(T)$.

The proposed distribution function for electrons is expressed as

$$f(\Delta E_A, n, \overline{E_{ex}}) = \frac{1}{1 + 4 \exp\left(-\frac{\overline{E_{ex}}}{kT}\right) \cdot \left\{ g_1 \exp\left(\frac{\Delta E_A - \Delta E_F}{kT}\right) + \sum_{r=2}^n g_r \exp\left(\frac{\Delta E_r - \Delta E_F}{kT}\right) \right\}}, \quad (1)$$

where ΔE_F is the Fermi level measured from E_V , g_r is the $(r-1)$ -th excited state degeneracy factor, and n is the highest excited state, which we consider in analysis. Here, the average acceptor level $\overline{\Delta E_A}$ is expressed as $\overline{\Delta E_A} = \Delta E_A - \overline{E_{ex}}$, and $\overline{E_{ex}}$ is the ensemble average of the ground and excited state levels, which increases with T . The Fermi-Dirac distribution function corresponds to $f(\Delta E_A, 1, 0)$ and the conventional function is $f(\Delta E_A, n, 0)$.

Using p-type 6H-SiC wafer, $p(T)$ was obtained by Hall-effect measurements. Using Free Carrier Concentration Spectroscopy (FCCS), ΔE_A , the acceptor density N_A and the compensating density N_{com} were determined, and are shown in Table 1. Figure 1 shows the $p(T)-1/T$ curves, and Fig. 2 displays the FCCS curve given by $H(T, E_{ref}) \equiv p(T)^2 \exp(E_{ref}/kT)/(kT)^{5/2}$, where the simulation results mean the curves simulated using Table 1.

In $f(\Delta E_A, 1, 0)$, although the simulated $p(T)$ is in agreement with the experimental $p(T)$, the simulated $H(T, E_{ref})$ is not, indicating that the excited states should affect $p(T)$. In $f(\Delta E_A, n, 0)$, the density of holes bound to acceptors increases, which results in the unreasonable high N_A . In our case, there are good coincidences between the experimental data and simulation results in Fig. 1 as well as in Fig. 2, and N_A and ΔE_A are considered to be reasonable.

In summary, the influence of the excited states on $p(T)$ should be considered, and the distribution function used in deep acceptors should be $f(\Delta E_A, n, \overline{E_{ex}})$.

Table 1 Results determined by FCCS

	$f(\Delta E_A, 1, 0)$	$f(\Delta E_A, 10, 0)$	$f(\Delta E_A, 10, \overline{E_{ex}})$
N_A [cm^{-3}]	2.95×10^{19}	2.19×10^{20}	1.91×10^{18}
ΔE_A [meV]	182	205	189
N_{com} [cm^{-3}]	8.35×10^{17}	2.65×10^{18}	3.37×10^{16}

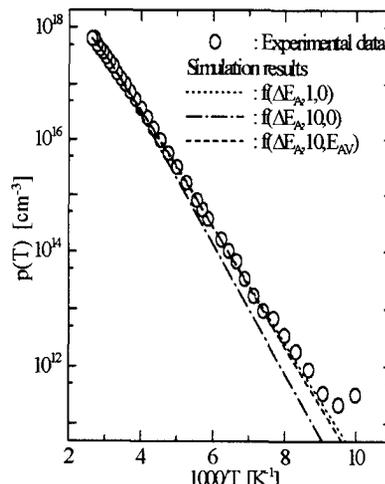


Fig. 1 Experimental and simulation results of $p(T)$

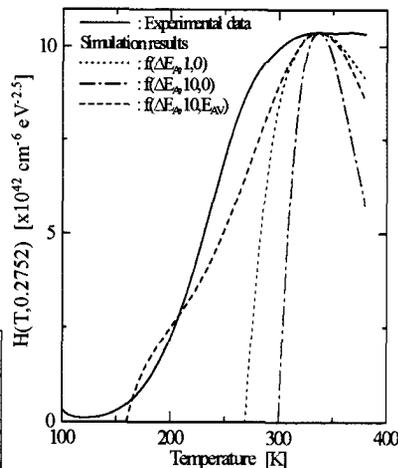


Fig. 2 Experimental and simulation results of $H(T, E_{ref})$

ALUMINIUM NITRIDE BULK CRYSTALS BY SUBLIMATION METHOD: GROWTH AND X-RAY CHARACTERIZATION

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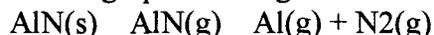
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Aluminium nitride AlN, a wide band gap material isomorphous to gallium nitride has good dielectric properties and chemical stability up to 1400°C. Despite of not enough maximum size of AlN single crystals reported so far the bulk crystals and thick epitaxial layers of aluminium nitride have a great potential as the substrate materials for GaN-based epitaxial structures.

Here, aluminium nitride crystals have been grown by sublimation technique in the conventional growth cell designed earlier for obtaining silicon carbide ingots by modified Lely (LETI) method of growth. High purity AlN powder was used as a source, a number of materials (SiC platelets, AlN/Al₂O₃ epitaxial structures, polycrystalline and textured Ta, W, C) serve as the substrates. Deposits were prepared at 1400..2100°C and reduced pressure of gas ambient (Ar+N₂) for 1..10 h. Conventional X-ray diffraction methods (mainly, double-crystal diffractometry and Laue pattern technique) have been employed to characterize the structure and phase composition of deposits. To prevent an effect of catalytic reduction of aluminium nitride onto the surface of graphite fittings in accordance with the reaction:



an additional foil insulation was placed into the growth cell.

We usually observe there are no any deposits onto the graphite substrate due to the reduction mechanism mentioned above. Unexpectedly, the formation of homogeneous AlN crystalline deposits onto the single crystalline SiC substrates is also hard to achieve. The samples grown at 1500..2000°C in both the vacuum and residual gas ambient were as a rule multiphase and contain both aluminium nitride and complex carbides such as Al₄SiC₄ and Al₄Si₂C₅. This effect probably being a result of surface graphitization of silicon carbide at the growth temperatures is also responsible for relatively small growth rates observed for SiC substrates. Singlecrystalline growth has been achieved onto AlN/Al₂O₃ epitaxial structures at the temperatures less than 1800°C. X-ray diffraction showed that the deposits with the thickness of up to some millimeters grown onto the substrate of up to 1 inch in diameter had obvious for aluminium nitride wurtzite structure. From the practical point of view, the major problem consists in the intensive nitridation of corundum part of epitaxial structure at the high temperatures of growth leading to its cracking and even to mechanical destruction. So, corundum substrate exposed at the 1600°C for 4 hours almost completely converts into the set of oxynitrides. Nevertheless, thick corundum substrates (more than 1000 μm) with the thick epitaxial layers appear to be successfully used as the initial seed of large-scale area for AlN growth in conventional sublimation process.

Also, large-grain homogeneous textured deposits were prepared onto the metal substrates such as tantalum and tungsten. The deposits were found to be only wurtzite phase with the lattice parameters agreed with the tabulated those.

Electronic structure of the UD3 defect in 4H and 6H SiC

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For SiC device applications it is highly desirable to achieve semi-insulating substrate material. Recently it became possible to grow bulk semi-insulating SiC by the HTCVD technique. The semi-insulating behaviour is probably due to one or several deep level defects, but a definite identification of these defects has not been possible so far. However, a series of sharp photoluminescence (PL) lines in the near infrared region is often found in such samples. These lines have been labelled UD1, UD2 and UD3, and the corresponding defects are likely candidates for the semi-insulating behaviour.

The aim of this work is to provide detailed insight into the electronic structure of the ground state and the lowest lying excited states of the UD3 defect. This is achieved by a combination of PL-, PL excitation- (PLE), polarization- and Zeeman-experiments. The UD3 defect gives rise to a no-phonon (NP) PL line at low temperatures at an energy of 1.3555 eV in 4H SiC and 1.3430 eV in 6H SiC. In a magnetic field UD3 in both polytypes splits into two lines. The magnitude of this splitting is strongly angular dependent: It is largest when the magnetic field is oriented parallel to the c-axis of the crystal and basically disappears for a magnetic field orientation perpendicular to the c-axis. The splitting is observable in both PL- and PLE-experiments. In PL however there is a thermal redistribution of intensity as the temperature is varied, whereas the two lines have identical intensity at all temperatures in PLE.

At zero magnetic field the lines are completely polarized $\vec{E} \perp c$ -axis.

In PLE experiments additional lines at a few meV above UD3 are found in the 4H polytype. The ones closest to the UD3 line are almost as sharp as UD3 itself and are attributed to transitions between the ground state and additional excited states with higher energies. Additional evidence for this is provided by the fact that the lowest lying additional lines can even be found in PL experiments at elevated temperatures when the corresponding levels are thermally populated.

The experimental findings can be consistently explained assuming the following electronic structure: The ground state is an orbital and spin singlet 1A_1 . Above that there is an orbital doublet 1E_2 . The transition between these gives rise to UD3. The g-value of 1E_2 -states is typically highly anisotropic, which explains the strong angular dependence of the Zeeman splitting. In addition only transitions with $\vec{E} \perp c$ -axis are allowed between A_1 and E_2 states. At energies above the E_2 state at least two additional singlet states have been found.

Possible candidates of the defect will be discussed based on the experimental findings.

Fabrication of 4H-SiC planar MESFETs having low contact resistance

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4H-SiC MESFETs were fabricated using high-density ion implantation to get low ohmic contact resistance without recess gate etching and contact annealing. The superior physical properties make SiC a very promising material for high power and high frequency devices especially for microwave power MESFETs. SiC MESFETs have typically had a recess-etched structure of gate active layer with a high-doped epitaxial layer for source and drain ohmic contact. The dry etching, however, leads to the degradation of device performance with the inferior gate Schottky characteristics due to the induced plasma damage in the near-surface region. Moreover, the inter-diffusion and the reaction between metal and SiC during contact annealing causes various problems such as the remaining-carbon. The ohmic contact resistance is somewhat high in the order of $10^{-4} \sim 10^{-5} \Omega\text{cm}^2$ because the doping concentration of high-doped layer of about 10^{19}cm^{-3} is not sufficient for the field-emission tunneling.

The fabrication process included mesa etching, P⁺ ion implantation and activation, formation of ohmic contacts, definition of gate contact and formation of pad. The structure of wafer from Cree Inc. consisted of n-type substrate, p-type buffer layer ($N_A=9.0 \times 10^{15} \text{cm}^{-3}$) and n-type channel layer having a thickness of $0.4 \mu\text{m}$ ($N_D=1.7 \times 10^{17} \text{cm}^{-3}$) (Fig. 1). The gate length was from $2 \mu\text{m}$ to $10 \mu\text{m}$ and the gate width was $100 \mu\text{m}$ and $500 \mu\text{m}$. Ohmic contacts were formed using Al without annealing, which means after the activation annealing of ion implantation, all processes were run at room temperature.

Fig. 2 shows the I_{ds} - V_{ds} characteristics of a fabricated MESFET. The pinch-off voltage, the saturation drain current and the transconductance were 30 V, 415 mA/mm, and 19.3 mS/mm, respectively. Very low contact resistance of $4.8 \times 10^{-6} \Omega\text{cm}^2$ was estimated from TLM measurement, which indicate the non-annealed Al ohmic contact can be applied for the device fabrication.

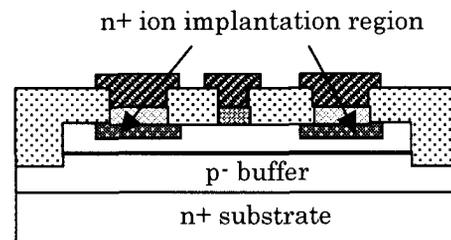


Fig. 1. Cross-sectional view of MESFET

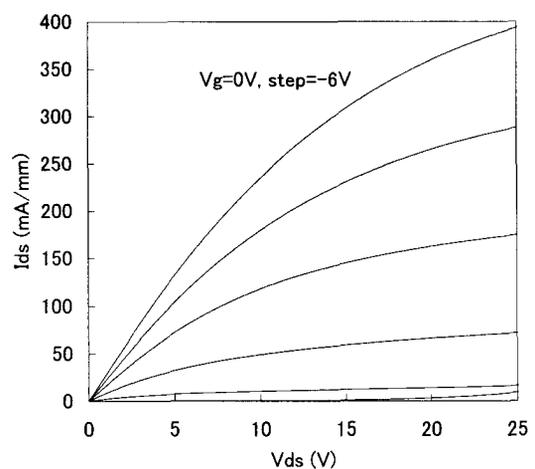


Fig. 2. DC characteristics of MESFET with $2 \mu\text{m}$ gate length and $500 \mu\text{m}$ gate width

Homoepitaxial growth of 4H-SiC thin film below 1000°C by microwave plasma chemical vapor deposition

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High temperature (around 1500°C) of homoepitaxial SiC film growth limits the variety of the SiC device process. Our goal is to achieve high-quality homoepitaxial α -SiC film growth below 1000°C by microwave plasma chemical vapor deposition (μ PCVD) for the purpose of providing more flexibility in the SiC device process, such as epitaxial growth using SiC on insulator (SiCOI) substrates, selective epitaxial growth by use of oxide or nitride mask and so on. To our knowledge, there are no papers reporting about homoepitaxial growth of α -SiC using PCVD.

SiC films were grown on 8° off-axis 4H-SiC(0001) substrates at temperature of 970°C and microwave power of 1300W without intentional doping. Mixture source gases of CH₄ and SiH₄ were used with H₂ carrier gas. The surface morphology and crystallinity of the obtained films was characterized by atomic force microscopy (AFM) and reflection high-energy electron diffraction (RHEED), respectively. The C/Si ratio was a very important factor for fabrication of high-quality films. Extremely high C/Si ratio (C/Si=175) in comparison with that used in conventional CVD technique was required to obtain smooth and single crystalline films.

The polytype of obtained films was confirmed by confocal microprobe Raman scattering spectroscopy. Figure 1 shows the Raman scattering spectra from the ~200nm thickness SiC film grown at C/Si ratio of 175 for 10h. By focusing probe laser at surface and substrate, we distinguished the signals from the grown film and the substrate. It is known that the LO phonon-plasmon coupled (LOPC) peak becomes broader and shifts to higher frequency with increasing the free carrier density n [1]. Since the substrate was highly doped n-type 4H-SiC, the Raman line of LOPC mode was very broad as shown in Fig. 1 (a). On the other hand, in a spectrum from the film surface (Fig. 1 (b)), a sharp line (964cm⁻¹) corresponding to the LO mode of pure 4H-SiC was observed with the broad LOPC line from the substrate. These results indicate that homoepitaxial growth of 4H-SiC have been attained below 1000°C.

[1] S. Nakashima *et al.*, Phys. Stat. Sol. (a) **162**, 39 (1997)

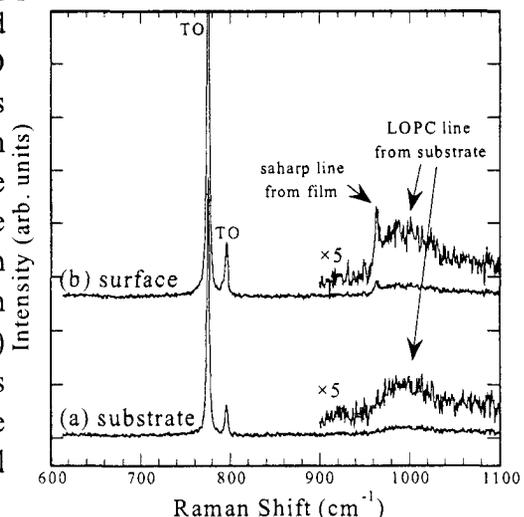


Fig. 1 Raman scattering spectra

Reduced micropipe density in boule-derived 6H-SiC substrates via H etching of seed crystals

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The effect of hydrogen etching of 6H-SiC Si(0001) on-axis SiC seed surfaces prior to crystal growth has been investigated. The most common method for producing SiC substrate wafers is to place a SiC seed in a closed graphite container and then deposit SiC vapor species onto the seed from a heated SiC source. Four quarters of the 2" seed were prepared for boule growth with each quarter prepared using various treatments. A photograph of the seeds investigated is shown in Fig. 1 (left) along with the resulting substrates (right). Hydrogen etching of the seeds was performed for 30 min. at 1600°C in a cold-wall CVD reactor to reduce seed crystal surface and subsurface damage. Boule growth was then conducted in an inductively heated PVT furnace and the boule sliced into wafers and polished. The micropipe density (MPD) was then measured using differential interference optical microscopy. For a conservative analysis the MPD for each wafer quarter were averaged and a statistical analysis performed to ensure independent samples. Using a 95% confidence criteria hydrogen etching of the seed appeared to reduce the MPD in the crystal by about $24.5 \pm 19.4\%$. Fig. 2 is a histogram of the MPD for seeds etched with hydrogen and non-hydrogen etched.

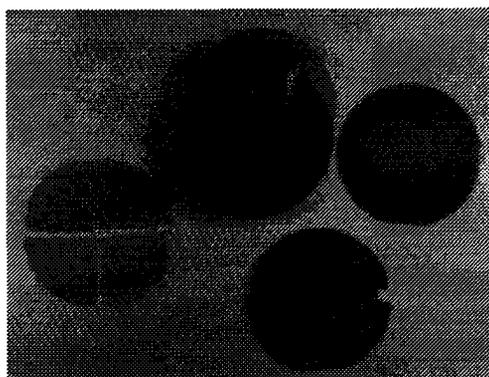


Fig. 1 Photo of tiled seeds (left) and resulting boule-derived substrates (right). 4 boules prepared in this study.

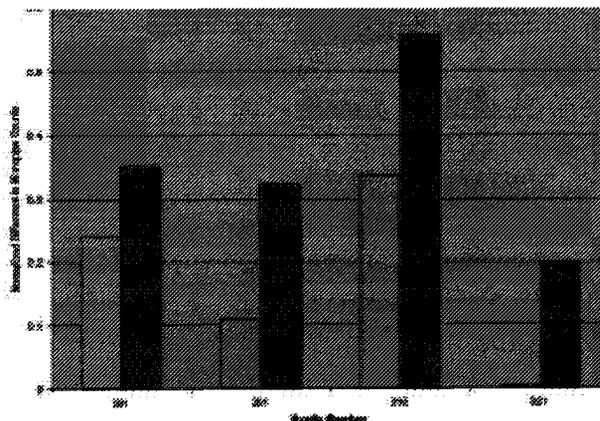


Fig. 2 MPD in boules grown using H-etched (light) and non-etched (dark) seed crystals. MPD reduced by ~ 25% with H etching.

X-ray photoelectron spectroscopy studies of post oxidation process effects on oxide/SiC interfaces

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SiC-MOSFETs have some problems to be solved before practical use, such as their low channel mobilities and higher on-resistances than those predicted. It has been reported^[1] that high interface trap density and high oxide-trapped charges of SiC MOS structures, which are estimated by *C-V* measurements, are concerned with the inferior properties of SiC MOSFETs. Also, it has been reported that some post oxidation processes, such as re-oxidation^[2], have improved their *C-V* characteristics. We have reported that,^[3] in the results of XPS measurements for slope shaped oxide films, several photoemission peaks corresponding to other bonding states than Si-C and Si-O bonds were observed in the oxide/SiC interfaces. In this report, we try to explore the changes of interfacial structures by post oxidation processes in terms of bonding states. We also reveal the reasons for the improvement of *C-V* characteristics by these processes.

6H-SiC homo-epilayers, 5 μm in thickness and $5 \times 10^{15} \text{ cm}^{-3}$ in carrier concentration (n-type) (Cree, Inc.), were used for the measurements. The (0001) Si faces of SiC epilayers were oxidized in a pure O₂ flow at 1100 °C for 3h. After the oxidation ceased, one of the samples was cooled down immediately ((a) quench), another one was post-oxidation-annealed in Ar gas atmosphere at 1150 °C for 3h ((b) Ar POA), and the last one was re-oxidized at 950 °C for 3h ((c) Re-oxi.) The three specimens were immersed gradually into buffered hydrofluoric acid at a constant speed to etch the oxide layers at an angle. The measuring point (1 mm in diameter) of XPS was scanned along the slope of the samples. Figure 1 shows the photoelectron spectra of C1s core levels as a function of oxide thickness. It was found that the number of C-O bonds and C⁻ bonds decrease with Ar POA and wet re-oxidation, respectively. C⁻ bonds are probably originated from a dissociation of C-Si bond. We also discuss the influence of C⁻ bonds and C-O bonds, in addition Si-Si bonds and Si-O-C bonds observed in Si2p, with respect to the electric properties of MOSFETs.

This work was partly performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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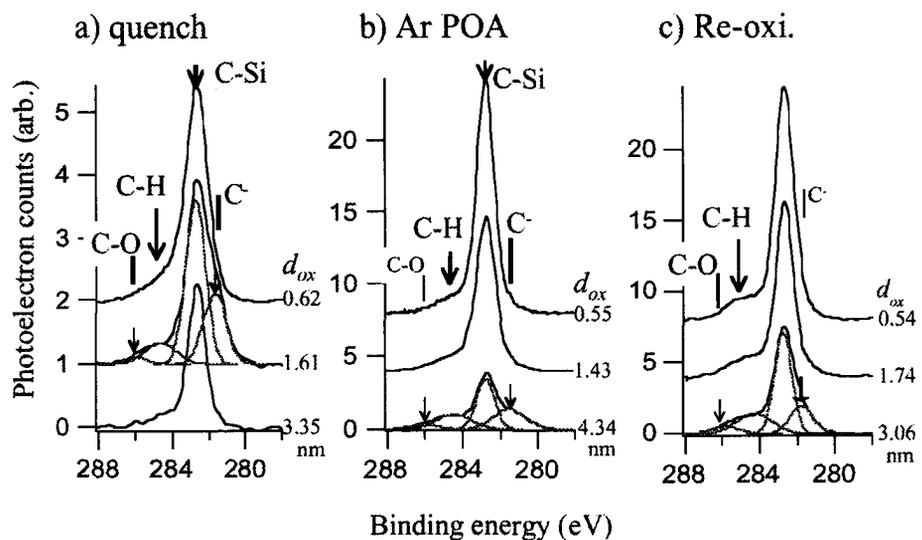


Fig.1 Photoelectron spectra of C1s core levels as a function of oxide

Replication of Defects from 4H-SiC Wafer to Epitaxial Layer

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The replication of defects such as screw dislocation and basal plane dislocation from 4H-SiC wafer to the epilayer was investigated by reflection X-ray topography. The Berg-Barrett geometry was employed using $\text{CuK}\alpha$ radiation and the \mathbf{g} vector was $11\bar{2}8$. The incident angle to the surface of samples was 4.9 deg. and the absorption depth is $6.0\ \mu\text{m}$ under these conditions.

Figure 1 shows the topographs from (a) 4H-SiC epilayer with a thickness of $30\ \mu\text{m}$ and (b) 4H-SiC wafer on which the previous epilayer was grown. The topograph (b) was recorded before the growth of epilayer. The screw dislocations marked A are observed in both topographs at the same position. They are perfectly replicated from the wafer to the epilayer with the strained area around them. Basal plane dislocations form a network in the wafer, as marked B in topograph (b). Most of them are not replicated to the epilayer but a few are observed at same position of both topographs as marked C. The defects marked D and marked E are observed only in the epilayer. These defects are produced during the growth. The formers are needle-like and elongated to the off orientation. The topographs from epilayer depend on its thickness. Details will be shown at the conference.

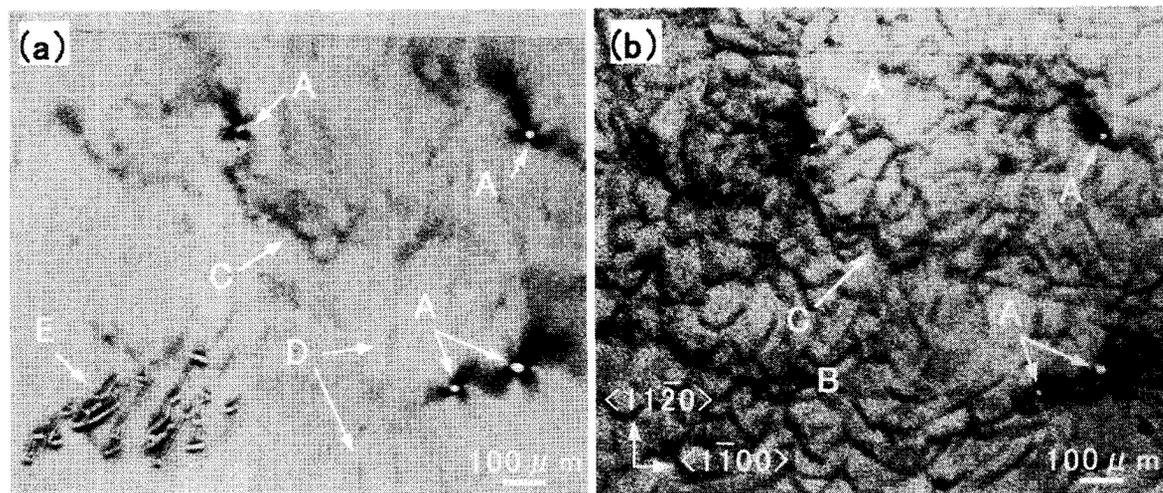


Fig. 1 Berg-Barrett topographs from (a) 4H-SiC epilayer and (b) the wafer on which the previous epilayer was grown. $\text{CuK}\alpha$ radiation. $\mathbf{g}=11\bar{2}8$

Acknowledgement This work was performed under the management of FED as a part of the METI Project (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

Simulation of High-Temperature SiC Epitaxial Growth Using Vertical, Quasi-Hot-Wall CVD Reactor

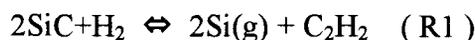
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High-voltage SiC power devices use thick epitaxial layers so that achieving high growth rate is an important issue. It is considered that higher growth temperature might be advantageous for growing high-quality epilayers with fast growth rate. Kushibe et al., However, reported that the growth rate at high temperature rather decreases with increasing temperature because of H₂ etching of SiC^[1]. We investigated the epitaxial growth model at high temperature by using computer simulation based on the competing reactions of H₂ etching and deposition taking account of the experimental data.

A vertical, quasi-hot-wall CVD reactor was used for experiments. The 2-dimensional axisymmetric model was used for simulations considering the thermal and multi-component gas-phase diffusions. The source gases were SiH₄ and C₃H₈, and carrier gas was H₂. The competing reaction on the SiC substrate surface was assumed as follows:



The simulation indicated that the source gases are completely decomposed to Si(g) and C₂H₂ near the SiC substrate surface, and Si(g) and C₂H₂ are also generated by the H₂ etching reaction at high temperatures (≥1640°C). As the result, it is considered that epitaxial growth rate is dominated by the three major reaction paths at high temperature, namely (i)SiC etching by H₂, (ii)re-deposition of the byproducts of etching, and (iii)deposition by source gases. The experimental data were well explained by this competing growth model.

Reference: [1] K. Kushibe et al., Proc. of ICSCRM '99 (1999) 470.

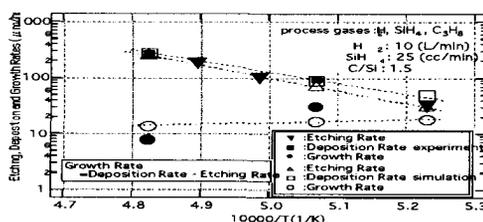


Fig.1 Temperature dependence of etching, deposition and growth rates.

Acknowledgement This work was performed under the management of FED as a part of the METI Project (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

Homoepitaxial growth of cubic silicon carbide by sublimation epitaxy

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Cubic silicon carbide has wider band gap than silicon and gallium arsenid and higher electron mobility than hexagonal silicon carbide. Therefore, cubic silicon carbide has an enough potential for low loss, high power and high frequency devices. In this work, crystal growth of cubic silicon carbide was carried out by sublimation method, especially sublimation epitaxy on cubic silicon carbide substrates.

Generally, cubic silicon carbide is grown on silicon substrates by chemical vapor deposition (CVD) [1]. However, the growth rate in CVD is very low. In this study, sublimation epitaxy was used in order to obtain thick and high quality cubic silicon carbide. In sublimation epitaxy, high quality epitaxial layers can be obtained with high growth rate (over 100 $\mu\text{m}/\text{h}$) [2].

Crystal growth was carried out on cubic silicon carbide substrates. These substrates were grown on silicon or silicon carbide substrates by CVD. The growth temperature and the growth pressure during the homoepitaxial growth process were 1850 $^{\circ}\text{C}$ and 30Pa, respectively. Crystal growth proceeded in argon atmosphere. In these conditions, the growth rate was about 50 $\mu\text{m}/\text{h}$.

Fig.1 shows Raman spectra of the substrate and the grown layer. The thickness of the substrate and the grown layer were about 20 μm and about 300 μm , respectively. 3C-SiC LO phonon peak near 974 cm^{-1} [1] is observed at both spectra. Therefore, it is considered that the cubic silicon carbide layer is grown on the cubic silicon carbide substrate. The surface of the grown layer was smoother than that of the substrate and anti phase boundary (APB) density was lower than the substrate.

In order to characterize grown layers, Raman scattering and X-ray diffraction were used. Moreover, the electrical property of the film and characteristics of Schottky diode will be discussed.

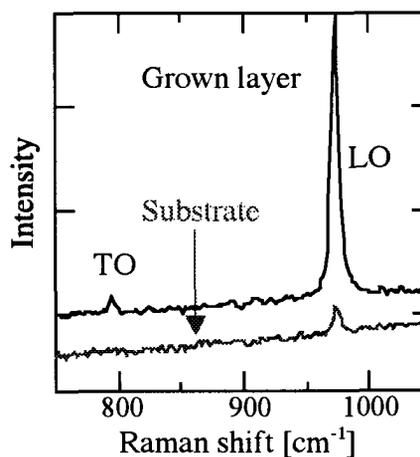


Fig.1 Raman spectra of the substrate and the grown layer.

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[2] T. Furusho, S. Ohshima and S. Nishino, Materials Science Forum **353-356** (2001) p.73.

Electron-irradiation-induced amorphization in 6H-SiC by 300 keV transmission electron microscopy equipped with a field-emission gun

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Irradiation with energetic particles is an important technique to develop new functional materials. It is necessary to elucidate the fundamental radiation effects in SiC to obtain or maintain desirable materials properties for device production. One of the most important parameters for describing radiation damage is the threshold displacement energy (E_d), which is defined as the minimum kinetic energy to create a stable Frenkel pair. Much effort has been devoted to determine E_d of SiC, but the values estimated experimentally are considerably scattered over nearly an order of magnitude. In this study, we performed electron irradiation into 6H-SiC using *in-situ* transmission electron microscopy (TEM).

Single crystalline wafers of 6H-SiC (Cree, Inc.) were fabricated into samples appropriate for TEM study. Electron-irradiation experiments were performed at room temperature using JEOL JEM-3000F with incident electron energy of 300 keV. This facility is equipped with a field-emission gun as an electron source whose electron flux ($\sim 5 \times 10^4$ A/cm²) is larger than conventional LaB₆ filament (~ 20 A/cm²).

High-resolution TEM observations and electron diffraction experiments indicated that the electron-irradiated area is successfully amorphized, though the present irradiation conditions are beyond those required to induce a crystal-to-amorphous phase transformation (the incident electron energy of >750 keV and the temperature of <290 K) [1]. The E_d calculated assuming the incident electron energy of 300 keV turned out to be ~ 30 eV for silicon. The E_d obtained here is quite similar with that in experimental and theoretical reports: 30-35 eV by Rutherford backscattering technique [2] and 35 eV by molecular-dynamics calculation [3]. Because of high-electron flux of field-emission gun used here, it is considered that the damage-producing rate dominates over the recovery rate in the electron-irradiated area. We will also report an example of nano-fabrication of SiC using electron-beam-irradiation.

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Observation of 2 inch SiC wafer by SWBXT at SPring-8

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SiC bulk crystal made by sublimation method has a lot of defects and stress fields. These defects affect performance of device operation. So we must investigate and decrease defects and stress fields. X-ray topography is useful tool to observe defects and stress fields in a wafer. By using SWBXT (Synchrotron White Beam X-ray Topography), we observed the defects using facilities at SPring-8 (BL28B2). SR beam at SPring-8 has much merit, such as 8GeV electron beam energy, ultra-bright, highly directional, linearly polarized and so on. So, we tried to observe 2inch SiC wafers and discussed about defects more detail. We prepared 2 inch (0001) and (11-20) SiC wafers, which were made by sublimation method and measured by transmission and reflection mode. Fig.1 shows the topography of transmission mode. The

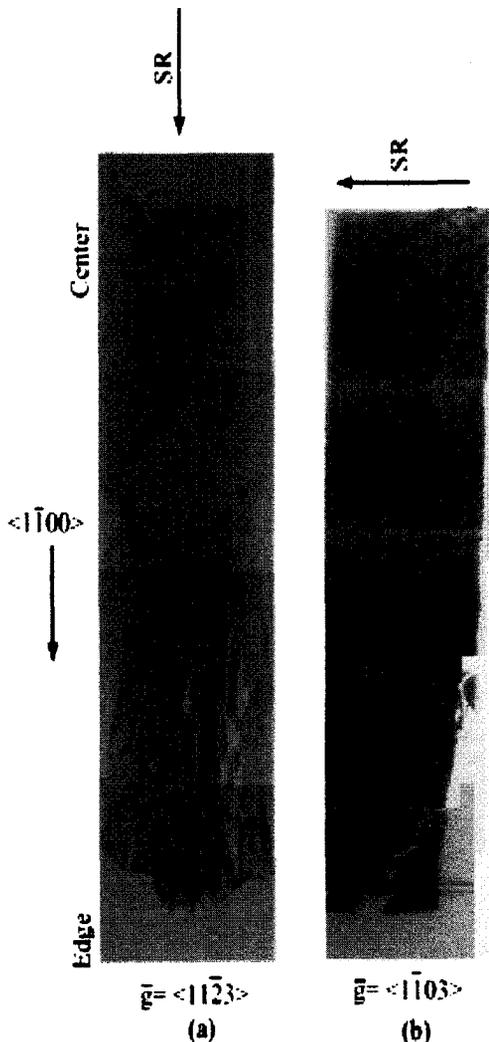


Fig.1 X-ray topography of (0001) 6H-SiC (transmission mode)

directions of incident beam of Fig.1 (a) and (b) were $\langle 1-100 \rangle$ and $\langle 11-20 \rangle$ and diffracted planes were (11-23) and (1-103), respectively. Fig.1 (a) and (b) were observed at same area. But the images were different each other. From these images, Fig.1 (b) has more fine stripes than Fig.1 (a). Fig.2 shows these fine stripes. The contrast in Fig.1 (a) corresponded to the sub-grain boundaries, whose Burgers vector was $\langle 11-20 \rangle$. And many fine stripes in fig.1 (b) were small defects or stress fields whose Burgers vector was $\langle 1-100 \rangle$ direction.

The defects were created by releasing the stress fields. But in the crystal, residual stress and elastic stress still exist, probably. And these stress fields appeared as small defects.

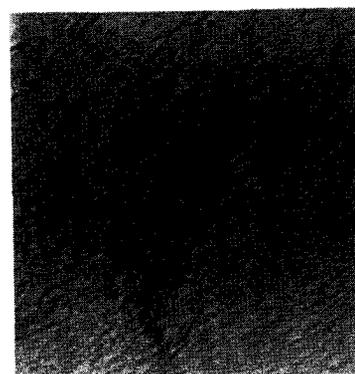


Fig.2 Enlarged image of Fig.1 (b)

Adsorbate Effects of the Surface Structure of 6H-SiC(0001) $\sqrt{3}\times\sqrt{3}$ R30°

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Surface structures of 6H-SiC(0001) $\sqrt{3}\times\sqrt{3}$ R30° surfaces have been studied by rocking curves of reflection high energy electron diffraction (RHEED) intensities and Auger electron spectroscopy (AES).

Two types of $\sqrt{3}\times\sqrt{3}$ surfaces, $\sqrt{3}\times\sqrt{3}$ -Si (oxygen free) and $\sqrt{3}\times\sqrt{3}$ -C surfaces (oxygen adsorbed), were observed in a series of an annealing process. The $\sqrt{3}\times\sqrt{3}$ -Si surface was obtained by annealing the Si pre-deposited specimen in a Si flux for 3 min at 1045°C. After leaving the $\sqrt{3}\times\sqrt{3}$ surface in a UHV chamber for 23 h, the RHEED pattern showed 1×1 periodicity, which turned into the $\sqrt{3}\times\sqrt{3}$ -C surface by annealing the 1×1 surface for 30 sec at 810°C. Rocking curves and AES spectra from the two $\sqrt{3}\times\sqrt{3}$ surfaces clearly show that the two $\sqrt{3}\times\sqrt{3}$ surfaces are structurally different. Peak-to-peak intensity ratios of Si LVV to C KLL peaks are 2.2 and 0.92 for the $\sqrt{3}\times\sqrt{3}$ -Si and $\sqrt{3}\times\sqrt{3}$ -C surfaces, respectively. The $\sqrt{3}\times\sqrt{3}$ -C surface transformed into the $\sqrt{3}\times\sqrt{3}$ -Si surface again by further annealing for 30 sec at 940°C. Rocking curves from the surface structures of the two $\sqrt{3}\times\sqrt{3}$ surfaces have been analyzed by RHEED dynamical calculations based on multi-slice transfer matrix method. In conclusion, the $\sqrt{3}\times\sqrt{3}$ -Si surface is determined to be terminated with Si single-adatoms on T4 or H3 sites of the bulk surface. The two sites are not distinguished from this analysis because of the poly-type structure surface. From a preliminary analysis, the $\sqrt{3}\times\sqrt{3}$ -C surface contains C trimer structure.

In order to find what causes the phase transition from the $\sqrt{3}\times\sqrt{3}$ -Si to the $\sqrt{3}\times\sqrt{3}$ -C phases, hydrogen gas and oxygen gas are exposed to the $\sqrt{3}\times\sqrt{3}$ -Si surface at room temperature, then the samples are annealed to 700°C and 790°C in UHV, respectively. In the case of the hydrogen-treated $\sqrt{3}\times\sqrt{3}$, the RHEED rocking curves and the Auger spectrum show good agreement with the $\sqrt{3}\times\sqrt{3}$ -C surface formed by annealing in UHV as mentioned above. Therefore, it is reasonable to suppose that the rearrangement of the $\sqrt{3}\times\sqrt{3}$ surface in UHV is caused by adsorption of hydrogen on the $\sqrt{3}\times\sqrt{3}$ -Si surface.

Annealing Kinetics of the implantation-induced amorphous layer in 6H-SiC(0001)

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We reported that the amorphous layer on (11-00) and (112-0) oriented SiC can recrystallized to the original polytype structure by annealing below 1000 °C. However, there is a few study about the annealing kinetics of the implantation-induced amorphous layer in (0001)-oriented SiC. In this study, we report the annealing kinetics for the Ar ion implantation-induced amorphous layer of (0001)-oriented 6H-SiC in annealing temperature below 1000 °C.

Figure 1 shows the image of the cross-sectional electron transmission microscopy taken from 6H-SiC, implanted with 100 keV Ar at a dose of $2 \times 10^{15}/\text{cm}^2$ at room temperature, before and after annealing at 950 °C for 1 hr. In the as-implanted sample, the 120-nm thick amorphous layer can be observed. On the other hand, in the annealed sample, it is found that the amorphous layer is recrystallized to 3C-SiC, which can be divided into two regions indicated as I and II in figure. Regions I and II contain a large amount of micro-3C SiC crystals and a small amount of relatively large 3C-SiC crystals, respectively. It is suggested that the regrowth mechanism was changed during the annealing. Figure 2 shows the annealing time dependence of the thickness of the regrown 3C-SiC from 320 nm-thick amorphous layer. At the first stage, the regrowth rate is very small and is estimated to be 0.044 nm/min at 800 °C, which is 2 order of magnitude smaller than the case of (11-00)-oriented 6H-SiC. This slow regrowth corresponds to the growth of micro 3C-SiC crystals (see Region I in fig. 1). After regrowth of 3C-SiC layer with a thickness of about 60 nm, the regrowth rate is increased to 10 times faster than the first stage, which is connected to the growth of the large 3C-SiC crystals (Region II in fig.1). The regrowth rate in

the second stage is estimated to be 0.35 nm/min at 800 °C. The activation energy of the regrowth of 3C-SiC is estimated to be 3.4 eV for both first and second stages, which is in good agreement with those of (11-00) and (112-0) oriented 6H-SiC.

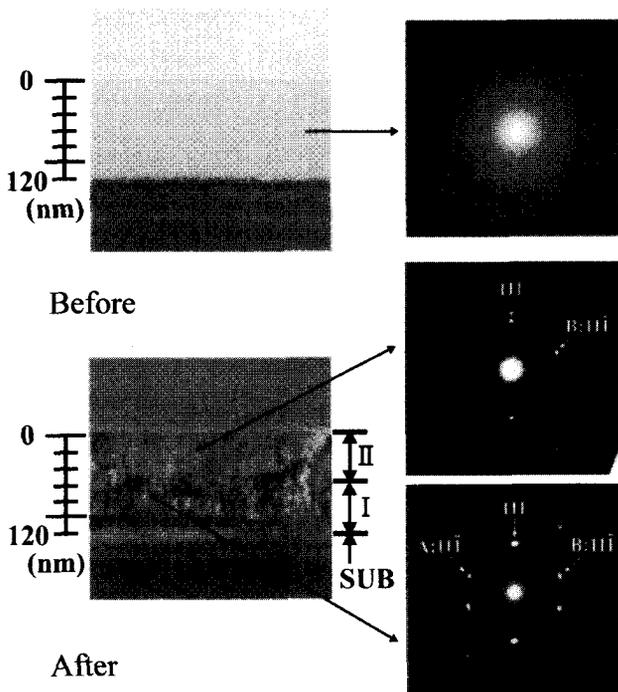


Figure 1

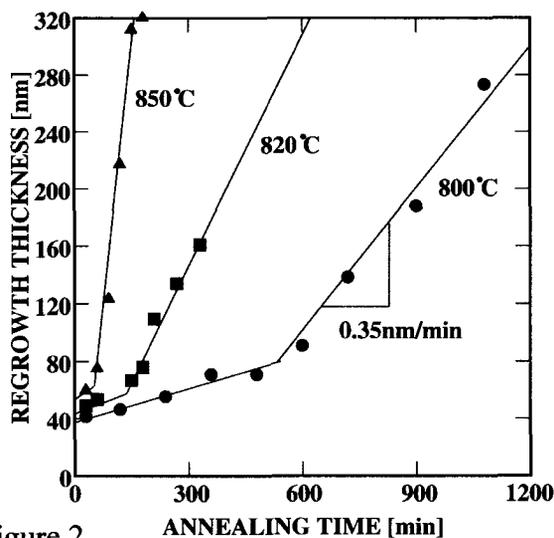


Figure 2

4H-SiC Schottky diodes with high on/off current ratio

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Silicon carbide Schottky Diodes (SD) with moderate blocking voltage (~300-1200V) are of great interest due to their high switching speed compared to Si PiN diodes. However, the on/off current ratio at fixed forward and reverse biases does not always compare as favourably. In this paper, we describe the fabrication and characterisation of SiC SD with moderate blocking voltage, having reduced reverse current and improved on/off current ratio.

The reverse current in a SiC SD depends on the contact metal barrier height and the applied voltage. Furthermore, the current under reverse bias is defined mainly by current flow through the contact periphery, where crowding increases the electric field. Conversely, the electrical characteristics of the diode under forward bias, are defined by the current flow through the whole diode area. Hence, the reverse current may be decreased with no increase in forward voltage drop if a thin strip of metal with higher barrier (e.g. Ni, 1.6 eV) surrounds the contact consisting of the metal with lower barrier height (e.g. Ti, 1.2 eV).

Commercial 4H-SiC $n-n^+$ wafers ($3 \cdot 10^{15} \text{cm}^{-3}$; 10 μm) were used to fabricate these diodes. All metals were deposited with no sample heating. Nickel, 100 nm thick, was deposited on the back side of the wafer and annealed at 1100°C to form the ohmic contact. To form the SD, titanium (4-15 nm thick) and nickel (100-150 nm) were deposited consecutively. After contact geometry definition by contact

photolithography and chemical etching of Ni (Fig.1b), the Ti was etched selectively to nickel (Fig.1c) in liquid etchant. The time of overetching defined the width of the Ni strip. During specimen drying, the Ni film was bent by surface tension forces forming tight contact to SiC (Fig. 1d). Finally, the Schottky contact was formed by annealing at 450-650°C for 60 min.

The diodes had a breakdown voltage of about 750 V, with a barrier height in forward bias of 1.2 V, (as observed for Ti SD) whilst the reverse current was similar to Ni SD (Fig. 2). They had an on/off current ratio at 1V/500V of about $5 \cdot 10^8$. This value exceeds the on/off ratio of Ti/SiC and Ni/SiC SD fabricated on the same epitaxial wafer and exceeds those published in the literature for SD with moderate breakdown voltage. To verify the formation of Ni contact strip around Ti Schottky contact, it was decorated as indicated in Fig. 1e-f. A SEM picture of the decorated edge strip is shown in Fig. 3. Full details of the diode fabrication and electrical characterisation will be given in the final paper.

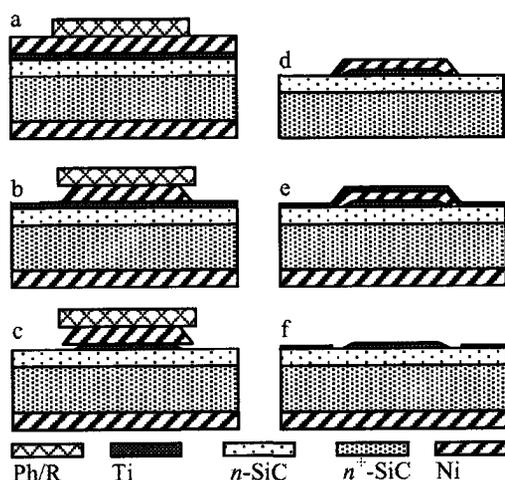


Fig. 1. Device processing flow map for (a - d) SD fabrication and (e - f) edge metal strip decoration.

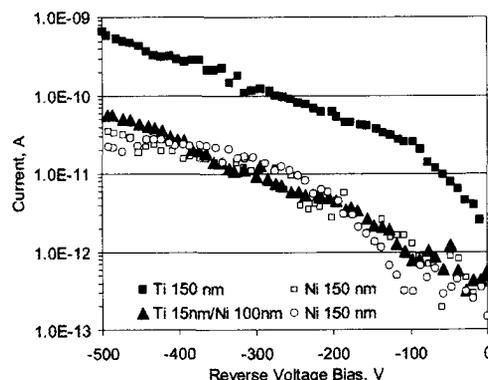


Fig. 2. Reverse currents of Ti, Ni, and Ti/Ni SD on 4H-SiC measured at room temperature. (SD diameter is 400 μm).

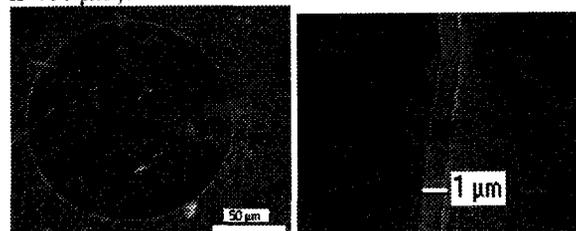


Fig. 3. SEM pictures of decorated edge metal strip.

Characteristics of MESFETs made by Ion-implantation in Bulk Semi-insulating 4H-SiCS. Mitra¹, M. V. Rao^{1*}, N. Papanicolaou² and K. Jones^{3*}¹ Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030, USA² Naval Research Laboratory, Washington DC 20375, USA³ Army Research Laboratory, Adelphi, MD 20783-1197, USA***Corresponding Author, 4400 University Drive, Fairfax, VA 22030, USA; Ph: 703-9931612, Fax: 703-9931601, Email: rmulpuri@gmu.edu, Presenting Author**

In this work, I-V, C-V and DLTS characteristics of fully ion-implanted n-channel Metal-Semiconductor Field-Effect-Transistors (MESFETs) made in semi-insulating (SI) bulk 4H-SiC with $W/L = 280 \mu\text{m} / 2 \mu\text{m}$ are studied. In order to create the source/drain and the channel regions of the MESFET, nitrogen implantations were performed to a depth of 300 nm at room temperature to volumetric concentrations of $2 \times 10^{19} \text{ cm}^{-3}$ and $6 \times 10^{17} \text{ cm}^{-3}$, respectively. To activate the implants, annealing was performed for 15 minutes at 1450°C in an argon ambient using an AlN encapsulation. Ohmic contacts to the source/drain areas were formed by e-beam evaporation and lift-off of Ni (100 nm), followed by a $1200^\circ\text{C} / 3$ minute anneal in vacuum. Al Schottky gate metallization (~ 100 nm thickness) was performed by e-beam evaporation. From capacitance-voltage (C-V) measurements taken before forming the channel recess, the channel substitutional dopant concentration was found to be $3 \times 10^{17} \text{ cm}^{-3}$, which represents a 50% activation of the implanted nitrogen species in this region. Van der Pauw Hall measurements of on-wafer test patterns showed a room temperature volumetric carrier concentration of $2 \times 10^{17} \text{ cm}^{-3}$, with a bulk electron mobility of $240 \text{ cm}^2 / \text{V}\cdot\text{s}$. The pinch-off voltage and the saturation drain current (I_{dss}) of the MESFETs are found to be -18 V and $\sim 30 \text{ mA}$, respectively. The drain conductance (g_d) and the mutual transconductance (g_m) calculated from the MESFET's I_D - V_{DS} - V_{GS} curves are 7.9 mS and 5.4 mS , respectively. A poor source/drain ohmic contact resistance of $\sim 10^{-2} \Omega\cdot\text{cm}^2$ is believed to be partially responsible for these low conductance values. The MESFETs showed stable device characteristics over the temperature range 25°C - 350°C . Due to the poor ohmic contact resistance value, the channel carrier mobility extrapolated from the g_d and g_m values is about 5 times smaller than the bulk Hall carrier mobility. The residual implant lattice damage at the interface is also partially responsible for the low g_m and g_d values. To investigate the implant lattice damage induced traps in the MESFET structure, we performed Deep Level Transient Spectroscopy (DLTS) measurements on the channel/SI substrate interface in the temperature range from 200K to 550K. A Schottky gate reverse bias voltage of $\sim -10\text{V}$ was applied to push the depletion region into the vicinity of the nitrogen implanted channel and the SI substrate interface. With a proper choice of the rate window, several traps were detected at the channel/ substrate interface at 0.51 eV, 0.6 eV, 0.68 eV, 0.768 eV and 0.89 eV above the valence band edge (E_V) at relatively high concentration ($N_t \sim 0.01 N_s$, where N_s is the net carrier concentration). The trap located at $E_V + 0.51 \text{ eV}$ is believed to be due to a point defect created by nitrogen implantation, and the trap at $E_V + 0.6 \text{ eV}$ can be related to the deep acceptor level introduced by the V dopant in the semi-insulating material. Origins of the other traps are unknown at this time. The normalized amplitude of all peaks decreased linearly with decreasing reverse bias on the Schottky gate, indicating that the defect concentration decreases at distances further from the channel/substrate interface. The implant defect related traps might have also contributed to the poor effective carrier mobility in these MESFET devices. Optimization of the implant/annealing temperatures and source/drain ohmic contact formation parameters are expected to yield improved device performance to make ion-implantation in SI substrates an attractive doping process for SiC device fabrication.

Epitaxial growth of (11-20) 4H-SiC using substrate grown in the [11-20] direction

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Homoepitaxial growth on 4H-SiC (11-20) substrate grown in the [11-20] direction by sublimation method has been investigated by low-pressure, hot - wall type CVD reactor with SiH₄ – C₃H₈ – H₂ – system. Typical gas flow rate of H₂, SiH₄ and C₃H₈ were 40 slm, 6.67 sccm and 3.33 sccm, respectively. The growth temperature and the reactor pressure were 1600°C and 250 mbar, respectively.

The surface of epilayers exhibited smooth and no defects morphology with the surface roughness (Rms) of 0.14nm in 16µm square. This roughness was smaller than that of epilayer grown on conventional (11-20) substrate grown in the [0001] direction. By KOH etching experiment, it was found that the stacking fault in the substrate was replicated to the epilayer and the density of the stacking faults was in the order of 10² cm⁻¹. The surface morphology was not affected by the stacking faults of this density range.

Figure 1 shows the x-ray rocking curve at 11-20 reflection peak obtained from 5 µm-thick epilayer. This epilayer exhibited the sharp and single diffraction peak in both x-ray incident directions of parallel and perpendicular to c-axis. The FWHM of each peak was 13.7 and 15 arcsec respectively. In our previous study, epilayers grown on conventional (11-20) substrate exhibited splitting and broadening (FWHM=477 arcsec) of the diffraction peak in the incident direction of perpendicular to c-axis [1]. The crystalline quality of (11-20) epilayers is improved by using the substrate grown in the [11-20] direction.

The characteristics of MOS structure fabricated on this epilayer will be also presented in this conference.

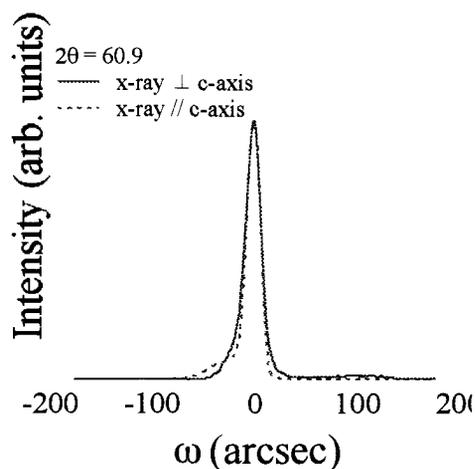


Figure 1. X-ray rocking curve of ω scan

Acknowledgement

This work was performed under the management of FED as a part of the METI Project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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Improvement of SiO₂/α-SiC interface properties by nitrogen radical treatment

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Si MOSFETs have good characteristics of fast switching and a low value of on-resistance (R_{on}) reduced year by year. The R_{on} of Si MOSFETs has almost reached a theoretical limit originated from material properties of Si. So it is important to develop MOSFETs on SiC to achieve further reduction of R_{on} for future evolution in power electronics. However, it is difficult to fabricate high performance MOSFETs on SiC because of poor interface characteristics of SiO₂/SiC. In recent years, a number of studies have been conducted on the effect of NO annealing, which improves SiO₂/4H-SiC interface properties. In this study, we propose a new method for the improvement of SiO₂/α-SiC interface quality by irradiation of N radicals with high reactivity at low temperatures.

N-type 6H- and 4H-SiC Si(0001) face epilayers with donor concentration of 2 × 10¹⁶ cm⁻³ were used. After standard RCA cleaning, dry oxidation was performed at 1100°C for 2h followed by post oxidation annealing in Ar at 1100°C for 30min. The oxide thickness was approximately 14nm determined by accumulation capacitance in high-frequency C-V curves. In N radical treatment, N₂ gas (gas flow:1.25sccm, pressure:1~5 × 10⁻⁵Torr) was activated by RF power (13.56MHz, 230W) applied to an induction coil. Charged species, which would cause damage to the oxide film, were eliminated from N plasma with the use of ion trap electrodes. So electrically neutral N radicals were irradiated to the surface of the sample. After growing the oxide film and N radical irradiation, angle resolved XPS (ARXPS) measurement was carried out to estimate atomic components in the oxide film. MOS capacitors with gate electrode of Al were fabricated. High-frequency (1MHz) C(G)-V measurements were performed to evaluate SiO₂/α-SiC interface properties.

Fig.1 shows the SiO₂/4H-SiC interface trap density determined by the Terman method. Fig.1 extends that the N radical treatment reduced interface trap density from 6 × 10¹² cm⁻² eV⁻¹ to 4 × 10¹² cm⁻² eV⁻¹ at the Fermi energy for 4H-SiC. The reduction of interface trap density was also observed for 6H-SiC (1.3 × 10¹² cm⁻² eV⁻¹ and 5.5 × 10¹¹ cm⁻² eV⁻¹ before and after the N radical treatment, respectively). The improved property was maintained after N₂ annealing at 1050°C. From ARXPS measurement, approximately 2-4at% N atoms were incorporated into the oxide film. Fig.2 shows N1s peak area as a function of depth, which represents N distribution in the oxide film. The result indicates that most of N atoms are accumulated at the surface of SiO₂. The improvement of interface properties was assumed to be due to interface modification by introducing small quantity of N radicals reached to the SiO₂/α-SiC interface, which could not be detected by ARXPS measurement due to low sensitivity.

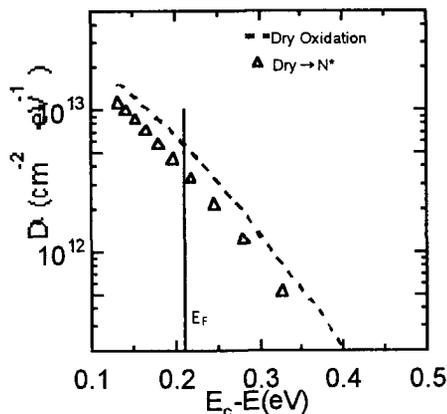


Fig.1 Energy distribution of D_{it} for n-type 4H-SiC

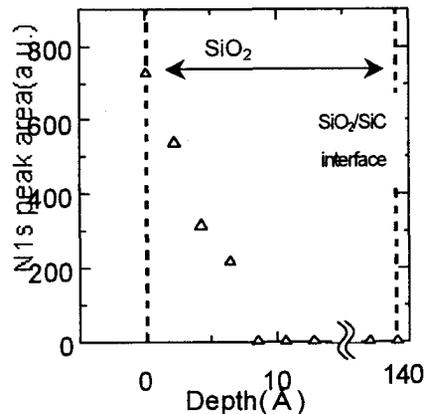


Fig.2 XPS depth profiles of N radical processed SiO₂/4H-SiC

Effects of Surface Treatments of 6H-SiC upon Metal-SiC Interfaces

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1. Introduction

Surface treatments to obtain clean and ordered surfaces of semiconductors are basic techniques. It is well known that the H terminated Si surfaces are obtained by HF treatments, and these surfaces function against chemical attacks of contaminants such as O and C, which degrade metal-Si interface quality [1]. In this study, we report on effects of surface treatments of 6H-SiC upon metal-SiC interfaces.

2. Experimental

Samples of n-type ($N_D - N_A = 8.61 \times 10^{17} / \text{cm}^3$) 6H-SiC (0001) Si-face were used in this study. In order to reduce scratches, as received samples were polished with colloidal silica before chemical treatments. To remove organic contaminations, $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ treatment at 150 °C was performed. After rinsing in deionized water, the samples were dipped in boiling HF (BoHF) at 95 °C (10 min x 3 sets) or in HF at room temperature (30 min). Some of BoHF and HF treated samples were rinsed in deionized water. The elemental composition of the surface was investigated by Auger electron spectroscopy (AES). For current-voltage (I-V) measurements, Al contacts were fabricated by thermal evaporation with a base pressure of $\sim 3 \times 10^{-7}$ Torr.

3. Results and Discussion

AES analysis indicated that the main elemental composition of the surfaces after chemical treatments was Si, C, and O atoms. The peak-to-peak height of the O *KLL* AES peak, which was normalized by the BoHF treated sample, was 1.00 (BoHF), 1.03 (BoHF+Rinse), 1.14 (HF), and 1.25 (HF+Rinse). After exposing these samples to air for 100 min, the O *KLL* peak-to-peak height changed to 1.10, 1.13, 1.25, and 1.36, respectively. From these analyses, it was found that the BoHF treatment removed O atoms from the surface and rinsing in deionized water added O atoms to the surface. In order to investigate metal-SiC interfaces, Al contacts were fabricated on the BoHF and HF+Rinse treated samples, subsequently exposed to air for 100 min. Fig. 1 shows I-V characteristics of the two samples. Significant differences were not found between two samples. We think that ohmic contacts were achieved because of gettering of O atoms to Al contacts and the sharp Al-SiC interface formation.

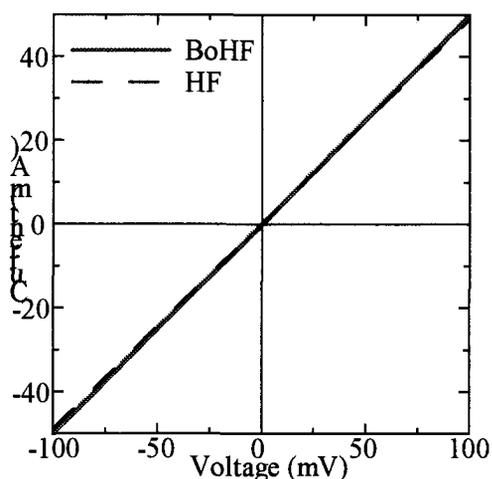


Fig. 1. I-V characteristics of the BoHF and HF+Rinse treated samples, subsequently exposed to air for 100 min.

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Hot Wall CVD Growth of 4H-SiC Using $\text{Si}_2\text{Cl}_6+\text{C}_3\text{H}_8+\text{H}_2$ System

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In these days, it has been succeeded in homoepitaxial growth of silicon carbide (SiC) by hot wall CVD using $\text{SiH}_4+\text{C}_3\text{H}_8+\text{H}_2$ system. It is desired to epitaxial growth using other safety silicon source material. And then, we have grown SiC using hexachlorodisilane (Si_2Cl_6) as a silicon source material. Si_2Cl_6 is a safe material and we already succeeded in a homoepitaxial growth of SiC by cold wall CVD. In this paper, we report homoepitaxial growth of 4H-SiC by hot wall CVD using $\text{Si}_2\text{Cl}_6+\text{C}_3\text{H}_8+\text{H}_2$ system.

A growth condition was as follows: Si_2Cl_6 flow rate is 0.3sccm~0.6sccm as a silicon source gas, C_3H_8 flow rate was 0.2sccm~0.4sccm as a carbon source gas, H_2 flow rate was 3.0slm as a carrier gas, a growth temperature were 1550°C~1650°C, a growth time were 60min~300min. 4H-SiC(0001)Si8.0°<11-20>off-axis was used for the substrate. A SiC coated separable cylindrical graphite blocks with square channel were used as a susceptor and a rf generator was 300kHz-20kW. The growth rate was about 2 μm /hour at Si_2Cl_6 flow rate was 0.3sccm.

At 1550°C growth, though the shallow round pits increased at Si-rich condition on the surface morphology of cold wall CVD, these pits increased at C-rich condition on that of hot wall CVD. In hot wall CVD the reaction gas was effectively dissociated, and generated different active chemical species from cold wall CVD. Therefore we got such a different surface morphology tendency to C/Si ratio between cold wall CVD and hot wall CVD.

At 1650°C growth, scratch like defects that array along to [1-100] direction was observed (Figure1). We think that these defects were generated to etch the surface due to be higher the substrate temperature. As the array direction of these defects is cross to a direction of step flow, these defects have any relation to step flow. Furthermore, when we took out an upper part of the susceptor block in order to minimize the radiation heating, these defects became deeper. We think that etching was enhanced due to expand a temperature gradient to between the surface and the gas flow.

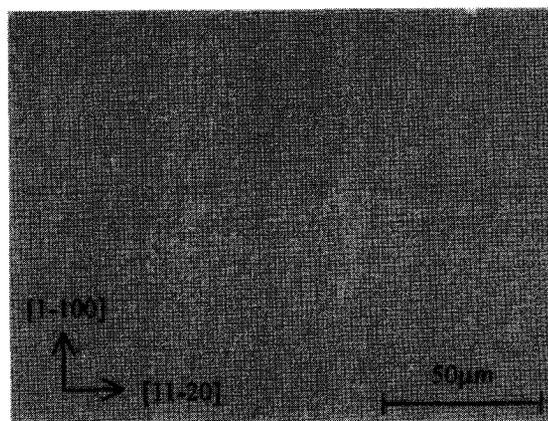


Figure1: Scratch like defects at 1650°C

Spatial mapping of the carrier concentration and mobility in SiC wafers by micro Fourier-transform infrared spectroscopy

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Silicon carbide is a promising material for applications in high-temperature, high-power, and high-frequency electronic devices due to its wide band gap, high saturated electron velocity, and high breakdown electric field. Recently, heavily doped SiC wafers have been grown in order to study the effect of heavily doping on crystal growth and defect generation. However, heavily doped SiC wafers are often not so uniform.[1] Since spatially inhomogeneous doping leads to poor quality epitaxial layers and thus to poor device performances, highly uniform doping is necessary for practical use. In the present study, we have, for the first time, tried to investigate the spatial distribution of carrier concentration and mobility in SiC wafers by micro Fourier-transform infrared (FTIR) spectroscopy. The sample used in this study was an intentionally inhomogeneous N-doped 6H-SiC wafer grown by modified Lely method. Reflectance measurements were carried out using a FTIR spectrometer at room temperature. The spatial resolution was 50 μm. Figure 1 shows typical reflectance spectra obtained from heavily doped (a) and lightly doped (b) regions. The reflectance spectra were analyzed using the dielectric function considering the contributions from phonons and plasmons.[2] From the analysis, carrier concentrations and mobilities were estimated to be $7.2 \times 10^{19} \text{ cm}^{-3}$ ($\mu = 11 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and $9.7 \times 10^{17} \text{ cm}^{-3}$ ($\mu = 73 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) for reflectance spectra shown in Fig. 1(a) and (b), respectively. Figure 2 shows the carrier concentration profile in the inhomogeneously doped SiC wafer. The measurements were made at various points along the white line in the photograph taken with a transmitted light, where dark areas correspond to heavily doped regions. Our results demonstrate that the micro FTIR is a useful and nondestructive technique to characterize the spatial distribution of carrier concentration and mobility in SiC wafers.

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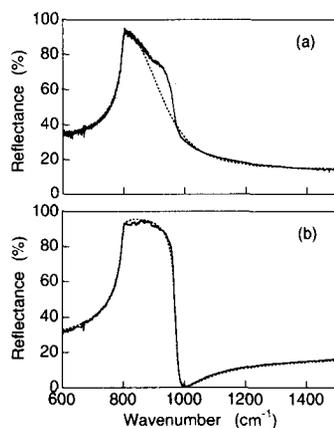


Fig. 1 Reflectance spectra of SiC.

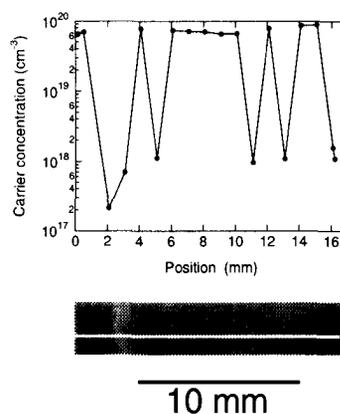


Fig. 2 Line profile of carrier concentration in SiC.

Characterization of inclusions in SiC bulk crystals grown by modified Lely method

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There have been the intense demands of a high quality silicon carbide (SiC) single crystal. However the quality still needs further improvement, because the crystals still contain a number of inclusions and defects. It is important to define the origin of the inclusions and the defects in bulk crystals to obtain a high quality bulk SiC single crystal. In this work, we have investigated two types of the inclusions, which have not been reported. They were dendrites, which consist of carbide of transition element, and the transparent inclusions with oval like shape, which were the origin of misoriented crystals.

6H-SiC bulk crystals were grown in the inductively heated furnace by modified Lely method. Commercial SiC abrasive with or without a chemical treatment were used as the source powder. The growth was performed in a high purity argon ambience at 10 Torr. The temperatures of the top and bottom of the crucible were 2200°C and 2250°C, respectively. The inclusions in the SiC bulk crystals were characterized with optical microscope and EPMA.

The dendrites were observed only in the SiC bulk crystal grown with the source powder without the chemical treatment. The components of the dendrites were measured by EPMA. The dendrites consisted of carbon, vanadium and titanium, which molar fractions were 0.41, 0.36 and 0.23, respectively. Silicon was not almost contained in the dendrites. It was considered that vanadium and titanium were incorporated into the SiC bulk crystals from the source powder and then the dendrites were generated by condensation of titanium carbide and vanadium carbide during the growth. Use of high purity source will prevent such generation of dendrite. Vanadium is used as the dopant of semi-insulating SiC single crystals. Such generation of the dendrites is a serious matter in the growth of the high quality semi-insulating SiC bulk crystals. The transparent inclusions with oval like shape are observed in the SiC bulk crystal grown with the chemical treated source powder. Misoriented phases mainly originate from these transparent inclusions. The inclusions had a small core on the optical microscopic observation. From the result of EPMA, the components of this small core consisted of carbon and silicon, which molar fractions were 0.67 and 0.33, respectively. Although the other part of the transparent inclusion also consisted of carbon and silicon, their molar fractions were 0.50 and 0.50, respectively. The transparent inclusions were considered to be the misoriented SiC phase, which was grown around a carbon-rich core.

This work was financially supported by METI partly through NEDO. The authors thank Mr. M. Okada for his help on EPMA analyses.

Temperature Dependence of Sublimation Growth on 6H-SiC (11 $\bar{2}$ 0) Substrates

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1. Introduction

Crystal growth on (11 $\bar{2}$ 0) substrates is strongly focused due to the high channel mobility of MOSFET [1] and the low leakage current of schottky diode [2]. Since crystals of SiC has been conventionally grown on (0001) substrates, crystal growth on (11 $\bar{2}$ 0) substrates has not been researched sufficiently. To grow high quality crystals on this plane, further investigation of growth mechanism is important. The role of "low-temperature growth process" insertion was investigated.

2. Experiment

Crystals were grown by the sublimation method. (11 $\bar{2}$ 0) substrates were prepared by cutting the boules previously grown on (0001) substrates. The source material was abrasive SiC powder. Temperature at the bottom of the crucible (T_b) was monitored by optical pyrometer. Crystals were grown in argon or nitrogen atmosphere. Growth pressure (p) was approximately 40 Torr. Surface was observed by optical microscope, scanning electron microscope and atomic force microscope.

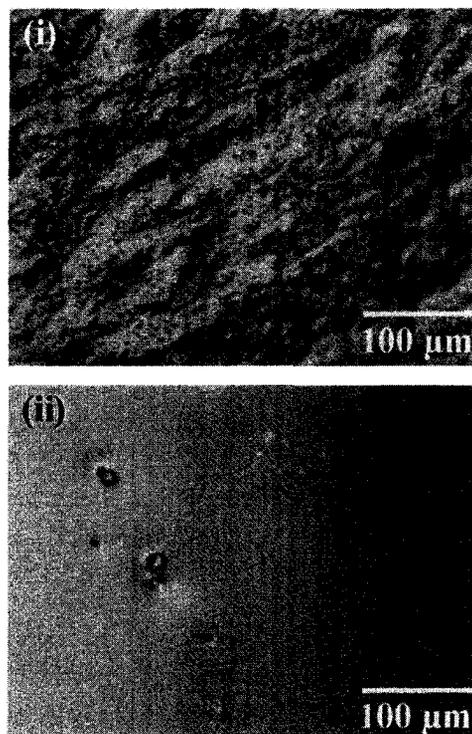
3. Results and Discussion

Figures (i) and (ii) are the surface morphology of the crystals grown on (11 $\bar{2}$ 0) substrates in nitrogen atmosphere. Figure (i) is a crystal which grown at $T_b=2400$ °C and $p=40$ Torr for 1 hour. The surface was undulated. By introducing a "low-temperature growth process", surface flatness was improved as shown in Figure (ii). A crystal shown in Figure (ii) was grown at $T_b=2100$ °C and $p=100$ Torr for 1 hour before growing at $T_b=2400$ °C and $p=40$ Torr for 1 hour. Insertion of this "low-temperature growth process" was effective to improve crystal quality.

Since (11 $\bar{2}$ 0) surface has a higher surface energy, an "adhesive" type growth is dominant than step flow growth. So, it is important to grow crystals in two-dimensional mode on (11 $\bar{2}$ 0) substrates. If crystals grow in three-dimensional mode, hollow core defects would be produced [3]. To grow crystals in two-dimensional mode on (11 $\bar{2}$ 0) substrates, atomically flat and defect free surface is key, since nucleation would preferentially occur at defect sites on the surface. At lower growth temperatures, surface diffusion length of migrating species become shorter and smaller islands nucleate with high density. This high density nucleation of islands enables the homogeneous coalescence at initial stage of the growth with low defect formation. In this way, flat surface with low defect density which is important to realize two-dimensional growth on (11 $\bar{2}$ 0) substrates was achieved. The difference between the growth in nitrogen atmosphere and in argon atmosphere will be also presented at the conference.

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Figures. Optical microscope images of the crystals grown on (11 $\bar{2}$ 0) substrates in nitrogen atmosphere.

(i) 1 hour growth at $T_b=2400$ °C, $p=40$ Torr.
(ii) 1 hour grown at $T_b=2100$ °C, $p=100$ Torr ("low-temperature growth process"), followed by 1 hour growth at $T_b=2400$ °C, $p=40$ Torr.

Vapor Phase Epitaxial Growth of n-type SiC Using Phosphine as the Precursor

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The material properties of SiC make it an interesting semiconductor for devices operating at high temperature, high power, and high frequency. As the development of device proceeds, the demands on the quality of the epitaxial layer and the doping controllability are rapidly increasing. Nitrogen and phosphorous are the most common n-type dopants in SiC. While nitrogen doping and its incorporation mechanisms during epitaxial growth have been studied extensively by several groups [1-3], not much research work has been reported on in-situ doping using phosphorous.

We have carried out phosphorous doped SiC epitaxial growth in a horizontal, water-cooled cold wall reactor. Experiments were performed at temperatures ranging from 1500-1620°C. Silane (2% in H₂) and Propane (2% in H₂) and phosphine (1000ppm in H₂) were used as Si, C and P precursors, respectively. Substrates were (0001) Si-face 4H-SiC and 6H-SiC from Cree. The epitaxial layers were characterized by mercury probe CV measurements and SIMS. The doping dependencies on PH₃ flow, growth temperature and C/Si ratio were studied.

The influence of PH₃ flow on phosphorous doping was investigated at 100 torr and 1560°C. Flow of H₂, SiH₄ and C₃H₈ were fixed at 7slm, 1 sccm and 1.2 sccm respectively. It is shown that the n-type doping concentration in the range of mid 10¹⁵ cm⁻³ to mid 10¹⁶ cm⁻³ can be achieved when PH₃ flow was varied from 0.05 sccm to 1 sccm. Also the increase of doping concentration is approximately proportional to the square root of PH₃ flow. Study on the effect of growth temperature showed that phosphorous doping decreased when temperature is increased from 1500 to 1620°C. This was explained by the enhanced desorption of Phosphorous-containing species on the growth surface at higher temperature. The site-competition growth was carried out with C/Si ratio varied from 0.3 to 14. It was shown that phosphorous incorporation was insensitive when C/Si was higher than 3 or lower than 0.9. However, the phosphorous incorporation increases with decreased C/Si ratio when C/Si is between 3 and 0.9. This is opposite to what has been reported in reference [4]. The difference might originate from different growth conditions (pressure, H₂ flow, etc.). Our result seems to suggest that phosphorous might occupy C site rather than Si site at certain growth conditions.

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A Simple Mapping Method of Elementary Screw Dislocations in Low-doped Hexagonal SiC Epitaxial Layers

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The morphologies of etch pits of three different kinds of dislocations in low-doped hexagonal polytype epitaxial layers have been investigated by KOH etching, synchrotron white beam x-ray topography (SWBXT), optical microscopy, and atomic force microscopy (AFM). A simple method by KOH etching and polishing for monitoring elementary screw dislocations in SiC epilayers is proposed.

Elementary screw dislocations are known to reduce the breakdown voltage of SiC p-n junctions and Schottky barriers. There are major efforts underway in reducing their density in both substrates and subsequent device layers. To do so, it is important to have or to develop a method for characterization of screw dislocation density and distribution.

The samples examined in this study were 4H-SiC wafers oriented 8° from the [0001] toward the $\langle 11\bar{2}0 \rangle$ directions with 10 μm thick epitaxial layers, and an on-axis n⁺ 4H-SiC substrate. The low-doped ($\sim 10^{15} \text{ cm}^{-3}$) epitaxial layers were grown on (0001) Si surface of substrate by vapor phase epitaxy (VPE) at a low pressure (~ 100 mbar). Epilayers were etched in molten KOH to reveal the locations where dislocations intersect the (0001) Si surface. The shapes of etch pits were analyzed by optical microscopy and AFM. The etch pits of threading dislocations were hexagonal in shape and had two distinctly different sizes. The larger ones were more symmetric than the small ones, implying the dislocations of small etch pits were inclined. The etch pits of basal plane dislocations were oval-shaped, suggesting small angle formed by the dislocation line with the surface. Three different etch pits could be distinguished under optical microscope at $\times 200$ magnification, owing to the difference in etch pit depth clearly visible using Nomarski differential interference optics. AFM study of lightly etched layers showed the large pits of threading dislocations are approximately twice as deep as the others. The large pits in etched morphology correspond one to one to the white dot contrasts of elementary screw dislocations in the SWBXT image. Etched epilayers were carefully polished with 6 μm diamond paste. It was possible to remove a top layer of the structure leaving only the etch pits due to elementary screw dislocations. The same method was tested on the on-axis n⁺ substrate. The etch pits were all circular and in several different sizes, making it very difficult to distinguish edge and screw dislocations.

Power Schottky and p-n diodes on SiC epi wafers with reduced micropipe density

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Micropipe density reduction and its impact on device performance is a critical topic in SiC power device development. In this paper we report on 2 mm diameter devices fabricated with high device yield on 2 inch 4H-SiC wafers with reduced micropipe density (RMD). Both Schottky and p-n diodes were fabricated on epitaxial layers grown on SiC RMD wafers.

Micropipe filling process was done on (0001)Si face of off-axis commercial 2 inch 4H-SiC substrates with standard micropipe density. Micropipe density after the filling did not exceed 10 cm^{-2} . 4H-SiC device epitaxial layers about 10 microns thick with concentration $N_d - N_a \sim 10^{15} \div 10^{16} \text{ cm}^{-3}$ were consequently grown by CVD method. Schottky diodes without edge termination were formed on the CVD layers by Ni (~15 nm) evaporation and consequent gold deposition (~0.5 μm) in the same evaporation run, to ensure good spreading of electric current.

P⁺-layers for p-n diodes were grown on the CVD n-type layers by sublimation method. Uniform p-type sublimation epitaxy for 2" SiC wafers was demonstrated for the first time. Mesa structures for pn diodes were formed by reactive ion etching.

Diodes of 2000, 1000, 500 and 200 μm diameter were fabricated. For more than 58% of 2 mm diodes, the leakage current was less than 1 μA at 300 V reverse voltage. For more than 50% of 2 mm diodes reverse voltage exceeded 600 V. Forward IV characteristics had a turn-on voltage of about 1.25 V and state-on resistivity of about 4 Ω . On-state resistance was determined by doping level of the substrate and can be reduced by diode parallel connection.

Reverse blocking voltage for 2 mm pn diodes of over 700 V was obtained. For both Schottky and pn diodes electric breakdown at device periphery was frequently observed. These results show high potential of micropipe filling technology for power device development, especially for large area (>3 inch) SiC wafers. Device and material characteristics will be presented and discussed.

OXIDATION-INDUCED CRYSTALLOGRAPHIC TRANSFORMATION IN HEAVILY N-DOPED 4H-SiC WAFERS

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Crystallographic stability of SiC during processing and device operation is of concern, particularly because of the recent discovery that 4H to 3C polytype conversion can occur under carrier injection in a *pn* junction. We have discovered a pronounced crystalline instability in 4H-SiC wafers doped with unusually high levels of N (nominally 0.008 Ω -cm resistivity, $\sim 3 \times 10^{19}$ cm⁻³ donors) when the wafers are subjected to a standard oxidation cycle. A total of seven such commercially obtained wafers (from five different boules), having ~ 2 μ m thick epitaxial layers doped at the $1-1.5 \times 10^{17}$ cm⁻³ level with N, were thermally oxidized at 1150 °C for 90 min. in dry O₂ to a thickness of ~ 325 Å. Their surfaces appeared normal and smooth prior to oxidation, but immediately after oxidation exhibited dimpled regions, usually in the centers of the wafers and surrounded by a pronounced ridge roughly 2 μ m high. The sharp ridges separating dimpled from undimpled regions generally coincide with the edges of the more heavily-doped central (dark) regions in the substrates. Those regions presumably correspond to the (0001) growth facets in the substrate boule. Some transformed wafers were characterized by confocal micro-Raman scattering, synchrotron-based white beam X-ray topography (SWBXT), and photoluminescence (PL). In addition, we fabricated Schottky diodes on three wafers using Ti, Ni, and Pt and characterized their barrier heights by current-voltage (*I-V*) and capacitance-voltage (*C-V*) methods. The barrier heights are uniformly lower in the dimpled regions by about 0.47 V compared to the peripheral, undimpled regions of each wafer, *independent* of the Schottky metal (even though the barrier heights differ by up to 0.6 V among the metals). Idealities of the diodes are actually better in the dimpled regions than in the undimpled regions, and the epilayer doping does not vary between dimpled and undimpled regions after transformation. The SWBXT images show a dense cellular structure of dislocations only in the central, dimpled regions, but were not able to detect any 3C material. The Raman measurements, which sample about the top 2 μ m of each sample, show phonons characteristic of 4H-SiC in both dimpled and undimpled regions, but a marked enhancement in the relative strength of several modes including A₁(LO) in the dimpled regions. The PL measurements, however, show a dramatic shift in the highest energy peak at 300 K from the usual 4H position of 3.16 eV in the undimpled peripheral regions to 2.42 eV in the dimpled areas, suggestive of 3C regions or lamellae (which may be too small to detect by Raman or topography). The 3C regions could also explain the reduced Schottky barrier heights. Transmission electron microscopy and low temperature PL are in progress to clarify the nature of the transformation. Possible causes will be considered. This effect may limit the maximum doping that can be employed in *n*-type substrates.

This work was supported by the National Science Foundation under Grant No. ECS 0080719, and by a Motorola Semiconductor Products Sector Sponsored Project.

Observation of planer defects in 2 inch SiC wafer

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SiC bulk crystal has been grown by the sublimation method. The defects such as micropipe (MP) and planer defect (PD) can cause serious problems for device performances. Therefore, it is important to reduce these defects for the realization of high device performance.

Diameter of the substrate was 40mm. As the crystal grew 15 mm, diameter was expanded to 50mm by the sublimation method. Top of the grown bulk was convex and facet appeared in the center. Three SiC wafers were cut out from the bulk. These wafers were almost transparent and observed by optical microscope (transmission mode) to investigate the PD distribution in the wafers. In each wafer, nine points were measured from the edge to the center.

Though the shape of PD was all hexagon, not all PD were regular hexagon, e.g. distorted hexagon, triangle, parallelogram and so on. The larger crystal grew, the less PD density (PDD) became. The PDD at the edge region was almost same as that at the center region. The MP density of the edge region was less than that of the center region.

Figure1 shows the distribution of PD size (PDS) in each wafer. The PDS close to the substrate was smaller than that near the surface. The PDS was smaller at the edge region than that of the center region. Before the growth, the growth surface was flat. On the flat surface, crystal grew mainly toward c-axis direction, and PD expansion was restricted. However, as crystal grew larger, growth surface became convex. In this case, growth toward a-axis direction became rapidly. So, in this region, PD was easily expanded laterally.

At several points, MP annihilation by PD was observed. There were three ways of MP annihilation, i.e. the annihilation of MP under PD at the center region of PD, at the edge region of PD and adsorption of MP out of PD at the edge region of PD.

Characterization of wafers by X-ray diffraction, Raman spectroscopy and KOH etching will be presented.

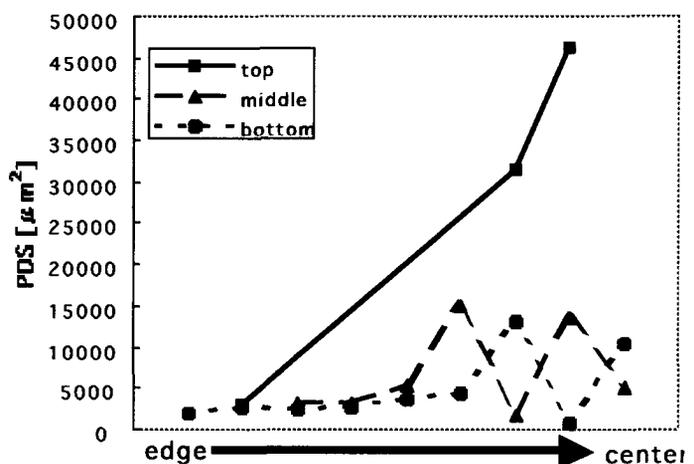


Figure1. The distribution of PDS in SiC wafers

The investigations of 4H-SiC/SiO₂ interfaces by optical and electrical measurements

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The channel mobilities of silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs) reported so far are much lower than the value expected from the bulk mobility. Many studies have been carried out to resolve these problems, nevertheless, the origin which lower device characteristics has not been clarified yet. In this report, we have examined SiC/SiO₂ interfaces by optical and electrical measurements to make clear the structures of the interfaces.

Epitaxial wafers of 4H-SiC with 8° off-oriented (0001) Si face and n type were used for the measurements. Thermal oxides were grown in pure O₂ ambient at 1200 °C. Simultaneous capacitance-voltage (C-V) measurement, Fourier-transformed infrared reflection absorption spectroscopy (FTIR-RAS) and spectroscopic ellipsometry were carried out as electrical and optical measurements, respectively. For the optical measurements, the samples were etched at an angle by dipping gradually into diluted hydrofluoric acid at a constant speed. FTIR-RAS and ellipsometric measurements were performed along the slope of the oxides films to obtain the data as a function of oxide thickness.

From C-V measurements, number of interface traps per unit area (N_{it}) were obtained to be over 7×10¹² cm⁻² and the shift of flat band voltage (V_{fb}) was +18 V. The apparent refractive indices derived from the spectroscopic ellipsometric measurements under the assumption that the oxide films have uniform refractive indices, do not constant but decrease with oxide film thickness, especially in the region below 10 nm in thickness. This change can be explained by the model that there exist interface layers with higher refractive indices than those of SiO₂ and SiC. Figure 1 shows the results obtained from FTIR-RAS measurement. The peak position of Si-O-Si stretch TO modes shifts to lower frequency in the region below 5 nm in thickness of oxide layers and the values become away from that of fused quartz. These results indicate that transition layers exist at the interface between SiC and SiO₂.

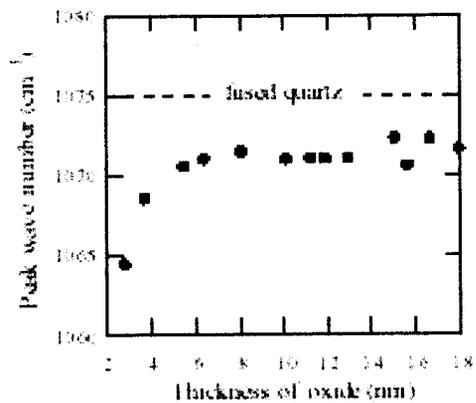


Fig. 1 Peak wave number of TO mode as a function of oxide thickness.

Growth and characterization of three-dimensional SiC nanostructures on Si

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SiC is known to be a promising candidate for high power, high temperature and high frequency devices. SiC based nanostructures could result in new and improved properties, phenomena, and processes and thus expand the potential to new optical, high-frequency and photonic applications.

In this work we present a study of morphological properties of SiC islands on Si and of three-dimensional SiC-Si nanostructures. SiC was grown on (001)Si by a pure carbonization process in a molecular beam epitaxial system using an electron gun evaporator as carbon source. At constant temperature, the SiC islands were generally growing in a three dimensional mode. At high temperatures above 800°C the nucleation density was increasing up to an effective coverage of around one tenth of a monolayer and remains constant after. The need of Si for the SiC formation as well as the Si evaporation results in a depletion of the area surrounding the SiC islands. As a result well resolved pyramids with a four fold symmetry are forming on on-axis substrates with SiC nuclei on the top. These pyramids are tilted on off-axis substrates and therefor non-symmetric. The SiC islands are growing downwards along the four edges, forming facets and maintaining the symmetry of the pyramids. In contrary, at low temperatures islands are growing faster laterally in a quasi two dimensional mode resulting in an early coverage of the surface and preventing the formation of pyramids. The size of Si pyramids can be enhanced by pre-deposition of 1 ML Ge prior to the carbonization. The saturation nucleation density in dependence on temperature, carbon flux and Ge pre-deposition was estimated and the activation energies extracted. Possible applications for the high-temperature-grown three dimensional SiC-Si structures will be discussed.

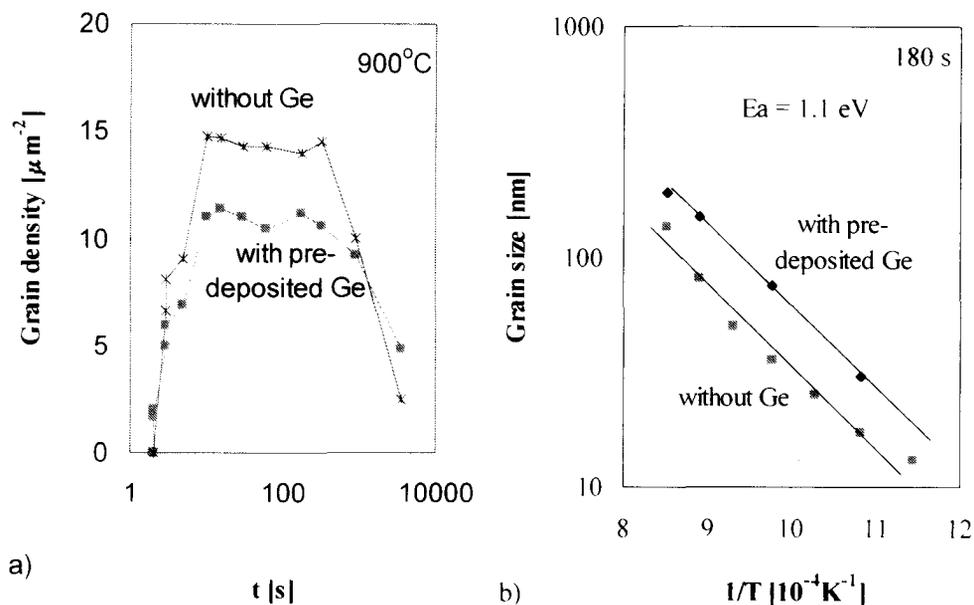


Fig. 1 Evolution of SiC islands on Si at a carbon flux of $10^{-13} \text{ cm}^{-2}\text{s}^{-1}$: a) Grain density versus time at 900°C and b) Grain size versus growth temperature after 180 s growth.

Characterization of 2 inch as Grown SiC Bulk by SWBXT at SPring-8

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There are few reports of research of SiC as grown bulk crystal without the surface morphology. So, we could research SiC bulk crystal using facilities at SPring-8 (BL28B2). Since the SR beam at SPring-8 has 8GeV electron beam energy, SR beam transmits even 2-inch SiC bulk crystal and we can observe SWBXT (Synchrotron White Beam X-ray Topography). We prepared 2-inch 6H-SiC bulk, which was made by sublimation method on (0001) 6H-SiC substrate. The height of sample is about 22mm and the shape is shown in Fig. 1. The distance from sample to the film is about 300mm, the exposure time is a few seconds. The directions of incident beam were $\langle 1-100 \rangle$ and $\langle 11-20 \rangle$ and the size of incident beam was 2mm x 2mm. The Laue pattern was 2 fold symmetry and the Laue spots became rectangle. We can investigate defects easily by the Laue pattern and spots. If the sample is perfect 6H-SiC crystal, these Laue spots have no contrast. But if the defects exist in the crystal, Laue spots are inhomogeneous.

Fig.2 and 3 show the Laue pattern and topography. The contrast of Laue spot of the sample was enlarged as shown Fig.3. The incident direction and diffracted planes were $\langle 1-100 \rangle$ and (11-20).

Since the shape of bulk crystal is like Fig.3, the transmission length and the length of topography image are different by the measurement points.

From this figure, the contrast decreases as growing and the image of Fig.3 (c) undulates $\langle 0001 \rangle$ direction. We can confirm the defects in the crystal decrease as growing.

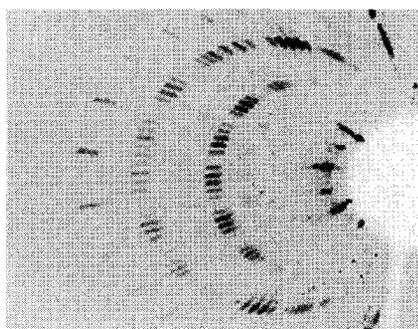
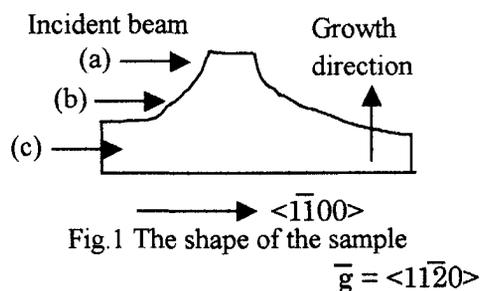


Fig.2 Laue pattern of 6H-SiC bulk crystal

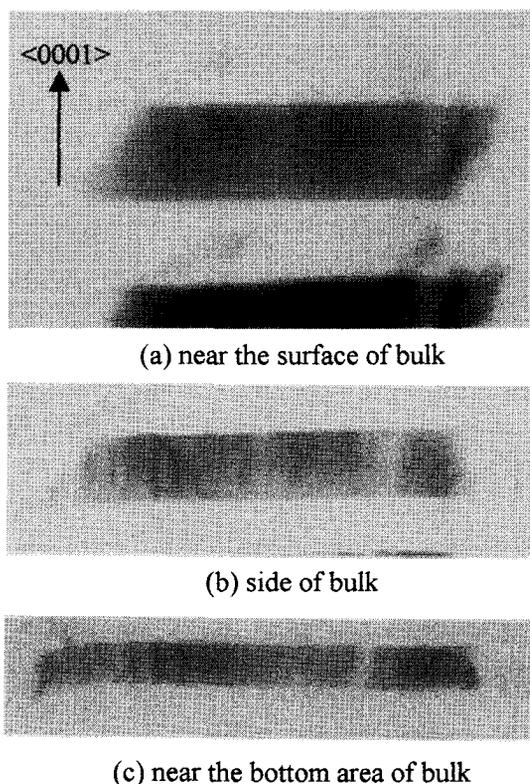


Fig.3 Topography of 6H-SiC bulk crystal

The neutral silicon vacancy in SiC: Ligand hyperfine interaction

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The silicon vacancy V_{Si} in SiC is of great interest both theoretically as one of the fundamental intrinsic defects and practically, because it is created in device processing steps like ion implantation. V_{Si} can exist in various charge states within the band gap, but a definite chemical identification has so far only been possible for the negatively charged silicon vacancy. This was possible by the observation of ligand hyperfine interaction with ^{13}C atoms in the nearest-neighbour (NN) shell and with ^{29}Si atoms in the next-nearest-neighbour (NNN) shell in electron paramagnetic resonance (EPR) experiments.

The neutral silicon vacancy has been observed in optically detected magnetic resonance (ODMR) experiments in electron irradiated samples when either one of the photoluminescence (PL) bands in the near infrared called V1, V2 and V3 in 6H SiC and V1, V2 in 4H SiC was resonantly excited with a Ti:Sapphire laser [1]. This number of lines arises from the corresponding number of inequivalent lattice sites on which the defect can reside in the two polytypes. A spin triplet state with the characteristic hyperfine signature of the NNN ^{29}Si atoms was observed by monitoring each PL band. However, due to low signal intensity the hyperfine interaction with the ^{13}C atoms (only 1.11% natural abundance) in the NN shell could not be resolved. Already in the 1980's triplet EPR signals with a similar crystal field splitting had been observed after the samples had been illuminated [2]. At that time the signals were attributed to distant vacancy pairs. More recently such lines were reported even in EPR experiments in dark, even though there the spectra were dominated by the signal from the negative charge state of the silicon vacancy [3]. No ligand hyperfine interaction could be resolved.

New ODMR experiments on a ^{13}C isotope enriched sample and on high quality epitaxial films now revealed these ^{13}C hyperfine lines. The hyperfine parameters of $A_{\parallel}^C \approx 28$ G and $A_{\perp}^C \approx 11$ G (with slight variations depending on polytype and lattice site) for interaction with the NN ^{13}C -atoms and $A^{Si} = 3.0$ G (isotropic) for the NNN ^{29}Si -atoms are very similar to the ones found for the silicon vacancy in its negative charge state. This confirms that the spin triplet observed in ODMR originates from the 'isolated' silicon vacancy.

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The deep boron level in high voltage pin diodes.

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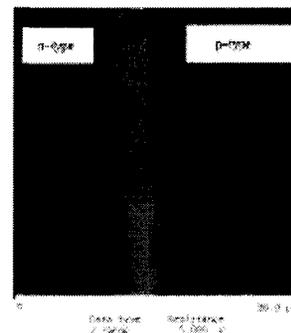
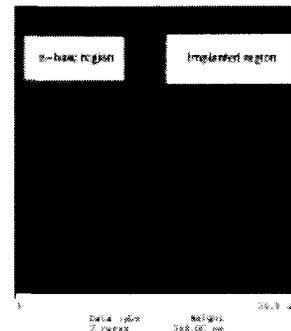
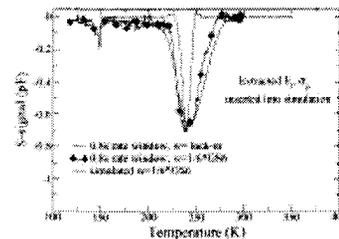
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Well behaved high-voltage (3.5 kV blocking voltage) 4H-SiC pin diodes were examined with respect to implantation induced electrically active defects using deep level transient spectroscopy (DLTS), admittance spectroscopy, capacitance-voltage measurements, atomic force microscopy and the new scanning spreading resistance technique (SSRM). The material used was 35 μm thick epitaxial n-type 4H-SiC layers grown on commercial Cree wafers by chemical vapor deposition. The nitrogen doping in the epitaxial layers were in the low 10¹⁵ cm⁻³ region. The diodes were manufactured with a shallow high concentration (10²⁰ cm⁻³) aluminum implantation and a deeper box profile of implanted boron of intermediate concentration. After the annealing process the metallurgical junction seen by secondary ion mass spectrometry SIMS displayed a "soft" junction character with an in-diffused boron tail of several micrometers. In the junction region a deep hole trap was found to dominate the metallurgical pn junction at room temperature (RT). High resolution DLTS weighting functions were used and the trap identified as the boron related D-level. This trap level effectively removed free carriers (holes) causing the in-diffused boron tail of the profile to become intrinsic. SSRM confirmed the existence of an intrinsic region where the boron had diffused into the material. By activating the trap level at temperatures *geq* 600 K the junction behaved as a low doped soft junction without an intrinsic region. The electrical measurements together with the chemical boron profile gave at hand that less than 10% of the in-diffused boron resides on substitutional sites forming shallow boron acceptors. The D-level operates as a hole trap.

The figures show: top) DLTS spectra of a reverse biased diode showing the D-center, center) Topography of the area between implanted and unimplanted diode using atomic force microscopy, bottom) SSRM of same region. The bright contrast shows the intrinsic region where a large fraction of the boron has diffused and formed D-centers that effectively traps the holes in this region.



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Growth of AlN films by Hot-Wall CVD and Sublimation Techniques: effect of growth cell pressure

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The demand of using AlN in many applications such as short wavelength optical devices and SiC based FETs is increasing but the perfection of the films is still limited mainly due to the difficulty of N incorporating, the strong reactivity of Al, gettering impurities from the ambient, and the lack of lattice matched substrate material. A lot of efforts have been directed towards developing better AlN synthesis methods but still the route to device quality material is not clear.

In this study hot-wall CVD and sublimation epitaxy were used that can provide high growth temperatures advantageous for the AlN deposition. The pressure inside the growth cell can influence the growth of AlN films and their properties such as thickness, morphology, and luminescence. In the CVD experiments the growth cell pressure was set to 1000, 100 and 50 mbar while the temperature was kept at 1200°C. Sublimation growth process experiments occurred at temperature of 2100°C at the source under nitrogen pressure of 200, 500 and 900 mbar. Characterization techniques used were SEM, cathodoluminescence (CL) and infrared reflectance.

At low growth cell pressure in the CVD experiments thick AlN layers with smooth surfaces, which produce interference fringes in the reflectance spectrum (Fig. 1, 50 mbar) were obtained. AlN films grown by sublimation consist of grains with height of up to 90 µm (Fig. 2). The change of the pressure at this temperature does not influence substantially the microstructure of the sublimation grown films except for the enlargement of the grains.

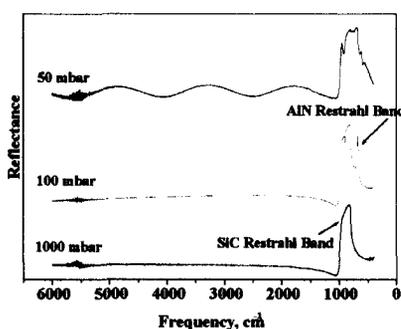
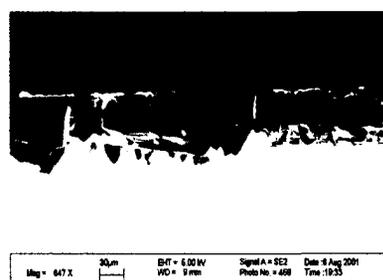


Fig. 1 Infrared Reflectance of AlN CVD layers grown at different cell pressure

Fig. 2 SEM image in cross-section taken from the sublimation grown layer at 200 mbar



CL panchromatic images with boundaries of dark contrast were taken from the films produced in either of the two deposition methods. Our results show that under conditions of moderate growth cell pressure (100 mbar in the CVD and 200 mbar in the sublimation experiments) both processes give good quality material AlN films in which the near band edge emission in the CL spectra appears.

A method of reducing micropipe using metal mask by the sublimation growth

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The silicon carbide substrate produced by the modified Lely method generates a lot of micropipe in the growth process even if lely crystal was used for a seed crystal. And the Lely method cannot obtain large diameter substrate.

For this reason when we produce the large diameter substrate, the crystal with many defects enlarged from the Lely crystal needs to be used as a seed.

Since the micropipe propagates to the grown crystal, it is difficult to reduce the micropipe.

In this study, we tried to use metal mask to cover the micropipe. This way seems to be similar to the epitaxial lateral over growth method that can reduce the spiral dislocation, by forming and carrying out lateral over growth on the mask.

The modified Lely crystal was used for seed crystal with a thickness of 0.8mm.

After the seed crystal was performed organic washing and acid washing, the metal mask was formed by the electron beam deposition method.

The metal used for deposition is W and Pt and the thickness of mask is 0-100 Å.

Then, the modified seed crystal was fixed to the graphite lid.

The graphite crucible was filled up with SiC powder, and was overheated to 2200 degrees C with the graphite lid.

The growth pressure was 100Torr.

The grown crystal was evaluated by the polarizing optical microscope.

Figure 1 shows the cross-sectional transmission microscope photograph near the interface of a seed crystal and a growth crystal with the thickness of the metal mask about 100 Å.

It was clearly shown that micropipe stops at the interface between seed crystal and grown crystal, on both W and Pt cases.

The micropipe density was measured with a polarizing optical microscope.

We confirm that the micropipe density in grown crystal decreases 50% than the micropipe density in seed crystal..

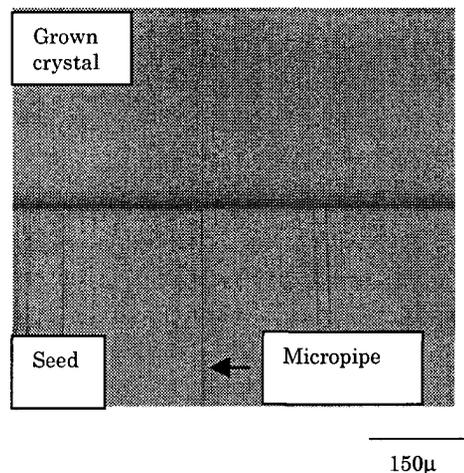


Fig.1 Cross-sectional photograph of the crystal using platinum

Atomic steps observation on 6H and 15R-SiC polished surface.

P. Vicente^{1,2}, E. Pernot³, D. Chaussende^{1,3}, J. Camassel².

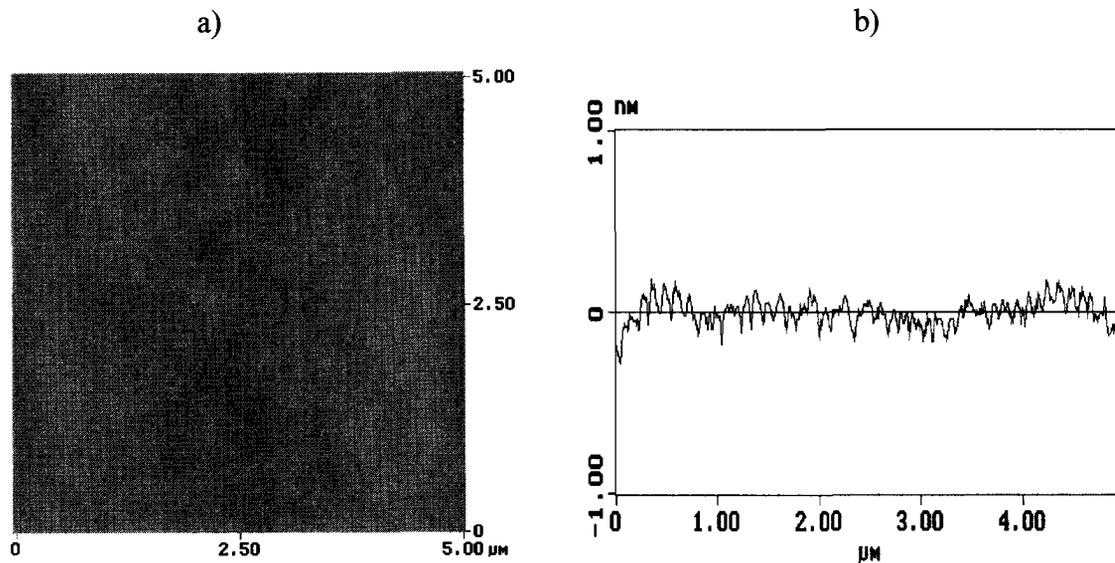
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6H-SiC bulk is widely used as a substrate for growth of III-Nitride epitaxial layers. The smaller lattice mismatch between GaN and SiC compared to GaN and sapphire, and the high thermal conductivity makes 6H-SiC a promising substrate for nitride growth. Surface preparation before the epitaxial growth is a critical step, because every defect on the surface of the substrate is a potential source for a defect in the epitaxial layer. In a similar way, the surface roughness can be a limiting factor for the roughness of the epitaxial layer surface. The most recent SiC polishing process, produces atomically flat surface, free of scratch and damaged layer [1].

Figure a) shows with Atomic Force Microscopy the presence of atomic steps on a 0° 8' off axis 6H-SiC surface (with 1.5 Å RMS roughness). Figure b) shows the corresponding profile through the steps (with step of about 2.5 Å in height and 110nm in length).



Due to an advanced polishing surface preparation, bi-layer atomic steps has been revealed both on 6H and 15R-SiC. By synchrotron X-ray topography, Raman spectroscopy and atomic force microscopy we have established the strong correlation between the polished surface and the bulk crystalline quality. For instance, grain tilt and twist can be evidenced by step length and direction.

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CVD SiC powder for high purity SiC Source material

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Recently, the need to the high purity SiC source material has been increasing in order to grow high quality SiC single crystal.

SiC powder which made by Acheson method has been used basically as this kind of raw materials and has been applied for abrasives and refractory. However the current powder has no cleaning way other than acid dipping or some similar treatment. Lots of reseachers studying single crystal SiC have been noticing the limitation of purity in the current raw material. Thereupon we developed high purity CVD-SiC powder for single crystal SiC. This powder is made from CVD-SiC polycrystal plate by crushing it directly. The result of the purity of the powder (A) is quite good rather than current powder(B) especially in Fe, Ni, Al, Ti as shown in Table 1.

As shown in Fig.1, the powder diameter distribution ranges from 1000 micron to 200 micron in powder(A) and 200 micron to 50 micron in powder(B). This powder source(A) will be a good precursor for getting sinlge crystal SiC by sublimation method.

Table 1: Impurity of SiC powder (by ICP-AES)

Powder type	Elements(ppm)										
	Fe	Ni	Ca	Al	P	B	Na	K	Ti	V	Zr
(A) CVD-SiC powder after crushing ^{*1}	0.1	0.1	0.1	0.1	<0.1	<0.1	<0.1	<0.1	<0.1	0.1	<0.1
(B) High Purity SiC powder by Current Acheson method ^{*2}	5	0.8	0.5	14	<0.1	<0.3	0.4	<0.1	3.5	0.7	0.4

^{*1}¹³C-SiC beta type ^{*2}⁶H-SiC alpha type

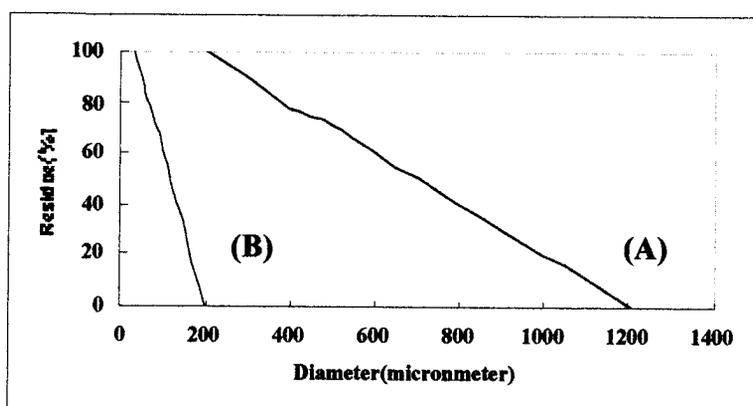


Fig.1 : Powder diameter distribution

PLD BN as an Annealing Cap for Ion Implanted SiC

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Planar SiC devices are fabricated using ion implantation because the rates of diffusion of dopants into SiC are too low even at temperatures as high as 1800°C to be technologically useful. The implanted dopants have to be activated by a high temperature anneal, and at the temperatures at which the dopants are activated, silicon evaporates preferentially from the SiC lattice. We have shown that the activation of the n-type dopant, nitrogen, is essentially complete at 1600°C with no surface degradation due to silicon evaporation when we used an AlN cap¹. However, at temperatures > 1600°C the AlN evaporates creating hexagonal holes through which the silicon can now preferentially evaporate². Unfortunately, the p-type dopants, Al and B, require temperatures at least as high as 1700°C for their complete activation³. Thus, a cap must be found to withstand temperatures this high and still retain the necessary qualities of the AlN cap, which are: 1) retains coverage of the SiC surface during the anneal, 2) does not react with the SiC surface during the anneal, and 3) can be removed selectively without harming the SiC surface after annealing.

We show that such a BN/AlN cap can withstand these temperatures and retain the properties of the AlN cap. This cap is created by depositing a ~200 nm AlN film by pulsed laser deposition (PLD) followed by the PLD deposition of ~300 nm BN film. The cap is removed after the anneal by ion milling the BN off, and then selectively etching away the AlN film in warm KOH. The structure of the SiC surface is then examined with a SEM and AFM, and the surface chemistry is studied by AES.

To better understand the cap properties, we recorded the surface structure of the BN with a SEM and AFM; checked for chemical intermixing at the interfaces and surface contamination of the SiC surface using AES, and examined the cap structure using FTIR spectroscopy and XRD. We are currently looking at the structure with TEM and will report the results at the meeting. Briefly, the results show that the BN film remains intact during the anneal and no intermixing of the BN and AlN films or AlN film and SiC substrate occur. We do not yet know to what extent the BN film has crystallized, but we expect the TEM results will tell us that.

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Growth characteristics of SiC in a hot-wall CVD reactor with rotation

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Rotation has been implemented in a horizontal hot-wall reactor for SiC CVD by means of gas foil levitation [1]. The bottom part of susceptor has been redesigned to carry a rotating disk with a capacity of three 2" wafers. The capacity of the reactor is three 2" wafers. Argon or hydrogen is used as the rotating medium and the rotation rate is maintained fast enough for growing thin MESFET structures. The CVD process is similar with the one previously described in [2].

Smooth surface without any decoration of dislocation defects has been achieved, after the substrate is raised slightly above the susceptor floor: the lifted-disk rotation. Under non-optimized conditions, particles are observed on the epilayer surface, presumably caused by gas phase nucleation. The best thickness uniformity has been obtained without lifting up the substrate, with 0.36% and 0.92% for 35 mm and 2" wafers, respectively. N-type doping uniformity as good as 1.35% on a 35 mm wafer has been achieved with un-lifted disk rotation as well. The good morphology in the lifted-disk rotation has been compromised by the slightly worse uniformity. However, thickness and doping uniformity values can still be as good as 6% and 7.7%, respectively for a 2" wafer. Both the intra-wafer and the run to run doping uniformities are less than $\square 10\%$. Both n- and p-type doping is readily achieved. The n-type doping ranges from $5 \cdot 10^{15} \text{ cm}^{-3}$ to $2 \cdot 10^{19} \cdot \text{cm}^{-3}$, and p-type doping between $5 \cdot 10^{15} \text{ cm}^{-3}$ and $5 \cdot 10^{18} \cdot \text{cm}^{-3}$ has been obtained. MESFET structures have been grown on semi-insulating substrates with excellent doping control.

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On shallow interface states in *n* type 4H-SiC metal-oxide-semiconductor structures

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The unacceptably low electron channel mobility currently observed in 4H-SiC metal-oxide-semiconductor field-effect transistors is of major concern. A possible reason for this mobility reduction is considered to be the high density of interface states near the conduction band edge of 4H-SiC. Using capacitance-voltage (CV) analysis the interface state density as a function of energy has been estimated and is found to increase rapidly towards the conduction band edge [1].

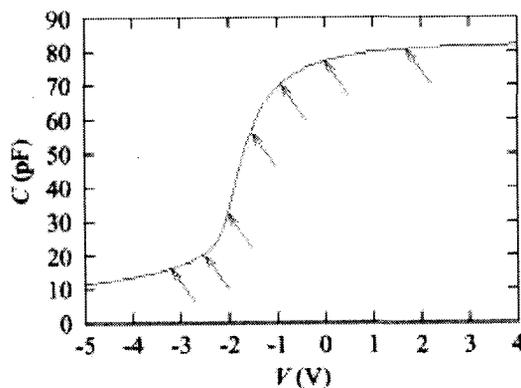


Fig. 1: A quasi-static CV measurement at 300 K for an *n* type 4H-SiC MOS. Arrows show the charging levels used in Fig. 2.

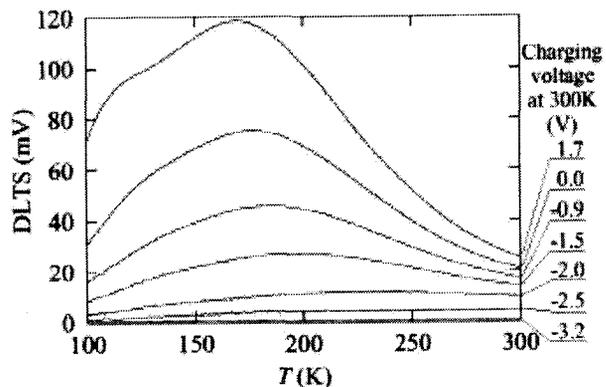


Fig. 2: DLTS spectra for an *n* type 4H-SiC MOS, measured for several charging levels. The discharging voltage is -5 V at 300 K.

In this work we examine shallow interface states by using constant capacitance deep level transient spectroscopy (DLTS) on *n* type 4H-SiC metal-oxide-semiconductor (MOS) capacitors. Fig. 1 shows a quasi-static CV measurement at 300 K. Fig. 2 shows that the DLTS spectrum measured at 1 Hz reveals an interface state peak at 170 K which grows as the charging level increases. This peak has an activation energy of approximately 0.12 eV and a number density that exceeds 10^{12} cm^{-2} . Capture rate data reveals that these interface states are slow, exhibiting a very small electron capture cross section in the range of $10^{-22} - 10^{-24} \text{ cm}^2$ at 170 K. Furthermore, we find similar traps in differently prepared oxides. In summary, slow interface oxide traps are observed whose distribution as a function of energy is a peak near the conduction band edge of 4H-SiC. These traps are possibly a signature of the native oxide defect described by Afanas'ev *et al.* [2]

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The Effect of epitaxial growth on warp of SiC wafers

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1. Introduction

Before the routine development of SiC devices can be claimed, many technological problems remain to solve. One of them is the warp of wafers. Especially, when the diameter of wafers is enlarged, it is necessary to pay attention. Tsuchida et al.^[1] reported that the epitaxial growth process improved the crystal bending. We investigate the effect of epitaxial growth process on the warp of SiC wafers. In this report, we performed the hydrogen etching and the epitaxial growth process on the wafers with the large warp and proposed the origin of the warp.

2. Experimental

We carried out hydrogen etchings and 4H-SiC epitaxial growth under 700Torr at 1500°C in our Hot-Wall CVD reactor. In the hydrogen etching, the wafers were exposed to 5SLM hydrogen gas for 5min. The epitaxial growth occurred using 2.5sccm silane and 1.2sccm propane in 5SLM hydrogen carrier gas for 1h. We measured the warp of the wafer after the processes. In each process, we used one-side (Si face or C face) polished wafers. We also measured the warp of the wafers before and after polishing.

3. Result and Discussion

Table 1 shows the curvature radius of wafers after each step. Both Si-face and C-face became concave after polishing. This indicated that the polishing process induced the internal stress. After the hydrogen etching, an improvement in the warp of wafers was confirmed, because the hydrogen etching reduced the stressed layer caused by mechanical polishing. The slightly convex surface was observed due to the overpolishing of a few microns at the periphery of the wafers. Further improvement of the warp was confirmed on the Si-face after epitaxial growth (the typical carrier concentration is $7 \times 10^{15} \text{cm}^{-3}$ and the typical thickness is $4.5 \mu\text{m}$). On the other hand, C-face became convex after epitaxial growth. Because the growth condition was optimized only for Si-face, not for C-face, the internal stress was supposed to be introduced in the C-face epitaxial layer

Table 1 The curvature radius after each step

		before	after	after
		polishing	polishing	process
Epitaxial	Si face	—	6.9m	80m
	C face	63m	11m	-6.5m
Hydrogen	Si face	87m	8.1m	-31m
	C face	57m	6.6m	-21m

4. Summary

We performed the hydrogen etching and epitaxial growth on Si face and C face of the 2inch SiC wafer and measured the warp of them. We confirmed the improvement of the warp after hydrogen etching and the further improvement on Si-face after epitaxial growth.

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Infrared investigation of implantation damage in 6H-SiC

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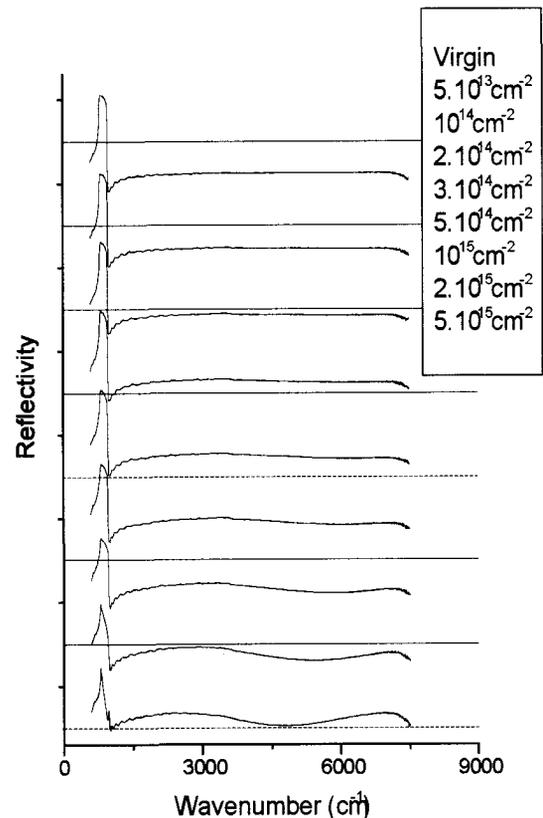
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We present the results of an infrared (IR) investigations of the effect of implantation damage on the reststrahlen band of 6H-SiC implanted with N⁺-ions. The implantation energy was 160 keV and the implantation temperature 300K. The dose ranged from 5 10¹³ to 5 10¹⁵ cm⁻². After implantation IR reflectivity spectra were collected at room temperature in the middle infrared range, from 500 to 7500 cm⁻¹. We used a Bruker IRTF spectrophotometer fitted with a microscope and a MCT detector. Results are shown in Fig. 1.

They demonstrate the following :

- i°) a decrease and broadening of the topmost reflectivity structure versus implantation dose. This comes from implantation damage and shows that, even if one focus only on the reststrahlen band, IR reflectivity constitutes a most sensitive tool to probe, on-line, the implantation damage ;
- ii°) a change in refractive index of the topmost (implanted) layer with respect to the host material. This change is dose-dependent and, at high dose, results in the appearance of a new (large) set of interference. This is again an useful tool to probe the in-depth extension of damage ;
- iii°) finally at very high dose (~ 5 10¹⁵ cm⁻²) a new (sharp) extra feature reveals, close to the LO frequency of bulk SiC [1]. It comes because of a strong change in the optical properties of the implanted material with appearance of a new (no longer pure SiC-like) effective medium.



We have modelled our IR spectra with the use a transfer matrix method [2] and product oscillators [3]. Results will be discussed in great details.

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TCAD optimisation of 4H-SiC channel doped MOSFET with p-polysilicon gate

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Abstract

In this paper the optimisation of structure of the channel doped MOSFET, with p-polysilicon gate based on 4H-SiC is studied using TCAD simulation. It is known that the channel mobility of the depletion mode of Al-gated C-MOSFET is improved by increasing the channel doping level but that this leads to a decrease in threshold voltage, V_{th} [1,2]. Since p-polysilicon has higher workfunction than Al or n-polysilicon gate, which results in higher V_{th} , p-polysilicon gate is expected to allow further improvement of the channel mobility by increased channel doping.

The device structure used is based on a $5 \times 10^{15} \text{ cm}^{-3}$ Al doped p-type substrate, gate width of 5um, tox of 50nm, source and drain doped with Phosphorus with depth of 0.5um, channel doping with Nitrogen, a surface trapped charge density of $1 \times 10^{11} \text{ cm}^{-2}$ and a fixed charge density in gate oxide of $1 \times 10^{17} \text{ cm}^{-3}$. The p-type and n-type Polysilicon gate material is doped with Boron and Phosphorus of $1 \times 10^{19} \text{ cm}^{-3}$ respectively, and their workfunctions calculated from the doping level. The channel doping concentration and depth are optimised to achieve maximum mobility in the enhancement mode MOSFET.

Fig.1 shows that V_{th} decreases with increasing channel doping concentration, N_c , and depth of channel. When the product of N_c and depth exceeds $7.5 \times 10^{11} \text{ cm}^{-2}$ V_{th} becomes negative, i.e. depletion mode. In the case of enhancement mode, the best mobility is gained at N_c of $2 \times 10^{16} \text{ cm}^{-3}$ and depth of 0.2-0.3um (Fig.1, 2). Electron distribution from the surface to the bulk clearly shows that the available channel conduction electron density increases with N_c (Fig.3). Fig.4 shows a comparison of mobility between gate materials with different workfunction. At the same V_{th} , n-polysilicon and AL gate show almost the same mobility (due to similar workfunction), while the p-polysilicon gate has about $50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ higher mobility. At a threshold voltage of 1V this represents a factor of 2 improvement, thus demonstrating the potential for improved performance with a p-polysilicon gate.

The final paper will report a new type of channel mobility model, which is based on the density of interface states, D_{IT} , and the modeling of surface deep levels. This model seems to have good agreement with experimental data. It is believed that the model is the best way to describe the SiC channel mobility because the main cause of low mobility is high D_{IT} .

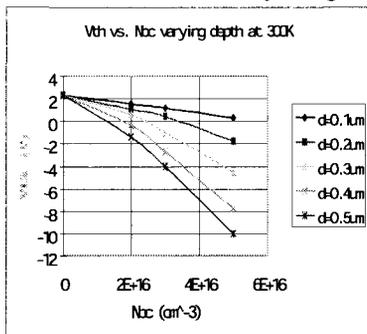


Fig.1 V_{th} vs. N_c with depth

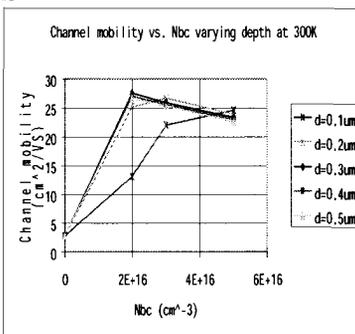


Fig.2 Mobility vs. N_c with depth

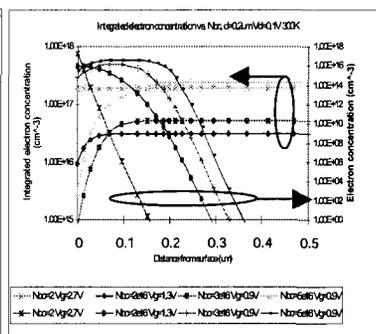


Fig.3 Electron concentration

Acknowledgement

This work was performed under the management of FED as a part of Ultra-Low Loss Power Device Technology Project supported by NEDO and was supported in part by the UK Engineering and Physical Sciences Research Council under research grant GR/L62320.

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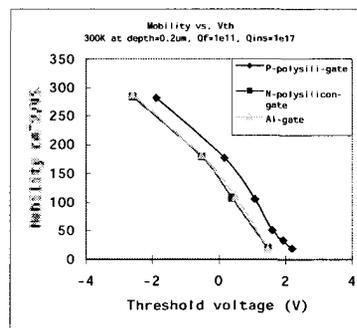


Fig.4 Mobility

Theory of Super-Junction Structure Forward Characteristics and Comparison of 4H-SiC and Si

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Abstract

Super-junction structure (SJS) can realize very low on-resistance in Si [1] and 4H-SiC [2] FET devices. The practical limits to device operation are, however, determined by a combination of the electrical characteristics of the device and the thermal constraints of the device and packaging technology. In this paper a formula for the forward drain current density (Jd) versus on-state voltage (Von) taking account of the built-in potential (Vbi) and the doping imbalance error between pillars (err=Na/Nd-1) is developed. Von and the product of Jd and breakdown voltage Vbr are studied and comparisons made between 4H-SiC and Si.

The relationship between Jd and Von is derived from junction field effect transistor (JFET) theory [3] in which the p-pillar acts like the JFET gate. The resulting relationship gives good agreement with TCAD at low voltage in the area of on-state (Fig.1).

The maximum package power dissipation is assumed to be 500W/cm² for Si and 1000W/cm² for SiC. Von is taken from the value where the Jd-Von line and the power line (Jd*Von) cross. In the case of an optimized structure and with the limitation of a minimum pillar width of 1um for realistic condition, we have found that Von remains same at low voltage and low imbalance error (Fig.2). With err=0.1 SiC 720V and Si 72V devices have about 0.2V and 0.3V Von respectively, and are both about half values of conventional FET devices at the same power dissipation. SiC 7200V and Si 720V devices display Von values of about 2V and 4V respectively (one third of conventional devices).

Jon*Vbr (switched VA product) versus Vbr (Fig.3) is one good way of measuring device performance. Fig.3 shows that for SJS the VA product increases in proportion to the square root of Vbr, while for conventional FET devices it decreases. This demonstrates the excellent performance potential of SiC SJS.

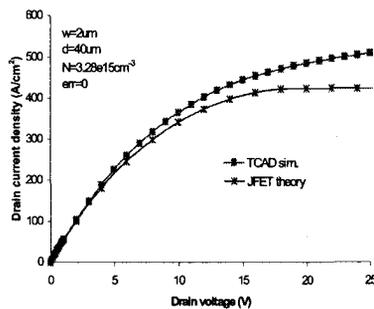


Fig. 1

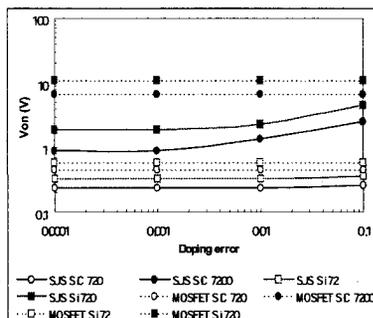


Fig.2

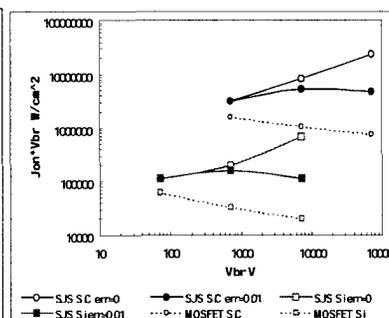


Fig.3

Acknowledgement

This work was performed under the management of FED as a part of Ultra-Low Loss Power Device Technology Project supported by NEDO and was supported in part by the UK Engineering and Physical Sciences Research Council under research grant GR/L62320.

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