

## Poster Session III

### **Surface Morphology of GaN Epilayer with Si x N 12 Buffer Layer Grown by Ammonia-Source MBE**

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### **Metalorganic Chemical Vapor Deposition Growth of GaN Thin Film on 3C-SiC/Si(111) Substrate Using Various Buffer Layers**

C. I. Park, J. H. Kang, K. C. Kim, K. S. Nahm, K. Y. Lim, E. K. Suh  
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**4H-SiC pn Diode Grown by LPE Method for High Power Applications**

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**Reactive Ion Etching Process of 4H-SiC Using the CHF<sub>3</sub>/O<sub>2</sub> Mixture with a Post O<sub>2</sub> Plasma Etching Process**

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## Surface Morphology of GaN Epilayer with Si<sub>x</sub>N<sub>1-x</sub> Buffer Layer Grown by Ammonia-source MBE

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GaN and related semiconductors such as AlN and InN are attractive materials for optoelectronic and high-temperature electron devices. The alloyed semiconductor of GaN, AlN and InN covers a wide bandgap range from 1.9 to 6.2 eV, promising for light emitting diodes and laser diodes. The GaN materials have also the high electron drift velocity and the high chemical stability, promising characteristics for high-temperature electron devices. Thus the growth of the high quality films is important for achieving the high performance of these devices, and there have been intensive growth studies using metal-organic chemical deposition (MOCVD), and molecular beam epitaxy (MBE).

In comparison with MOCVD technique, MBE technique has the advantages in growing the quantum structure including abrupt interface with good uniformity. However, due to the large lattice mismatch, heteroepitaxy of GaN on sapphire substrates results in the high density of dislocations, and in order to improve the film quality, it is necessary to employ additional techniques such as GaN or AlN low temperature buffer layer [1], migration enhanced epitaxy [2], In exposure [3], SiN buffer layer [4] and so on.

The usage of thin SiN films has been mainly employed in MOCVD system [4] and the significant improvement of the crystal quality has been reported. In this study, we employed the SiN buffer layer for NH<sub>3</sub>-source MBE technique.

The GaN films were grown by a Riber 32 MBE system with a reflection high-energy electron diffraction (RHEED) setup. Ga, Al and Si fluxes were supplied by Knudsen cells. NH<sub>3</sub> was supplied through an injector maintained at 300 °C. The flow rate of ammonia was adjusted using a 50 SCCM mass flow controller. The chamber pressure during films growth was 5 - 6 × 10<sup>-6</sup> Torr. The (0001) sapphire substrates with 3000 Å Mo film deposited on the backside were used, and the substrate temperature was monitored by a pyrometer.

First, GaN epilayers without SiN buffer layer were grown as follows. The nitridation of the sapphire substrates were performed by exposing the surface to an ammonia flow of 20 SCCM at a substrate temperature of 900 °C for 10 min. The low-temperature (LT) GaN buffer layers with 300 - 500 Å thickness were then grown at 600 °C, and annealed at 900 °C for 20 min. The growth rate of the LT GaN buffer was about 0.2 μm/h. The 1-μm thick GaN layers were then grown at the growth rate of 0.6 - 1.0 μm/h. The SEM image of the surface is shown in Fig. 1. The hexagonal surface features with a size of about 2 μm were observed. The Hall mobilities of the GaN films without SiN buffer layer were 100 - 120 cm<sup>2</sup>/Vs. The high-

resolution X-ray diffraction (XRD) measurement was performed, and the full width at half-maximum (FWHM) of the  $\omega$ -rocking curve were 830 - 860 arcsec. The FWHM of  $\omega$ -2 $\theta$  scans were 70 - 80 arcsec.

Next we investigated the effects of the thin SiN buffer layers. Just after the nitridation of the sapphire substrates, the SiN thin films were deposited by exposing sapphire substrate to Si and NH<sub>3</sub> flux for 10 min. The flow rate of NH<sub>3</sub> was kept at 20 SCCM, and the temperature of Si Knudsen cell was 1050 - 1200 °C. On this SiN thin films, The LT GaN buffer layers were then deposited and annealed using the same condition as has been mentioned. The 1- $\mu$ m thick GaN layers were then grown. During the growth, the RHEED patterns were more streakylike in comparison with the cases without thin SiN buffer layer. Figure 2 shows the SEM image of the surface of the grown GaN layer when the temperature of Si Knudsen cell was 1200 °C. The surface morphology in Fig. 2 exhibits a step-like surface structure. We also found the improvement of the Hall mobility. The Hall mobilities of the GaN films with the thin SiN buffer were 150 - 160 cm<sup>2</sup>/Vs. In terms of the XRD measurement, the FWHM of the  $\omega$ -rocking curve were about 700 arcsec. The FWHM of  $\omega$ -2 $\theta$  scans were 60 - 70 arcsec.

The details will be discussed at the presentation.

#### References

- [1] N. Grandjean, M. Leroux, M. Laügt and J. Massies, *Appl. Phys. Lett.* 71(1997), p. 240.
- [2] K. Kushi, H. Sasamoto, D. Sugihara, S. Nakamura, A. Kikuchi and K. Kishino, *Mater. Sci. and Eng.* B59(1999), p. 65.
- [3] X. Q. Shen, S. Tanaka, S. Iwai and Y. Aoyagi, *Jpn. J. Appl. Phys.* 37(1998), p. L637.
- [4] S. Sakai, T. Wang, Y. Morisha and Y. Naoi, *J. Cryst. Growth*, 221(2000), p. 334.

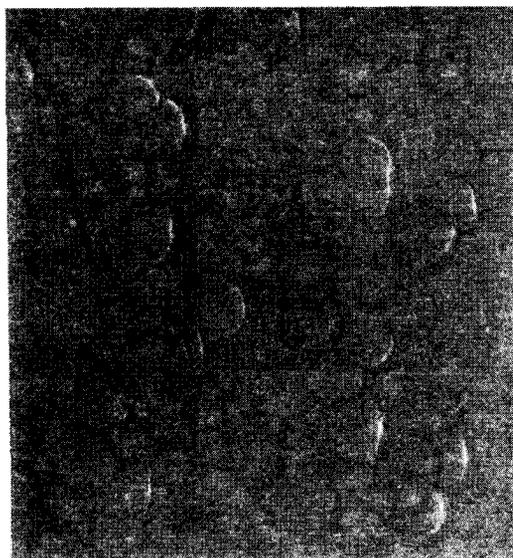


Fig. 1. The SEM image of GaN epilayer grown without SiN film.



Fig. 2. The SEM image of GaN epilayer grown with SiN film.

## Metalorganic chemical vapor deposition growth of GaN thin film on 3C-SiC/Si(111) substrate using various buffer layers

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A key issue for the growth of GaN has been the lack of an ideal substrate. Most GaN has been grown on sapphire ( $\alpha$ -Al<sub>2</sub>O<sub>3</sub>) since GaN substrates are not readily available [1]. The growth of high quality GaN films on silicon substrates using a SiC intermediate layer has been stimulated because of the irreplaceable merits of the Si wafer such as low cost, high surface quality, large area wafer availability, high conductivity and well-established processing techniques [2-5].

In this work, we have investigated the growth of high quality GaN films on 3C-SiC/Si(111) substrates using GaN, AlN, or GaN/AlN superlattice buffer layers with a MOCVD technique. 3C-SiC(111) films were grown on Si(111) substrates using tetramethylsilane (Si(CH<sub>3</sub>)<sub>4</sub>, TMS). GaN films were grown on 3C-SiC/Si(111) in a low pressure commercial MOCVD system using trimethylgallium (TMG), trimethylaluminum (TMA) and ammonia (NH<sub>3</sub>). Fig. 1 shows AFM images for GaN films grown with and without buffer layers. When the GaN films grow without any buffer layer and with a 200 Å GaN buffer layer, they produce very rough surfaces (see Fig. 1(a) and (b)). However, the surface morphology is significantly improved for GaN films grown with AlN and superlattice buffer layers as can be seen in Fig. 2(c) and (d). Root mean square (RMS) roughness of the surface was about 4.21 Å for GaN films grown with superlattice buffer layers. Figure 2 shows XRD spectra for GaN films grown on SiC/Si(111) substrate using various buffer layers. For the GaN film grown directly on 3C-SiC/Si substrate, XRD spectrum shows a peak of wurtzite GaN(0002) at  $2\theta = 34.4^\circ$  with various small peaks, indicating the growth of polycrystalline-like GaN. However, the nature of polycrystallinity begins to decrease when grown on buffer layers. Consequently, the GaN film grown with a superlattice buffer layer (sample D) shows only a peak associated with the GaN(0002). Raman spectrum for the GaN films grown with superlattice buffer layer also showed the growth of high quality GaN films. Low temperature PL measurements showed that peaks associated with band edge emission and donor-acceptor pair recombination ( $D^0A^0$ ) were observed from GaN films grown with and without GaN or AlN buffer layers, whereas GaN films grown with the superlattice buffer layer exhibited a strong band edge peak with very weak  $D^0A^0$  emission. The surface morphology and structural and optical properties of the GaN films were well correlated for the evaluation of GaN crystal quality.

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## References

- [1] S. Nakamura, *Jpn. J. Appl. Phys.* 30 (1991) L1705.
- [2] J. Wu, H. Yaguchi, H. Nagasawa, Y. Yamaguchi, *Jpn. J. Appl. Phys.* 36 (1997) 4241.
- [3] Y. H. Mo, S. H. Yang, K. C. Kim, W. H. Lee, K. S. Nahm, E.-K. Suh, K. Y. Lim, *J. Korean Phys. Soc.* 34 (1999) s364.
- [4] J. Wu, H. Yaguchi, H. Nagasawa, Y. Yamaguchi, K. Onabe, Y. Shiraki, R. Ito, *J. Cryst. Growth* 189/190 (1998) 420.
- [5] A. J. Steckl, J. Devrajan, C. Tran, R. A. Stall, *Appl. Phys. Lett.* 69 (1996) 2264.

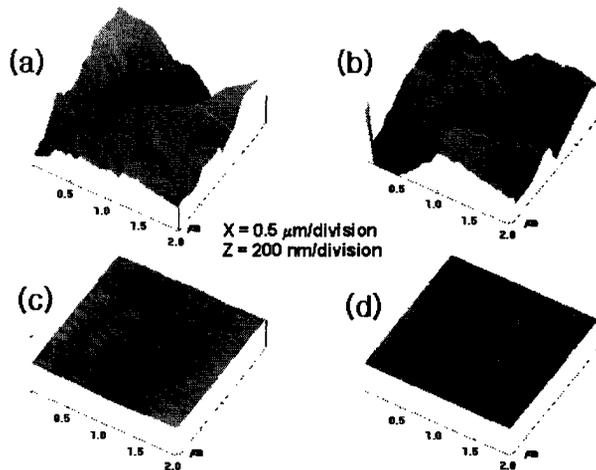


Figure 1. AFM images for GaN film surfaces grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer consisted of four periods of 32 Å GaN layer and 20 Å AlN layers.

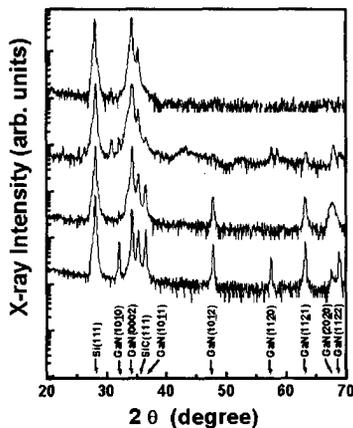


Figure 2. Wide angle range XRD spectra for GaN films grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer.

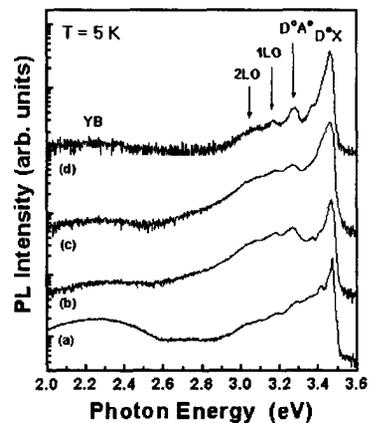


Figure 3. Low temperature (5 K) photoluminescence (PL) spectra for GaN films grown on SiC/Si(111) substrate: (a) without buffer layer, (b) with 200 Å GaN buffer layer, (c) with 200 Å AlN buffer layer, and (d) with superlattice buffer layer.

## Catalytic growth of high quality GaN micro-crystals

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The preparation of amorphous GaN and GaN powder crystals is of great interest in sublimation growth of bulk GaN as well as in nano-scale optical technology [1-3]. It has been prospected that preparation of nano-crystalline GaN structures such as quantum wires or quantum dots is one of the most promising approaches for improving the performance of optical devices based on III-nitrides [4].

In this work, GaN micro-crystals were catalytically grown using Ni-mesh by direct reaction of gallium and ammonia in a homemade quartz tubular reactor. The Ni catalyst was completely dipped in the Ga melt during the growth. The grown GaN crystals were separated from as-grown mixture by dissolving unreacted Ga and Ni catalyst in HCl solution. Figure 1 shows that the growth rate of the GaN crystals increases as the reaction temperature rises from 1000 to 1100 °C and the dependency of the growth rate on the temperature is much more significant in the presence of Ni catalyst. The use of the catalyst induced the increase of GaN crystal size. Figure 2 shows the TEM dark-field micrographs and the corresponding selected area diffraction pattern (SADP) along the electron beam direction  $\mathbf{B}=[0110]$  with the reflection vectors  $\mathbf{g}=0002$  (a) and  $\mathbf{g}=\bar{2}110$  (b), respectively. Dark field micrographs show that the crystal consists of 2H hexagonal single crystal without any grain boundary. PL spectrum showed a strong band edge emission at the energy position of  $\sim 3.35$  eV with FWHM of  $\sim 115$  meV. The time-resolved photoluminescence measurements also reveal  $\tau_1 = 22$  and  $\tau_2 = 109$  ps for the catalytically grown GaN nano-crystals (Fig. 3), indicating the growth of high quality GaN. In order to investigate the effect of the Ni-catalyst on the cracking of  $\text{NH}_3$  and the growth of GaN, the gas composition in the reactor was insitu analyzed using a quadrapole mass spectrometer (QMS). It was observed that reactive nitrogen species produced in the presence and absence of the Ni catalyst are different each other and the growth of GaN mostly occur by the reaction of Ga with atomic N adsorbed on Ni catalyst.

In conclusion, the Ni-catalyst stimulated the decomposition of  $\text{NH}_3$  gas into the chemically active nitrogen atoms directly participating in the growth of GaN, resulting in the increase of the growth rate of the GaN crystals.

### Acknowledgements

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### References

- [1] S.Kurai, T.Abe, Y.Naoi, and S.Sakai, Jpn. J. Appl. Phys., 35 (1996) 1637.

- [2] V.J.Leppert, C.J.Zhang, H.W.H.Lee, I.M.Kennedy, and S.H.Rishud, Appl. Phys. Lett., 72 (1998) 3035.
- [3] K.E.Gonsalves, S.D.Rangarajan, G.Carlson, J.Kumar, K.Yang, M.Benaissa, and M.Jose-Yacanan, Appl. Phys. Lett., 71 (1997) 2175.
- [4] T. J. Goodwin, V. J. Leppert, S. H. Risbud, I. M. Kennedy, H. W. H. Lee, Appl. Phys. Lett., 70 (1997) 3122.

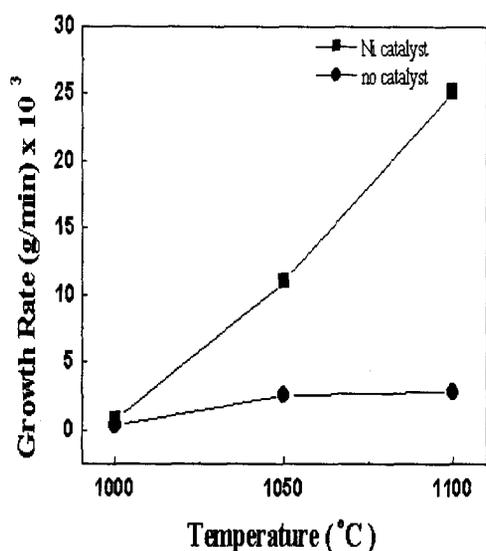


Figure 1. The growth rate of GaN crystals as a function of growth temperature at 1atm with 50sccm NH<sub>3</sub>. (■ : in the presence and ● : absence of Ni-mesh catalyst).

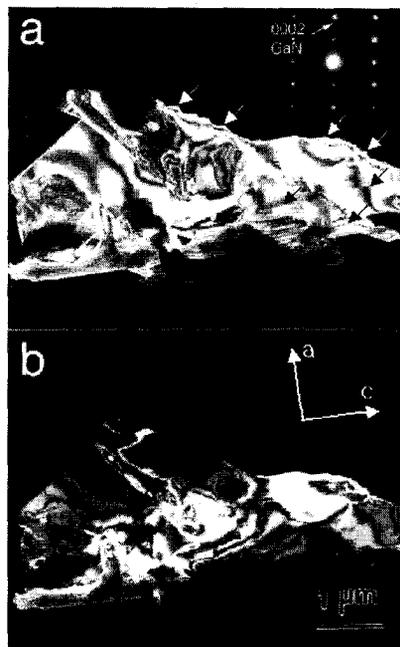


Figure 2. The dark-field micrographs and the corresponding selected area diffraction pattern (SADP) along the electron beam direction  $B=$  with the reflection vectors  $g=0002$  (a) and  $g=2110$  (b), respectively.

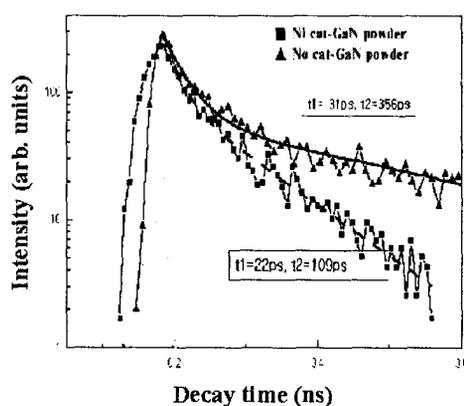


Figure 3. Photoluminescence decay for the catalytically grown GaN nano-crystals.

## Crystallographic Growth Models of Wurtzite-Type Thin Films on 6H-SiC

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Epitaxial growth of GaN has been tried using various kinds of substrates so far. Of all the substrate,  $\text{Al}_2\text{O}_3$  has been widely used for the GaN growth. Besides  $\text{Al}_2\text{O}_3$ , SiC is also expected as one of the most suitable substrates for the GaN growth, since SiC has a small mismatch in the lattice parameters with GaN and has good thermal stability under controlled atmospheres during the GaN growth. Both 6H-SiC and GaN having wurtzite structure belong to the same space group ( $P6_3mc$ ). The lattice parameters are as follows :  $a=3.08$ ,  $c=15.12 \text{ \AA}$  for 6H-SiC and  $a=3.19$ ,  $c=5.18 \text{ \AA}$  for GaN. SiC has two opposite surface polarities along [001] direction. The main objective of our research was to establish a crystallographic growth model of GaN on the  $(00\cdot1)$ 6H-SiC with different polarities of Si and C surfaces.

### Growth model of GaN on $(0001)_{\text{Si}}$ SiC

Fig.1(a) shows the surface structure of  $(00\cdot1)_{\text{Si}}$ SiC. Since coulomb attraction works between positive silicon ions and negative nitrogen ions, nitrogen atoms are deposited on the  $(00\cdot1)_{\text{Si}}$ SiC in the first growth step. Because of the covalent nature of SiC and GaN, nitrogen atoms deposit just above silicon atoms and  $\text{Si}(3\text{C},\text{N})$  tetrahedra are formed (Fig.1(b)). In the second growth step, three gallium atoms bond with one nitrogen atom and  $\text{N}(\text{Si},3\text{Ga})$  tetrahedra are formed as shown in Fig.1(c). In the third growth step, nitrogen atoms are deposited directly above gallium atoms and  $\text{GaN}_4$  tetrahedra are formed (Fig.1(d)). Growth steps second and third should repeat alternatively and this will result in a complete wurtzite-type GaN structure. The Ga-N bond along the  $c$ -axis direction is weak compared to other three Ga-N bonds in a tetrahedron. The final layer of GaN film would be a gallium layer. That is, Ga-terminated GaN films are grown on  $(00\cdot1)_{\text{Si}}$ SiC.

### Growth model of GaN on $(0001)_{\text{C}}$ SiC

Fig.2(a) shows the surface of  $(00\cdot\bar{1})_{\text{C}}$ SiC. Gallium atoms are deposited on the  $(00\cdot\bar{1})_{\text{C}}$ SiC in the first growth step for the same reason as described in the previous section. Ga atoms deposit just above carbon atoms and  $\text{C}(3\text{Si},\text{Ga})$  tetrahedra are formed (Fig.2(b)). In the second growth step, each nitrogen atom is deposited onto three gallium atoms and  $\text{Ga}(\text{C},3\text{N})$

tetrahedra are formed (Fig.2(c)). In the third growth step, gallium atoms are deposited directly above nitrogen atoms and  $\text{NGa}_4$  tetrahedra are formed (Fig.2(d)). In this case, the final layer of the GaN film would be a nitrogen layer. This indicates that N-terminated GaN films are grown on  $(00\cdot\bar{1})_{\text{C}}\text{SiC}$ .

These modeling simulations were discussed from the Poling laws, and compared with the results obtained in the GaN growth on SiC substrates in literatures.

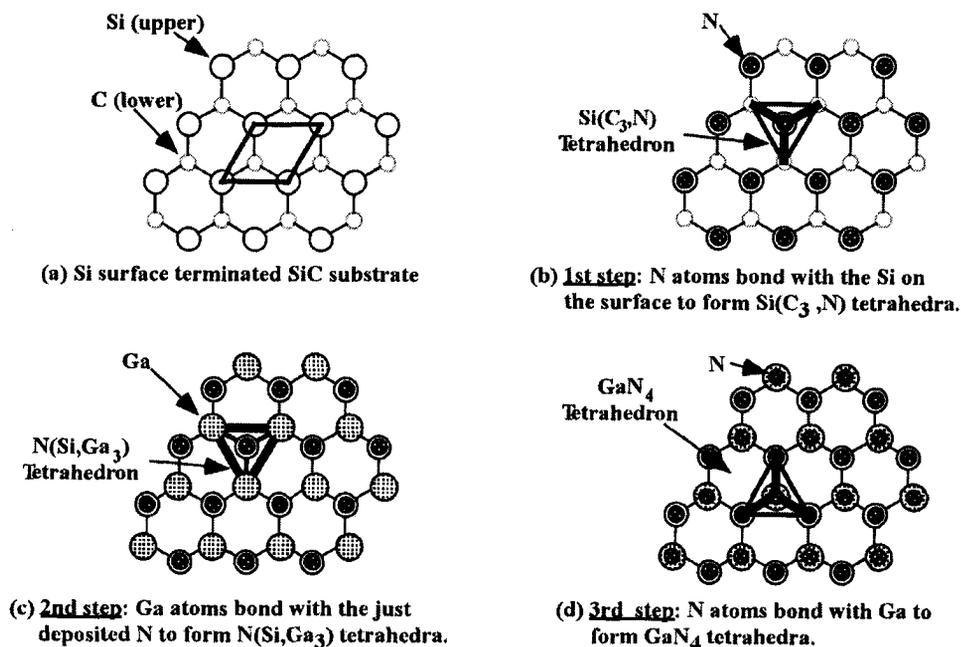


Fig.1 Growth of GaN on  $(0001)_{\text{Si}}\text{SiC}$

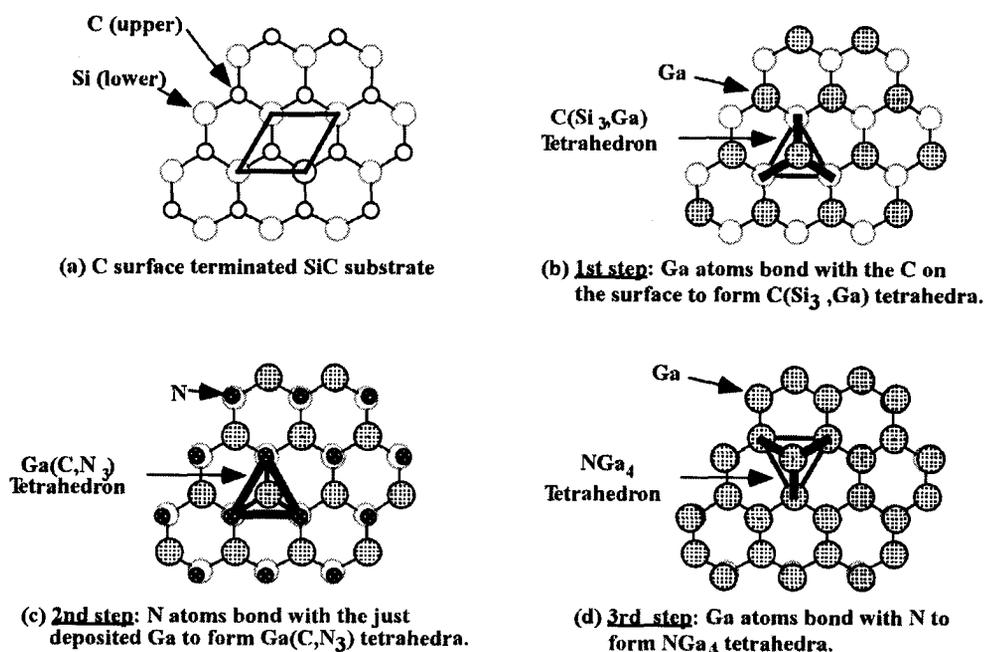


Fig.2 Growth of GaN on  $(0001)_{\text{C}}\text{SiC}$

**Structural properties of single crystalline solid solution  $(\text{SiC})_{1-x}(\text{AlN})_x$  obtained by sublimation epitaxy .**

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**Abstract**

Solid solutions  $(\text{SiC})_{1-x}(\text{AlN})_x$  - new semiconductor materials obtained in single crystalline form in every interval composition [1]. SiC and AlN form non - stop series of solid solution with a width of band gap from 3-6eV. which during definite composition have a direct gap structure [2]. Excluding this solid solutions  $(\text{SiC})_{1-x}(\text{AlN})_x$  inherits unique mechanical, chemical and thermal properties from silicon carbide. That's why, presents perspective application of them in instruments, working in experimental condition in short wave region of optical range . Especially perspective solid solutions  $(\text{SiC})_{1-x}(\text{AlN})_x$  in instruments, based on heterojunctions (injectional lasers, light diodes, photoreceivers,..etc). As such near parameters of lattices and coefficients of temperature expansions SiC and  $(\text{SiC})_{1-x}(\text{AlN})_x$  allow obtaining heterojunctions on their base with lesser number of defects on heteroboundary.

This work was dedicated in the learning of processes of growth epitaxial layers

$(\text{SiC})_{1-x}(\text{AlN})_x$  from gaseous phases methods of sublimation and investigation of structural properties depending on technical parameters of growth.

Single crystalline epitaxial layers  $(\text{SiC})_{1-x}(\text{AlN})_x$  grown on substrates SiC polytype 6H in the temperature range of 2300-2550K at the pressure of  $\text{N}_2+\text{Ar}$  mixture from  $2 \cdot 10^4$ - $8 \cdot 10^4$  Pa in the zone of growth .

Sublimation etching surface substrates in surplus vapors Si and next growth epitaxial layers in nonstoppable process allows to decide problem of defectness in transitional layers on the boundaries of substrates epitaxial layers, form due to the passivation of surfaces substrate of carbon during the dissociation of SiC.

Definite dependence on growth speed, composition of epitaxial layers from technological parameters. Establishment, which effected on the composition of growing layer of solid solutions  $(\text{SiC})_{1-x}(\text{AlN})_x$  show the relation of partial pressure of argon and nitrogen in the growth zone. Growth speed increase partial pressure  $P_{\text{N}_2}$  and decreases with the increase in temperature improves the structure completely of the layers.

Investigation shows possibility of controlling types of electrical conductivity with a change in partial pressure of  $\text{N}_2$  in the working chamber. In this work it is shown the method used in obtaining anisotype heterostructures  $n\text{-SiC}/p\text{-}(\text{SiC})_{1-x}(\text{AlN})_x$  in nonstoppable system of growing layers.

Polytype structures and completion of epitaxial layers depend on the contents of AlN. Layer with  $x < 0.4$  have high completion but with increase in AlN structural completion deteriorates and also during  $x \geq 0.65$  observed block structure and high nonhomogeneous composition in volume and in surface.

Volume homogeneity was formed and identified by laser introsopic method. In this work we present results of the investigation of the interaction of radiation of nitrogen laser ( $P=15\text{-}20\text{kwatt}$ ,  $V=120\text{mvolt.}$ ,  $\lambda=0.337\mu\text{m}$ ) on the dynamic reorganization of structural defects in epitaxial layers. It is found that the increase in concentration centers of radiation recombinants intensive luminescence centers, forming and burning of defects.

### References

1. G. K. Safaraliev, Sh. A. Nurmagomedov, Yu. M. Tairov, V. F. Tsvetkov, Patent, No. 1297523, Russia, 1986.
2. A. N. Pikhin, G. K. Safaraliev, Sh. A. Nurmagomedov, Yu. M. Tairov, V. F. Tsvetkov, Sov. Tech. Phys. Lett., 12, 1043, 1986.

**PHYSICS OF HETEROEPITAXY AND HETEROPHASES**

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Because of the differences in the elastic, geometric and thermal properties of host materials involved in modern heteroepitaxial growth, the interfaces of the elaborated structures can be of variable quality. It is well known that materials presenting large lattice mismatch develop misfit strains at their interfaces. Beyond the critical thickness of the growing overlayer, extended defects as misfit dislocations can be created and then can propagate into the overlayer.

We have performed a theoretical approach which enables (i) to evaluate the best choice of host materials for heteroepitaxy and (ii) to propose a valuable strategy for optimizing their interfaces. The essential idea of the theory is based on the relationship between strain gradient and dynamics as shown by elasticity theory equations. From these equations we can identify the S factor -  $S=f(C_{ij})/\rho$ , where  $f(C_{ij})$  are the effective elastic constants and  $\rho$  the density - as the important parameter of the theory. S must be considered within an approach which takes account not only of the mismatch of the lattice parameters of the host materials, but also of the difference in their elastic-density features. The theory implies interface continuity conditions which must be fulfilled by the host material's relevant physical properties.

We have considered a wide range of heterosystems including  $Si_{1-x}C_x/Si$ ,  $Si_{1-x-y}C_xGe_y/Si$ , 3C-SiC/Si, AlN/3C-SiC, GaN/3C-SiC, ... In heterostructures where a large misfit exists between the substrate and the overgrown material, the insertion of a transitional layer or the incorporation of foreign atoms aiming at improving the interface quality, may often be useful. In this case, we demonstrate that our approach can be used to predict the composition of such transitional layers. By applying the continuity conditions imposed by the present theory, i.e., by performing in-heterostructure semiconductor physics, we are then able to determine optimized choices which can be exploited in heteroepitaxial growth experiments.

## Formation of Epitaxial Mesa Structures on 4H-SiC (0001) and (11 $\bar{2}$ 0) Substrates

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Silicon carbide (SiC) is a potentially important candidate for high-power and high-frequency devices, owing to its excellent properties of wide bandgap, high electron saturation drift velocity, high thermal conductivity and high breakdown field. High-quality homoepitaxial layers can be obtained at 1200-1500 °C by chemical vapor deposition (CVD) utilizing "step-flow growth" on off-axis SiC (0001) substrates. Matsunami group has researched the growth mechanism of SiC on on-axis and off-axis 6H-SiC substrates[1]. The nucleation, lateral growth anisotropy, and effects of off orientation have been described utilizing mesa tables on 6H-SiC (0001) substrates[2]. In this paper, we report the formation of SiC epitaxial mesa structures on partly masked 4H-SiC substrates by a CVD method. The various influences on SiC mesa structure and polytypes of grown layers are investigated.

In this work, off-axis 4H-SiC (0001) 8° inclined toward  $\langle 11\bar{2}0 \rangle$  and (11 $\bar{2}$ 0) Si face substrates were used. Masked substrates for mesa growth were prepared using a photoresist by a conventional lithographic technique and annealing at 800 °C for 10 min in Ar. The annealed photoresist (0.5 μm-thick carbon layer) as a mask for mesa growth can be removed after growth by oxidizing at 1000 °C. Epitaxial mesas were grown at 1500 °C by atmospheric-pressure CVD using a SiH<sub>4</sub>-C<sub>3</sub>H<sub>8</sub> system in a horizontal water-cooled reactor. The flow rates of SiH<sub>4</sub>, C<sub>3</sub>H<sub>8</sub>, and H<sub>2</sub> were 0.15-0.30 sccm, 0.15-0.30 sccm, and 3.0 slm, respectively. These conditions have led to the corresponding homoepitaxial growth rates of 1.2-2.5 μm/h on maskless SiC substrates. The growth time was 30-60 min. SiC mesa epilayers were unintentionally doped with a C/Si ratio of 3, and characterized with a Nomarski microscope, a scanning electron microscope (SEM), and Raman scattering.

Figure 1 gives the Nomarski microscopic and SEM images before and after mesa growth on masked 4H-SiC substrates. Due to the anisotropy in the lateral growth rate, a circular opening before growth was deformed into a hexagonal mesa structure after CVD growth on the off-axis (0001) substrate (Fig.1(b)). Especially, along the [11 $\bar{2}$ 0] off-direction the hexagonal shape is sharper than the other equivalent directions. This is ascribed to an additional step-flow growth on the off-axis (0001) substrate compared to the growth on an on-axis substrate. A (0001) facet on the off-axis (0001) SiC substrate can be seen at the upstream side of step-flow on the SiC mesa structure as reported by Kimoto and Matsunami[2]. The (0001) facet broadened and the elongated hexagonal mesa structure became sharper with increasing the growth time. A grooved surface emerged at the upstream side of step-flow or in the vicinity of (0001) facet. On the masked 4H-SiC (11 $\bar{2}$ 0) substrate, the mesa structure after growth almost retained a circular shape (Fig.1(c)).

Figures 1(d) and (e) show the SEM images of SiC mesa structure on 4H-SiC substrates after the carbon mask was removed by thermal oxidation. The masked region was specular without surface degradation, resulting in the successful formation of SiC epitaxial mesa structures on SiC substrates. Since the surface migration of reactant species on the surrounding mask into the growth region occurred during the growth, the growth thickness profile across the patterned area shows a thicker periphery than the center of the patterned area.

As shown in Fig. 2, the lateral growths on the carbon mask are also observed by an SEM at the upstream and downstream sides of the  $[11\bar{2}0]$  off-direction. Due to the occurrence of additional step-flow growth along the  $[11\bar{2}0]$  off-direction, the lateral growth length on the carbon mask at the downstream side is larger than that at the upstream side.

On the off-axis (0001) masked substrate, 3C-SiC appeared on the SiC mesa structure at the upstream side of step-flow in the part of grooved surface, but only 4H-SiC epilayers without 3C-SiC were grown in the part of flat surface (downstream side of step-flow), which were verified by Raman scattering. On the  $(11\bar{2}0)$  masked substrate, however, no 3C-SiC was detected on the SiC mesa structure by Raman scattering. Circular SiC mesa structures with smooth morphology can be obtained on the masked  $(11\bar{2}0)$  4H-SiC substrate. Details of 4H-SiC homoepitaxy on partly masked substrates will be described in the presentation.

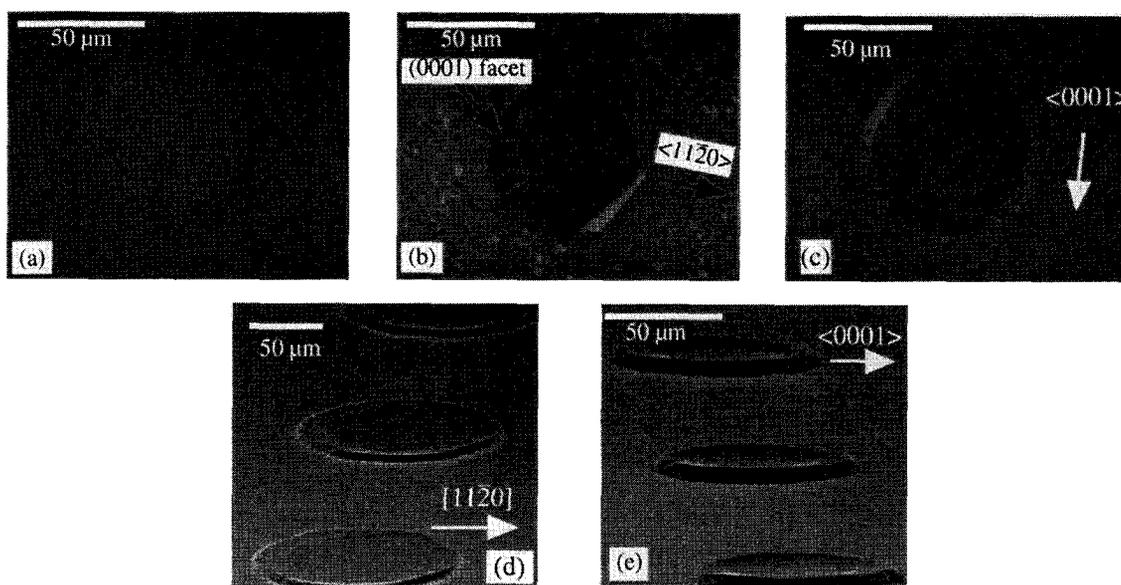


Fig. 1 Nomarski microscopic and SEM images of SiC mesa structure on 4H-SiC masked substrates: before growth (a), after growth on (b) off-axis (0001) and (c)  $(11\bar{2}0)$ ; SEM images grown on off-axis (0001) (d) and  $(11\bar{2}0)$  (e) substrates.

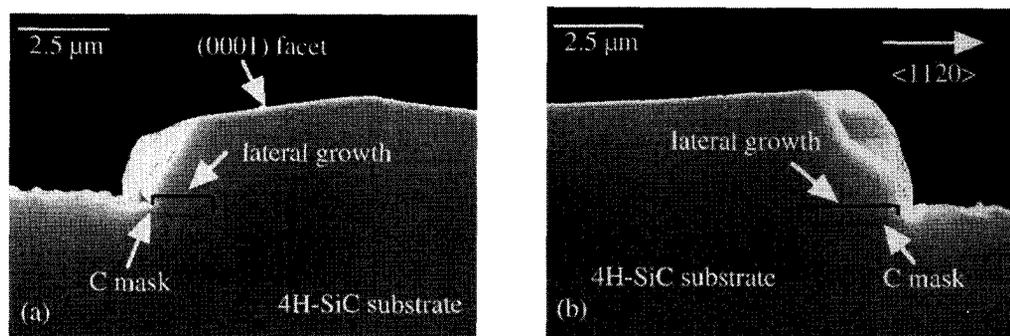


Fig. 2 Cross sectional images of SiC mesa structure with a diameter of 60  $\mu\text{m}$  grown on off-axis (0001) substrate. (a) at the upstream side and (b) at the downstream side of  $[11\bar{2}0]$  off-axis.

#### References:

- [1] H. Matsunami and T. Kimoto, Mater. Sci. & Eng. R20 (1997) 125-166.
- [2] T. Kimoto and H. Matsunami, J. Appl. Phys. 76 (1994) 7322.

## Growth of low doped 4H-SiC layers by sublimation epitaxy: effect of low doped SiC source material and tantalum in the growth environment

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Sublimation epitaxy is a technique for growth of thick epitaxial layers with growth rates up to 100  $\mu\text{m/h}$  while maintaining smooth as-grown surfaces and conditions for improved structural quality [1]. The remaining issue of avoiding introduction of impurities from the growth environment to the epitaxial layer is a challenging task. The purity of the solid polycrystalline SiC source material used for feeding the epitaxial layer during growth is the most critical issue in the growth of low doped SiC layers by sublimation epitaxy.

In this paper the influence of impurities, in particular the predominantly existing boron, in relatively pure source material and the effect of tantalum (which is used in the growth cell to getter carbon and avoid graphitization of the source and epilayer by increasing the Si/C ratio in the vapor) has been studied. The layers have been characterized using capacitance-voltage measurement, deep level transient spectroscopy, minority carrier transient spectroscopy and cathodoluminescence techniques to detect electrical characteristics of electron as well as hole traps and impurities. Sublimation epitaxy [2] was performed on the Si-face of 4H-SiC substrates with surfaces off-oriented  $8^\circ$  in the  $[11\bar{2}0]$  direction. The deposition rate was ranging from  $\sim 25 \mu\text{m/h}$  up to  $\sim 200 \mu\text{m/h}$  in the temperature intervall of 1725 to 1800°C. The layers are n-type with net carrier concentrations in the  $E15 \text{ cm}^{-3}$  range or low  $E16 \text{ cm}^{-3}$ .

One limitation in growth of low doped epilayers by sublimation techniques is that very high purity SiC source material (total impurity concentration  $<E15 \text{ cm}^{-3}$ ) and tantalum are not available. The available polycrystalline SiC wafers contain nitrogen, boron and aluminium as major impurities. The typical concentrations are given in Table I for three suppliers of polycrystalline SiC wafers (denoted source A, B and C in Table I). Even though the overall purity of source C is improved in comparison to other source materials, it still contains boron. This study mainly presents results from sublimation epitaxial growth using this source material and various tantalum foils of different thicknesses and purity.

	Thickness	Purity	B conc. [atoms/cm <sup>3</sup> ]	Al conc. [atoms/cm <sup>3</sup> ]	N conc. [atoms/cm <sup>3</sup> ]
Source supplier A			Low E16	E15	E17
Source supplier B			Low E18	.*	Low E16
Source supplier C			E15 - E16	.*	<E16
Ta foil 1	25 $\mu\text{m}$	99.997%			
Ta foil 2	250 $\mu\text{m}$	99.98%			
Ta foil 3	2 mm	99.999%			

TABLE I. Summary of purity of polycrystalline SiC source and Ta foil studied in the sublimation epitaxial growth, impurity levels assessed from SIMS measurements. \* - below detection limit.

The source of aluminium seems to be the tantalum foil. We will show that the thickness and purity of the tantalum foil are important to avoid aluminium. At optimized conditions the Al concentration of the layers is below the detection limit of SIMS ( $5 \times 10^{14} \text{ cm}^{-3}$ ) and aluminium is not observed in low-temperature photoluminescence or cathodoluminescence measurements. The concentration of boron in the epilayers increases with increasing growth time, Fig. 1. The shallow boron center is generally formed in epitaxial growth [3] and boron in this case is believed to occupy the silicon site in the SiC lattice. During sublimation epitaxy the initial effect of the Ta foil to getter carbon is probably decreasing and thus the Si/C ratio in the vapor is decreasing during growth. This provides conditions of increased incorporation of boron in the epilayer with decreasing Si/C ratio which is in agreement with studies of the site competition effect [4].

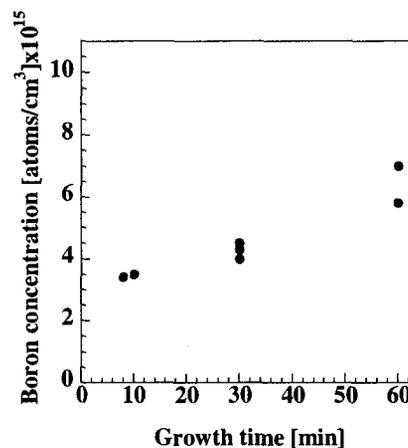


Fig. 1. Boron concentration in the layers vs growth time.

Most interestingly, in the electrical measurements we observe that the compensation level is low even though the boron concentration as measured by SIMS is in the same order as the nitrogen concentration or even higher while the layers still are n-type. This suggests that most of the boron is not electrically active. The amount of electrically active boron seems to depend on the concentration of boron in the epilayer. Investigations of deep levels in the epilayers indeed show presence of boron. Both shallow boron and deep boron D-centers are detected in the layers.

Electron trap (capture cross section)		$Z_{1,2}$	0.4-0.5 eV ( $2 \times 10^{10} \text{ cm}^2$ )	0.65 ( $3 \times 10^{16} \text{ cm}^2$ )	1.0 ( $2 \times 10^{14} \text{ cm}^2$ )
Sample type 1	Sample 1	$4.0 \times 10^{13}$	$2.7 \times 10^{13}$	$1.2 \times 10^{13}$	$3.0 \times 10^{13}$
	Sample 2	$2.4 \times 10^{13}$	$1.0 \times 10^{13}$	*	$6.0 \times 10^{12}$
Sample type 2	Sample 3	$2.5 \times 10^{13}$	*	*	*
	Sample 4	$4.0 \times 10^{13}$	*	*	*

Table II. Electron traps detected in two types of layers grown by sublimation epitaxy using source C, \* - below detection limit.

The concentration of the  $Z_{1,2}$  electron trap is in the order of  $\sim 2-4 \times 10^{13} \text{ cm}^{-3}$ , Table II. This is in similar concentration as measured in thick layers with similar doping but grown by high-temperature chemical vapor deposition at deposition rates ranging from 10 to 14  $\mu\text{m/h}$  at growth temperature 1700°C. The concentration of  $Z_{1,2}$  was decreased to  $1.3 \times 10^{13} \text{ cm}^{-3}$  in the best case [5]. Other electron traps, see Table II, are either in the E12 to E13 range or below the detection limit depending on the growth conditions. More details of the boron incorporation and electron trap formation related to sublimation epitaxy growth conditions will be presented.

- [1] M. Syväjärvi, R. Yakimova, H. Jacobsson, and E. Janzén, J. Appl. Phys. 88 (2000) 1407.  
 [2] M. Syväjärvi, R. Yakimova, M. Tuominen, A. Kakanakova-Georgieva, M.F. MacMillan, A. Henry, Q. Wahab, and E. Janzén, J. Crystal Growth 197 (1999) 155.  
 [3] A.A. Lebedev, Semiconductors 33 (1999) 107.  
 [4] D.J. Larkin, Phys. Stat. Sol. (b) 202 (1997) 305.  
 [5] T. Kimoto, S. Tamura, K. Fujihara, and H. Matsunami, Jap. J. Appl. Phys. part 2 (letters) 40, no. 4B (2001) L374.

### Aluminium incorporation in 4H-SiC layers during epitaxial growth in a Hot-Wall CVD system

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The incorporation of aluminium during epitaxial growth in a horizontal Hot-Wall CVD system has been studied in the concentration range from  $1 \times 10^{15} \text{ cm}^{-3}$  to  $2 \times 10^{18} \text{ cm}^{-3}$ . Epitaxial growth was performed using silane (2% diluted in  $\text{H}_2$ ) and propane (5% diluted in  $\text{H}_2$ ) as process gases and trimethylaluminium (TMA) as doping source. 4H-SiC (0001) substrates off-oriented  $8^\circ$  towards  $\langle 11\bar{2}0 \rangle$  with diameters of 35 mm (Cree Res. Inc., SiCrystal) were used. Before loading into the Hot-Wall CVD reactor the substrates were cleaned according to the RCA procedure followed by immersion in a HF solution in order to remove the surface oxide. The substrates were etched in hydrogen atmosphere at  $1550^\circ\text{C}$  adding a small quantity of propane to reduce the surface roughness and to remove a residual surface damage layer immediately before layer deposition.

Sources of residual background donor impurities, especially nitrogen, may be the susceptor, the thermal insulation and the reaction cell. To suppress the contamination by nitrogen the susceptor and the substrate holder were made of high purity graphite with SiC coating. Argon is available as a purge gas during loading and unloading the cell.

In accordance with the site competition mechanism the N incorporation can be controlled by the C/Si ratio [1]. In [2] this ratio was varied from 0.5 to 2 by keeping all growth parameters constant except the propane flow. The expected suppression of the N incorporation with increasing C/Si ratio was observed. For a C/Si ratio of 2, the N concentration is already lowered down to  $2 \times 10^{14} \text{ cm}^{-3}$ . Therefore the compensation by unintentional nitrogen doping can be neglected in the investigated p-type doping range.

Typical ranges of the most important parameters for the CVD-experiments are given in Table 1.

Table 1: Typical growth parameters

silane flow, 2% diluted in $\text{H}_2$	propane flow, 5% diluted in $\text{H}_2$	C/Si ratio	temperature	system pressure	hydrogen main flow
450 sccm	90 to 120 sccm	1.5 to 2	1550 to 1600 $^\circ\text{C}$	150 to 250 mbar	20 to 50 slm

The thickness of the epitaxial layers was determined by means of a Fourier transform infrared spectrometer and a software package (both obtained from BRUKER) evaluating the interference fringes which occur in the reflectance spectra. The chemical Al concentration was measured by secondary ion mass spectroscopy (SIMS) whereas the electrically active doping concentration was determined by capacitance-voltage (C-V) and Hall effect measurements. Because of the relatively high ionisation energy of the Al acceptors it was necessary to set the C-V measuring frequency down to 10 kHz for obtaining the full net acceptor concentration at room temperature.

The Al-doped epitaxial layers showed very smooth, mirror like surfaces. The net acceptor concentration estimated from C-V measurements agreed well with the Al concentration determined by SIMS. Hence, the passivation of Al acceptors by hydrogen seems to play no

significant role in comparison to boron doping [1] under our growth conditions. The Al concentration increased strongly with the Al partial pressure.

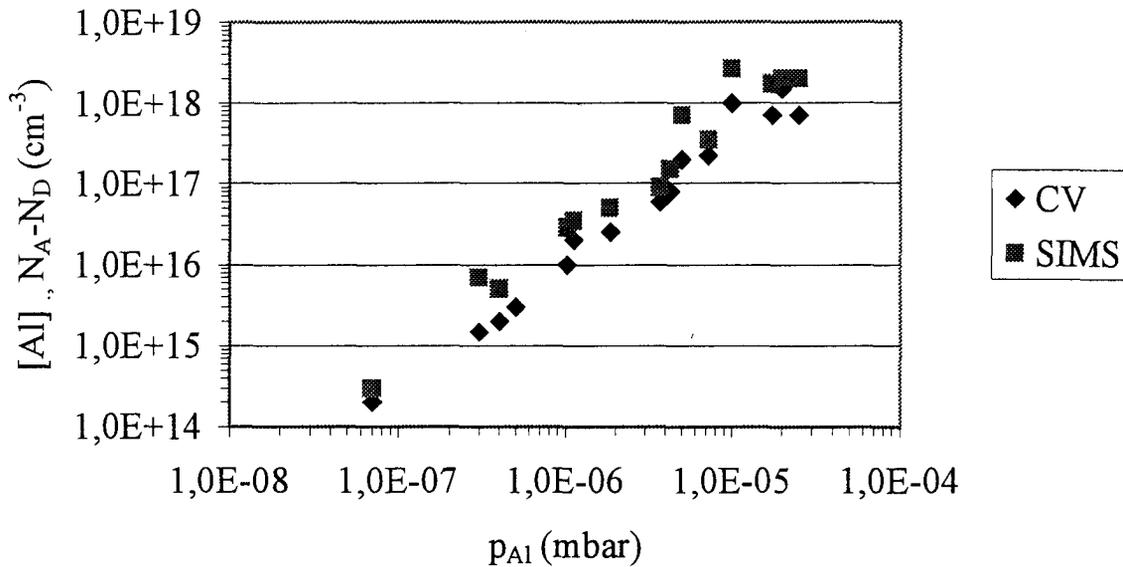


Fig. 1: Al and net acceptor concentration determined by SIMS and CV measurements, respectively, in dependence of the Al partial pressure

Hall effect investigations were conducted in van der Pauw arrangement. For the evaluation of electrically active Al concentrations, the Hall scattering factor for holes given in Ref. [3] was taken into account. The Al acceptor concentrations determined by Hall effect agree well with the values obtained from SIMS and CV measurements (not shown in Fig. 1). The Hall mobility values at room temperature ranging from  $66 \text{ cm}^2/\text{Vs}$  to  $110 \text{ cm}^2/\text{Vs}$  in epilayers with Al concentrations varying from  $10^{16} \text{ cm}^{-3}$  to  $10^{18} \text{ cm}^{-3}$  reflect the high quality of the grown Al-doped epilayers.

#### References

- [1] D. J. Larkin, *phys. stat. sol. (b)* **202** (1997), 305.
- [2] G. Wagner, K. Irmischer, *Mater. Sci. Forum* **353-356** (2001), 95.
- [3] N. Schulze, J. Gajowski, K. Semmelroth, M. Laube, G. Pensl, *Mater. Sci. Forum* **353-356** (2001), 45.

## Epitaxial growth of 4H-SiC with hexamethyldisilane HMDS

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SiC is a semiconductor of great interest for high temperature and high power electronic devices. For these applications, high growth rate material is important. In this work, we studied the homoepitaxial growth of 4H-SiC using hexamethyldisilane  $\text{Si}_2(\text{CH}_3)_6$  (HMDS) in place of the usual silane/propane system. HMDS is a single source C and Si precursor. It has been used for 3C-SiC heteroepitaxial growth [1, 2] in order to lower the growth temperature.

The growth was performed in a AP-CVD vertical reactor at 1600 and 1500°C on 8°off 4H-SiC substrates. In this system heteroepitaxy of 3C-SiC on Si at 1350°C with HMDS [3] leads to a maximum growth rate of 6  $\mu\text{m}/\text{h}$  for a C/Si ratio of 3.5. For comparison the maximum growth rate obtained with the silane/propane system in similar growth conditions is of 3  $\mu\text{m}/\text{h}$  only. Higher growth rates degrades the crystalline quality.

In this study HMDS was used as Si and C source or with addition of propane to vary the C/Si ratio from 3 to 15. Comparison was made with the silane/propane system. The HMDS flow rate was varied from 0.6 to 2.4 sccm, which corresponds to a silicon flow rate of 1.2 and 4.8 sccm respectively. The 4H-SiC layers were characterized by optical microscopy, atomic force microscopy (AFM), Raman spectroscopy and low temperature photoluminescence (LTPL). Infra-red reflectivity was used to evaluate the layer thicknesses.

The layers exhibit a defect density of about  $10^4$  per  $\text{cm}^2$  highly dependent on the substrate quality. The average AFM roughness (RMS) is 0.5 nm ( $10 \times 10 \mu\text{m}^2$  scans) for both HMDS/ $\text{C}_3\text{H}_8$  and  $\text{SiH}_4/\text{C}_3\text{H}_8$  precursors. The growth rate ranged from 2.6 to 10  $\mu\text{m}/\text{h}$  for HMDS flows of 0.6 to 2.4 sccm. The typical growth rate obtained with the silane (0.8 sccm) and propane mixture is 3.4  $\mu\text{m}/\text{h}$ . The growth efficiency related to the Si flow is then lower for the HMDS precursor. HMDS do not allow the growth with high C/Si ratios. Only the layers grown with a  $\text{C}/\text{Si} \leq 7$  exhibit a mirror like morphology whereas the C/Si ratio can be as high as 15 with silane/propane.

Raman spectra exhibit two FTO modes ( $796$  and  $776 \text{ cm}^{-1}$ ), the FLA ( $610 \text{ cm}^{-1}$ ) and the FLO ( $964 \text{ cm}^{-1}$ ) modes. The quality factor  $\kappa$  ratio [4], which is the ratio of the intensity of the two FTO modes  $796/776$  increases by increasing the C/Si ratio for both precursors. LTPL spectra show the N-BE zero-phonon line  $Q_0$  with phonon replica. The 77 meV phonon replica of the free exciton transition is also observed. A DAP Al-N band which was present on the substrate spectrum also appears. No difference in these characteristics have been observed between the silane and the HMDS system.

[1] K. Takahashi, S. Nishino, J. Saraie, J. Electrochemical Soc. 139 (1992) 3565.

[2] Y. Chen, K. Matsumoto, Y. Nishio, T. Shirafuji, S. Nisino, Mat. Sci. Eng. B61-62 (1999) 579.

[3] P. Aboughé-Nzé, Thesis, Université Lyon 1, january 2001.

[4] C.C. Tin, R. Hu, J. Liu, Y. Vohra, Z.C. Feng, J. Cryst. Growth 158 (1996) 509.

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## Low temperature preparation of $\alpha$ -SiC epitaxial films by Nd:YAG pulsed laser deposition

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### Introduction

Silicon carbide attracts a considerable attention since it is a promising material as high-temperature and wide band-gap semiconductor. Lots of efforts are devoted to synthesize high-quality single crystals for device applications. Recently, single crystals wafers of SiC with 2 inches diameter have been commercially available. However, because of high melting point, large size of SiC single crystal is still hard to synthesize and is very expensive. Many trials have been made for preparing epitaxial films as well. It needs high temperature process to fabricate the films for the same reason. In this study we report the fabrication of hetero-epitaxial  $\alpha$ -SiC films on sapphire substrates at considerably low temperature ( $T_s=820^\circ\text{C}$ ) by using pulsed laser deposition (PLD).

### Experimental

Silicon carbide (SiC) films were fabricated by a PLD method using the 4<sup>th</sup> harmonic (266nm) of Nd:YAG pulsed laser under the following conditions; the pulse frequency of 2Hz and the fluence of  $\rho=2\sim 20\text{J}/\text{cm}^2$ . Targets of sintered  $\alpha$ -SiC were purchased from Furuuchi Chemical Co. Fabrication was made on Si (111) and sapphire (001) single crystal substrates. After ultrasonic cleaning in acetone solvent, the substrate was set in a vacuum chamber and was heated to  $800^\circ\text{C}$  to clean the surface. All deposition was made under argon atmosphere of 50Pa, since oriented films did not grow in vacuum at low temperature. The crystallinity and orientation of the prepared films were examined by X-ray diffraction (XRD) using Cu  $K\alpha$  x-ray and reflection high-energy electron diffraction (RHEED), respectively.

### Results and Discussions

#### (i) $\alpha$ -SiC films on Si substrates

Figure 1 shows XRD patterns of the SiC films fabricated on Si (111) substrates at  $800^\circ\text{C}$  using a laser fluence of (a)  $20\text{J}/\text{cm}^2$  and (b)  $10\text{J}/\text{cm}^2$ . Two diffraction lines are observed at  $2\theta=38.08^\circ$  and  $81.56^\circ$  which are definitely assigned to XRD from  $\alpha$ -SiC (6H (103) and 6H (206) for 6H  $\alpha$ -SiC). Low temperature stable SiC ( $\beta$ ) does not give rise to signal at the angles. Full width at half maximum (FWHM) of the 6H (103) XRD line measured by  $\omega$ -scan was  $0.98^\circ$ , indicating the growth of one-axis oriented crystalline film. The growth temperature of the film is considerably low compared with that of other methods such as CVD ( $T_s\sim 1500^\circ\text{C}$ ). The reason may be as follows. Kinetic energy of ejected species in PLD process is much higher than that for other deposition process. The high kinetic energy may supplement the insufficiency of the energy for crystallization of the film. It is consistent with the result that the XRD peak intensity (which correlates to the crystallinity) increases with increasing the fluence of laser beam as seen in Fig.1, since increasing the laser fluence may lead to an increase of the kinetic energy.

At the present time it is not possible to fabricate the oriented films of  $\alpha$ -SiC in vacuum at low substrate temperature around 800°C. The reason is not clear, but might be as follows. Argon atoms collide with the ejected particles and may scatter the components with low kinetic energy. As the results only particles with high energy selectively reach the surface of the substrate and make high quality of films.

### (ii) $\alpha$ -SiC films on sapphire substrates

We have tried to fabricate SiC films on sapphire (001) substrates under the deposition conditions of  $T_s=820^\circ\text{C}$  and  $\rho=20\text{J}/\text{cm}^2$ . Formation of SiC films with c-axis orientation was confirmed by XRD. The films have different orientation from that on Si substrates. Figure 2 shows RHEED patterns of a sapphire substrate and the film deposited on it. Before the deposition, two kinds of diffraction patterns are alternatively observed by every 30° rotation (Fig.2 (a) and (b)), showing the  $C_6$  symmetry. The direction of the incident electron-beam for the images (a) and (b) is [100] and  $[\bar{2}10]$  of the substrate, respectively. After the deposition of the SiC, the diffraction pattern (a) turns to the dotted pattern with large separation (Fig.2 (c)). The pattern (d) is obtained at the direction where the image (b) was observed for the substrate. These results indicate that the film has the same symmetry as the substrate. Lattice constant of the film was estimated to be  $\sim 3.02\text{\AA}$  from the separation between dotted lines. It agrees with the reported value ( $a=3.08\text{\AA}$  for  $\alpha$ -SiC). These results indicate the epitaxial growth of SiC films. It is also found from the RHEED patterns that hexagonal lattice of SiC (001) does not have the same alignment as sapphire unit lattice (solid line in Fig.3) but have the same orientation as the oxygen sub-lattice of sapphire (dotted line in Fig.3) which is rotated by 30° against the sapphire hexagon. The results are reasonably explained by the good lattice matching of SiC (001) with the oxygen sub-lattice of sapphire as seen in Fig.3 (The mismatch is only 4.1%).

SiC films fabricated on Si substrates showed no RHEED patterns except for Laue ring which is characteristic of polycrystalline films. It might be because of the large lattice mismatch of 19.8% between the film and Si (111).

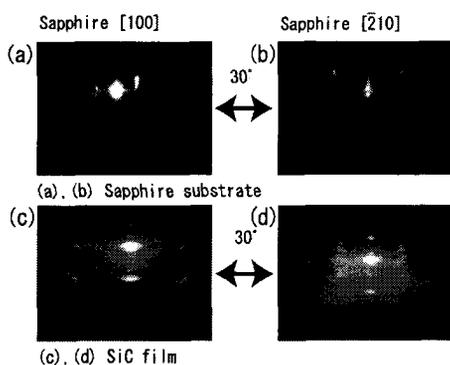


Figure 2. RHEED patterns of SiC film on sapphire substrate (a), (b) before and (c), (d) after deposition.

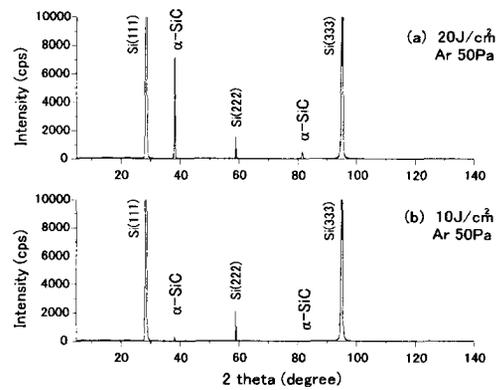


Figure 1. XRD patterns of SiC films fabricated on Si (001) at  $T_s=800^\circ\text{C}$  with a laser fluence of (a)  $\rho=10\text{J}/\text{cm}^2$  and (b)  $20\text{J}/\text{cm}^2$ .

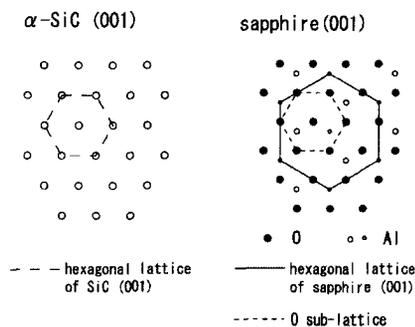


Figure 3. Schematic diagrams showing the hexagonal lattice of  $\alpha$ -SiC (001) and sapphire (001) planes.

## Fabrication and characterisation of 3C-SiC layers on 6H-SiC (0001) substrates

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Epitaxial 3C-SiC layers on 6H-SiC (0001) substrates were obtained in an ultra high vacuum MBE chamber through repeated steps of 2 mono-atomic silicon layer deposition on the (3x3) reconstruction followed by a carbonization reaction using C<sub>2</sub>H<sub>4</sub> gas. Substrates of 6H structure with (0001) facets of 1 cm<sup>2</sup> area, grown by the modified Lely method, were on-axis N-doped single crystals. The 3C-SiC layer growth was controlled in situ by LEED, XPS and XPD. The microstructure of one deposited layer was identified by transmission electron microscopy (TEM) on a thin foil specimen corresponding to a cross-section of the layer. We found that such epilayers of 16 nm thickness are epitaxial and formed by a single 3C-SiC phase. Their epitaxy with substrates corresponds to a (111) plane of the cubic structure parallel to the (0001) 6H-SiC plane at the interface and a [110] direction of 3C-SiC parallel to a [1100] direction of the hexagonal structure. However, as such an epitaxial relationship implies three orientation possibilities the 3C-SiC structure with respect to the substrate, twinned domains were formed. When examined by TEM, superimposed twinned domains oriented along <110> zone axes give rise to moiré effects, which have previously been discussed without reaching a clear understanding of their origin [1]. We show at least, how the assumption of a 9R polytype can be ruled out from a careful analysis of both high resolution images and corresponding electron diffraction.

[1] U. Kaiser, P.D. Brown, A. Chuvilin, I. Khodos, A. Fissel, W. Richter, A. Preston, C. J. Humphreys, *Materials Science Forum*, 264, 259 (1998).

## Formation of extremely thin, quasi-single-domain 3C-SiC film on on-axis Si(001) substrate using organo-silane buffer layer

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Heteroepitaxially grown 3C-SiC on Si provides one of the possible solutions to the problems of limited diameter and the micropipes of present SiC wafers. The heteroepitaxy, on the other hand, suffers formation of several kinds of defects in the grown film. Among them, anti-phase boundary (APB) is considered to be the hardest barrier to eliminate, which forms deep levels in the energy gap and acts as scattering centers for carriers<sup>1</sup>. To suppress APBs at the interface and their subsequent development in the growing film as well, miscut Si wafers have been used to facilitate anisotropic growth to develop predominant domains<sup>2</sup>. The problems with this method are the formation of defects in the grown film triggered by the surface steps on the miscut Si substrate<sup>3</sup> and the possible degradation of the device characteristics formed on the inclined film surface. To overcome this, a method has to be developed to realize the single-domain surface without using miscut surfaces. We here present a new method to grow a quasi-single-domain 3C-SiC film on on-axis Si(100). What should be emphasized is the extremely thin thickness (45 nm) of the film, which is compared to that required in a previous study ( $>5 \mu\text{m}$ )<sup>1</sup> to achieve the single-domain surface on an on-axis Si(001) substrate.

The method starts with formation of a 3C-SiC interfacial buffer layer on on-axis Si(001) substrate at  $T_s=650^\circ\text{C}$ <sup>4</sup> using monomethylsilane ( $\text{SiH}_3\text{CH}_3$ ; MMS) at  $P_{\text{MMS}}=5.0\times 10^{-5}$  Torr. Samples were resistively heated by passing a DC current along either [100] or [1-10] direction. A 3C-SiC film was then grown onto the buffer layer (Organo-silane buffer layer: OS-buffer layer) at  $T_s=900^\circ\text{C}$  using MMS at  $P_{\text{MMS}}=5.0\times 10^{-5}$  Torr.

Figure1 presents a reflection-high-energy-diffraction (RHEED) pattern from the on-axis Si(001) surface flash-annealed at  $1000^\circ\text{C}$ . The pattern, taken along the [110] azimuth, shows a  $(2\times 1)+(1\times 2)$  reconstructed surface structure with Kikuchi lines, which indicates a presence of atomically flat, double-domain surface on this starting substrate. Figure2 shows a RHEED pattern from the OS-buffer layer prepared at  $T_s=650^\circ\text{C}$ ,  $P_{\text{MMS}}=5.0\times 10^{-5}$  Torr for 5 minutes. Appearance of only 3C-SiC spots indicates the formation of a uniform, single-crystalline 3C-SiC buffer layer that fully covers the Si substrate. Cross-sectional TEM observation<sup>4</sup> indicates formation of an atomically flat SiC/Si interface without voids at this low temperature, which is ascribed to the unique adsorption nature of the MMS molecules<sup>5</sup>. When a 3C-SiC film was grown onto this buffer layer using a resistive heating along the [100] direction, the [110]-RHEED pattern presented fundamental spots as well as 1/2-order streaks, while the [1-10] pattern presented only fundamental spots. With post-annealing at  $1000^\circ\text{C}$  for 1 minute, the intensity of the 1/2-order streaks developed in the [110]-pattern (Fig. 3(a)) and a new set of 1/3-order streaks appeared in the [1-10] pattern (Fig.3(b)). There were no 1/3-order streaks in the [110] pattern and the 1/2-order streaks in the [1-10] pattern

were very weak as compared with 1/3-order streaks. These results suggest successful formation of a 3C-SiC(001) single-crystalline film with quasi-single-domain 3x2-reconstructed structure on the on-axis Si(001) substrate.

The [100] direction of the DC current used above is tilted 45° from the surface atomic steps of the Si(001) substrate, if any. To investigate the effect of the current direction on the film growth, experiments using a current along [1-10], a direction, parallel or perpendicular to the atomic steps on Si(001) surface, have been conducted. The [110]-RHEED pattern after a post-annealing at temperatures 900-1200°C, showed fundamental spots and 1/2-order streaks. This indicates that the surface reconstruction occurs in such a way that the dimer rows are perpendicular to the current direction. Applying a reverse current ([-110] direction) gave no change in the surface reconstruction, i.e., the fundamental spots and the 1/2-order streaks without the 1/3-order streaks in the [110]-RHEED pattern. These results indicate that the formation of a 3C-SiC(001) single crystal with an almost single-domain 3x2 surface structure is formed regardless of the current directions. Although the origin for the anisotropic growth and the mechanism for the reordering of the surface are not yet understood, the technological importance of the present method that realizes the formation of quasi-single-domain 3C-SiC film on on-axis Si(001) at such a thin film thickness should be obvious.

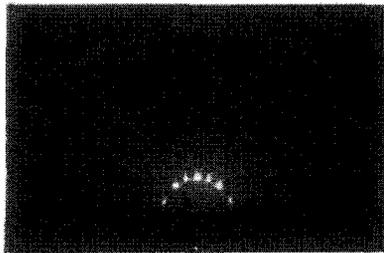


FIG.1 RHEED pattern from Si(001) (2×1)+(1×2) clean surface

(a)

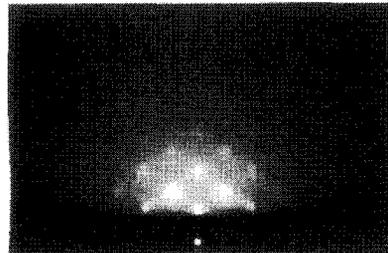
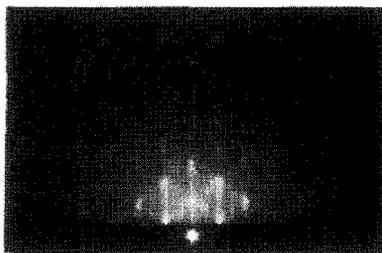


FIG.2 RHEED pattern from OS-buffer layer on Si(001)

(b)

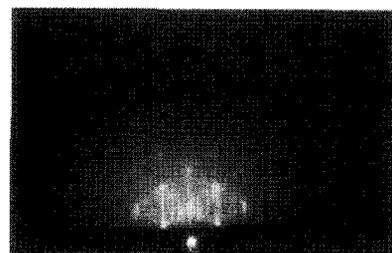


FIG.3 RHEED patterns along [110] (a) and [1-10] (b) azimuths from 3C-SiC(001) film grown on 0°-off Si(001) substrate post-annealed at above 1000°C.

#### References

- <sup>1</sup>Y. Ishida, T. Takahashi, H. Okumura, T. Sekigawa, and S. Yoshida, *Jpn. J. Appl. Phys.* **38**, 3470 (1999).
- <sup>2</sup>T. Hatayama, T. Fuyuki, and H. Matsunami, *Mat. Sci. Forum* **264-268**, 235 (1998).
- <sup>3</sup>M. Kitabatake, and J. E. Greene, *Jpn. J. Appl. Phys.* **35**, 5261 (1996).
- <sup>4</sup>H. Nakazawa, and M. Suemitsu, *Appl. Phys. Lett.*, to be published.
- <sup>5</sup>H. Nakazawa, and M. Suemitsu, *Appl. Surf. Sci.* **162-163**, 139 (2000).

## Comparison of the growth characteristics of SiC on Si between low pressure CVD and triode plasma CVD

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In order to investigate the effect of the supply of hydrogen radicals during the SiC growth, SiC films were grown on Si substrates by low-pressure thermal CVD (LPCVD) and triode plasma CVD using dimethylsilane (DMS). Activation energy for the epitaxial growth rate of SiC by LPCVD was estimated as about 90kcal/mol, whereas that by triode plasma CVD was about 45kcal/mol. Compared to the growth rate in the case of monomethylsilane (MMS), the activation energy was 20kcal/mol larger when LPCVD was used, reflecting the molecular composition, while that was about the same when the triode plasma CVD was used. Therefore, the rate-determining step for the SiC growth is considered to have been varied by supplying hydrogen radicals.

### 1. Introduction

Silicon carbide (SiC) is a wide band-gap semiconductor with large breakdown voltage, large saturated electron drift velocity and large thermal conductivity. Therefore, SiC has been intensively studied for the devices operating at high power, high frequency and high temperature. Among many polytypes, 3C-SiC with zincblende crystal structure can only be grown on Si substrates. Successful heteroepitaxy of 3C-SiC on Si has been achieved by atmosphere pressure chemical vapor deposition (APCVD) method at 1350°C using silanes and hydrocarbon gases after carbonization process[1]. Such a high growth temperature resulted in the generation of the residual stress (tensile) and the high-density defects such as dislocations and voids in the SiC films and in the film-substrate interface, due to large difference in thermal expansion coefficients between SiC and Si and to the high vapor pressure of Si, respectively. Therefore, lowering the growth temperature of SiC on Si is eagerly desired. Moreover, silane used for 3C-SiC growth is pyrophoric gas. Therefore, a carefully designed safety deposi-

tion system is required. Using an alternating gas supply method of SiH<sub>2</sub>Cl<sub>2</sub> and C<sub>2</sub>H<sub>2</sub> under low pressure after carbonization, the high quality 3C-SiC epitaxial films have been grown at 1000-1050°C[2]. The supply of hydrogen radicals without high-energy charged particles is also effective to the reduction of the growth temperature. In our previous study, the 3C-SiC films have been grown directly on Si substrates using MMS diluted with hydrogen by triode plasma CVD and LPCVD without carbonization process [3]. The organosilicon compounds such as MMS and DMS are considered to be promising candidates for the epitaxial growth of SiC because of their non-toxic and non-pyrophoric properties.

In this study, in order to investigate the effect of the supply of hydrogen radicals on the growth characteristics, SiC films were grown on Si substrates by LPCVD and triode plasma CVD using DMS.

### 2. Experimental

The triode plasma apparatus has a mesh grid electrode between the cathode and the

anode of a conventional diode type plasma CVD chamber, as described in a previous paper [3]. Strips cut from Si wafers ((111) just and miscut (001) 4° toward [110]) of about 8mm wide and 15mm long were used as the substrates. After evacuating growth chamber to  $10^{-4}$ Pa, the experiment was performed. Experimental conditions are the same as the case of SiC growth using MMS, i.e. H<sub>2</sub> flow rate 400 sccm, DMS gas pressure during film growth  $1.3 \times 10^{-3}$  Pa, gas feed ratio H<sub>2</sub>/DMS=1700, substrate temperature 900-1100°C, total gas pressure during the growth 133 Pa, rf power 100 W. Hydrogen plasma was generated by an rf (13.56MHz) power source.

### 3. Results and discussion

Figure 1 shows the dependence of the growth rate on the growth temperature in the both cases of LPCVD and triode plasma CVD. The growth rate by triode plasma CVD was large compared with that by LPCVD in the whole temperature range of 900 to 1100°C. Activation energy for the SiC growth by triode plasma CVD calculated from the slope in this region was about 45kcal/mol irrespective of the substrate orientation. This energy was about the same as that of 43kcal/mol in the case of triode plasma CVD using MMS. On the other hand, the activation energy for SiC growth by LPCVD was 90kcal/mol. This value was 20kcal/mol larger than that in the case of MMS, and growth rate by DMS was far smaller than that using MMS below 1000°C. This difference in the activation energy considered to be due to the difference in the molecule compositions. Supplying the high-density hydrogen radicals produced by triode plasma CVD, the activation energy became small by 45kcal/mol compared with that by LPCVD. The dissociation energy of Me-SiH<sub>3</sub> in MMS has been reported to be 85kcal/mol [4]. The activation energy for the H-desorption from the polycrystalline 3C-SiC surface has been reported to be 63 and

72kcal/mol, using temperature-programmed desorption [5]. Therefore, the high-density hydrogen radicals are considered to enhanced not only the hydrogen desorption from SiC surface but the desorption of methyl groups.

SiC films were grown even at 900°C using triode plasma CVD, while the growth was not observed in the case of LPCVD. For the SiC epitaxial growth, the growth temperature higher than 900°C is required due to the requirement of the desorption of H atoms from C-H bonds on SiC film surface [6]. From these results, the enhancement of H-desorption from SiC film surface by hydrogen radicals was confirmed.

### Reference

- [1] S. Nishino, Y. Hazuki, H. Matsunami, T. Tanaka, *J. Electrochem. Soc.*, **127** (1980) 2674.
- [2] Nagasawa, K. Yagi, *Phys. Stat Sol. (b)*, **202** (1997) 335
- [3] K. Yasui, K. Asada, T. Maeda, T. Akahane, *Appl. Surf. Sci.*, **175-176** (2001) 495.
- [4] P. S. Neudorfl and O. P. Strausz, *J. Phys. Chem.*, **82** (1978) 241.
- [5] M. D. Allendorf and D. A. Outka, *Surf. Sci.* **258** (1991) 177.
- [6] H. Nakazawa, M. Suemitsu, S. Asami, *Mater. Sci. Forum*, **338-342** (2000) 269.

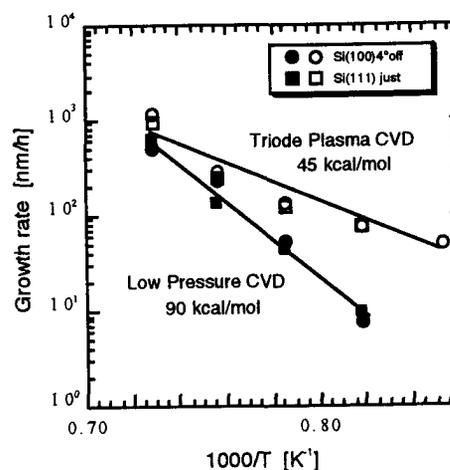


Fig. 1. Dependence of the growth rate of SiC films on the substrate temperature.

## Thin film growth of 3C-SiC on Si using CH<sub>3</sub>SiH<sub>3</sub> by LPCVD

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SiC is a potentially important material for as high speed, high efficiency, and high power semiconductor because of its wide band gap and its isotropic electron mobility. 3C-SiC has high electron mobility, high saturated electron drift velocity and thermal stability in the poly-type of SiC. Recently, the growth of 3C-SiC on Si substrate has been studied intensively. However, there are some problems, such as that the growth temperature is high, and the lattice mismatching of a SiC/Si interface produces defects in the grown crystal. Lower growth temperature is required because the impurity atoms diffuse into crystal at the high temperature.

In order to solve those problems, we have used monomethylsilane (MMS) as a source gas which has one atom each of Si and C in a molecule, this one source system can be simpler for both the equipment and the process than the two source gases system using silane and hydrocarbon. Growth of 3C-SiC on Si using MMS is reported in the low-temperature region [1,2].

In our study, thin SiC films have been successfully grown at the substrate temperature of 850 °C with a MMS cracking temperature of 1200 °C by very low-pressure chemical vapor deposition (LPCVD). The growth chamber was evacuated with turbo molecular and rotary pumps and was had a background pressure of 10<sup>-8</sup> Torr. MMS was supplied into the cold-wall vertical CVD reactor through a cracking cell. The cracking temperature was varied from 0 to 1200 °C. The flow rate of MMS controlled by a mass-flow controller was varied from 0 sccm to 2sccm. Growth of SiC on Si(100) was conducted with 2 sccm for 3 hours and MMS pressure of 1.0× 10<sup>-5</sup> Torr, where thin SiC films have been grown without an initial carbonization step on Si (100).

The grown films are analyzed using auger electron spectroscopy (AES), grazing angle X-ray diffraction (XRD) and Fourier transform infrared absorption spectroscopy (FTIR). XRD pattern indicates that the grown films on Si(100) substrate is 3C-SiC under the conditions. The depth profile of the chemical composition from the surface to interface has been investigated by AES using Ar ion etching. It turns out that the growth rate of the

film was 1.5 nm/min and the C/Si ratio was about unity. The obtained SiC films are characterized by FTIR absorption spectroscopy. The strong peaks of Si-C bonds (stretching vibration) near  $800\text{ cm}^{-1}$  and Si-H bonds (wagging vibration) near  $600\text{ cm}^{-1}$  are observed in the IR absorption spectra [3,4] as shown in Fig.1. Si-O absorption peak is considered to be backside oxide of substrate from Attenuated total reflectance method.

As a result, absorption FTIR spectra suggest that Si-C bonds are transferred from gas to film since Si-C and Si-H bond have nearly equal binding energy.

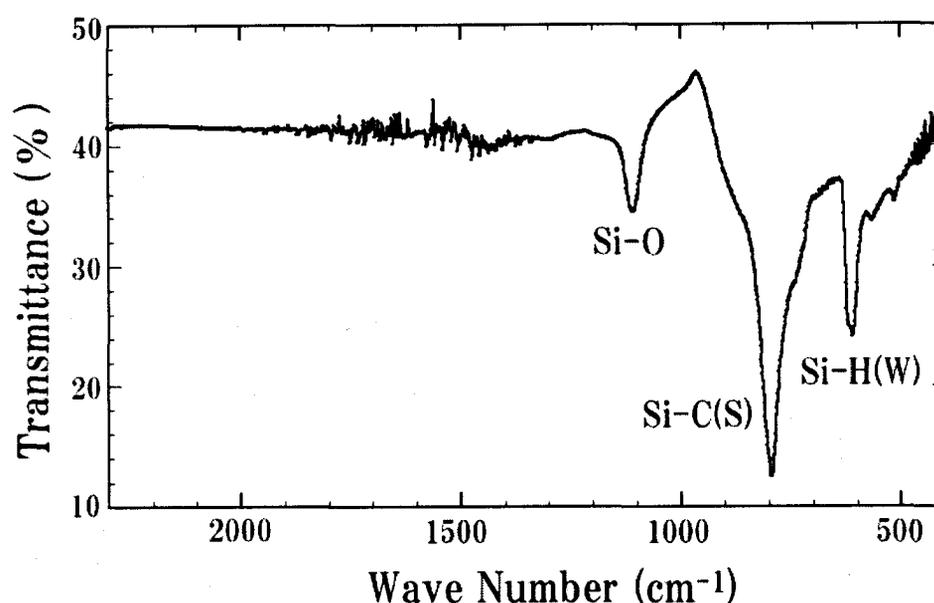


Fig.1: Absorption FTIR spectra obtained from the grown film on Si(100) at  $850\text{ }^{\circ}\text{C}$  with a cracking temperature of  $1200\text{ }^{\circ}\text{C}$ , at MMS pressure of  $1.0 \times 10^{-5}$  Torr.

[References]

1. I. Golecki, F. Redinger, and J. Marti, *Appl. Phys. Lett.* **60** (1992) 1703
2. H. Nakazawa, M. Suemitsu, S. Asami, *Thin Solid Films* **369** (2000) 269
3. Y. Sun, T. Ayabe, T. Miyasato, *Jan. J. Appl. Phys.* **38** (1999) L714
4. T. Fujii, M. Yoshimoto, T. Fuyuki, H. Matsunami, *Jan. J. Appl. Phys.* **36** (1997) 289

## The kinetic study of 3C-SiC growth on Si by pyrolyzing tetramethylsilane

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The 3C-SiC has been grown mostly on Si substrates in CVD systems using the reaction of SiH<sub>4</sub> (or Si<sub>2</sub>H<sub>6</sub>) and C<sub>3</sub>H<sub>8</sub> (or C<sub>2</sub>H<sub>4</sub>, C<sub>2</sub>H<sub>2</sub>) at high temperatures above 1300°C [1]. But it is difficult to grow high quality 3C-SiC on Si because of big mismatches in lattice constants ( $\approx 20\%$ ) and thermal expansion coefficients ( $\approx 8\%$ ) between SiC and Si. The use of a single organosilane precursors has been investigated [2-4]. The organosilane precursors contain directly bonded Si and C atoms and decompose at relatively low temperatures. Tetramethylsilane (TMS) single source have reported to grow successfully high quality 3C-SiC on Si at relatively low temperature below about 1000°C [3-5]. However, the previous works have mainly focused on the growth and characterization of 3C-SiC films. The kinetic study should be carried out to fully understand the growth process of high quality 3C-SiC film from TMS. The kinetic data are also important for the design of CVD reactor.

In this work, we investigated the growth kinetics of 3C-SiC films on Si(111) by pyrolyzing TMS. Figure 1 shows that the SiC thickness increases linearly with the growth time with the values of 12.3, 22.9, 45.1, and 84.0 nm/min for 0.5, 1.0, 2.0, and 3.0 sccm of TMS flow rates, respectively. XRD and Raman spectroscopy indicated that the grown films is 3C-SiC(111). The growth rate increased with the growth temperature. The activation energy of the SiC growth was measured from Arrhenius plot made using the rate data measured at different temperatures (Figure 2). The measured activation energies are 72.2 and 38.16 kcal/mol in the temperature ranges of 1100 - 1250°C and 1250 - 1420°C, respectively. QMS spectra of TMS showed that CH<sub>3</sub>SiH<sub>n</sub> (m/e = 42~45) and (CH<sub>3</sub>)<sub>3</sub>SiH<sub>n</sub> (m/e = 72~74) are major characteristic peaks for TMS with weak intensities of CH<sub>n</sub>, C<sub>2</sub>H<sub>n</sub>, SiH<sub>n</sub>, and (CH<sub>3</sub>)<sub>2</sub>SiH<sub>n</sub> peaks at m/e of ~15, ~26, ~30, and ~58, respectively. Figure 3 shows that with increasing the temperature, the partial pressures of hydrocarbon related species increase, while those of silicon related species decrease. On the basis of the above observation, the growth mechanism of  $\beta$ -SiC film in our growth system may be proposed in the following alternating reactions of gaseous Si atom and CH<sub>3</sub> radical. The TMS molecules are thermally decomposed to produce a gas mixture containing plenty of carbon sources and Si atoms. The CH<sub>3</sub> radical may adsorb on hydrogen treated clean Si surface as a carbon source. At high temperatures, the adsorbed CH<sub>3</sub> radical decomposes into CH<sub>x</sub> (x<3) species, or comes under the attack by another CH<sub>3</sub> · in the atmosphere of abundant CH<sub>3</sub> · to produce the adsorbed CH<sub>x</sub>(x<3) species and CH<sub>4</sub> gas, and subsequently CH<sub>x</sub> bond is broken by reacting with Si atom to liberate H<sub>2</sub> gas, leaving the formation of SiC bond. Gaseous Si atom are absorbed at hollow bridge site on C-terminated surface by surface migration or by direct arriving, forming Si terminated surface of 3C-SiC films.

### Acknowledgment

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### References

1. A.J.Steckl and J.P.Li, IEEE Trans. Electron Devices, 39, 64(1992).
2. S.Nishino, Y.Hazuki, H.Matunami, T. Tanaka, J. Electrochem. Soc., 127, 2674(1980).
3. K. Takahashi, S. Nishino and J. Saraie, J. Electrochem. Soc., 139, 3565(1992).
4. Y.H.Seo, K.S.Nahm, E.-K.Suh, Y.H.Lee, H.J.Lee, and Y.G.Hwang, J. Vac. Sci. & Tech. A, 15(4), 2226(1997).
5. Y.H.Seo, K.C.Kim, H.W.Shim, K.S.Nahm, E.K.Suh, H.J.Lee, D.K.Kim, and B.T.Lee, J. Electrochem. Soc., 145(1), 292(1998).

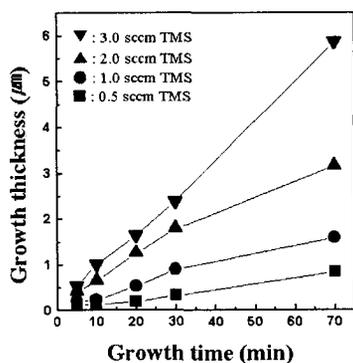


Figure 1. The thickness of 3C-SiC film as a function of growth time in terms of TMS flow rate: ( $\nabla$ ) 3.0 sccm, ( $\blacktriangle$ ) 2.0 sccm, ( $\bullet$ ) 1.0 sccm, and ( $\blacksquare$ ) 0.5 sccm TMS flow rates. The growth was carried out at 1250 °C with a H<sub>2</sub> flow rate of 1500 sccm.

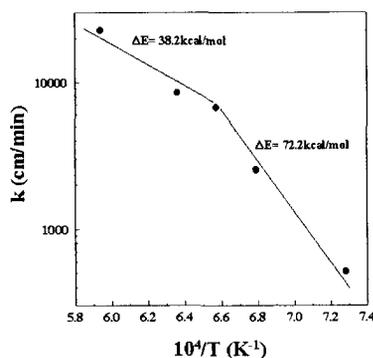
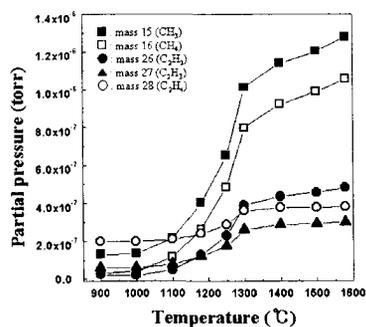
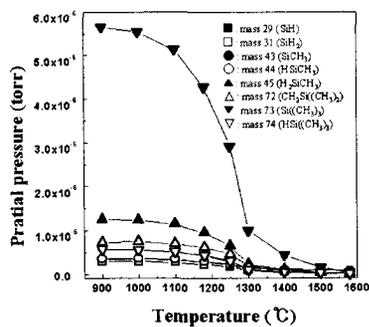


Figure 2. The Arrhenius plot of reaction rate constant,  $k$  vs.  $1/T$ .



(a)



(b)

Figure 3. The plot of partial pressures of (a) hydrocarbon related species ( $m/e=15, 16, 26, 27,$  and  $28$ ) and (b) Si related species ( $m/e=29, 31, 43, 44, 45, 72, 73,$  and  $74$ ) as a function of temperature.

## Investigation of structural defects during the 4H-SiC Schottky diodes process by synchrotron topography

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In view of its excellent thermal, mechanical and electronic properties such as wide bandgap and mobility, 4H silicon carbide (SiC) is an important semiconductor material for high temperature and high power devices. The performances of the silicon carbide devices depend of the structural quality of the substrate and its purity, but, also from the process of the device. The most important structural defects in SiC crystals are misoriented domains, inclusions, macrodefects, dislocations and micropipes [1]. At the moment, these defects were found to severely limit the quality of the SiC devices. This paper is devoted to the topographic investigation of the structural defects in the substrate and those induced by the processing of Schottky diodes on 4H silicon carbide wafer.

Schottky diodes with a surface of 0.05 to 2 mm<sup>2</sup> were made on a 35 mm 4H-SiC wafer from CREE. The substrate was 8° off-axis. A 6 μm thick epilayer was grown using CVD technique at about 1400°C with a n-type doping. Ti was deposited and patterned on the n-type layer to realize the Schottky contact. On the backside of the substrate the ohmic contact is obtained by a full sheet metallization. Structural defects were investigated by Synchrotron Topography at ESRF before any operation, after epitaxy and after metallization. Finally, some Schottky diodes were tested to do the relation between structural defects and their electrical properties. Three techniques of Synchrotron topography were used to investigate the structural defects. White beam projection topography show the defects inside the bulk of the sample. Whereas, white beam reflection topography has the advantage to show only a small thickness at the surface of the crystal. In our case this thickness is about 20 μm. It is a very useful technique to study an epilayer. The third technique, called zebra patterns technique, consists in illuminating the crystal with a monochromatic beam, E=17keV in our case. Because of the curvature of the crystal and the narrow wavelength selected by the monochromator, only a few part of the crystal diffracts. To study the entire sample, it is necessary to turn the sample on itself. A step by step rotation gives a zebra pattern, see for example Fig 1, 2 and 3. The curvature and the structural defects can be observed by this method.

Fig 1 is a zebra pattern of the substrate before epitaxy without any other operation. The rotation between two exposures was  $\Delta\omega=0.005^\circ$ . This angle and the number of the line on the image mean that the radius of the curvature is about 6 m. This topograph shows also a subgrains, indicated by an arrow on Fig. 1. The misorientation is about 30 arcsec. The complex contrast inside the circle is associated to the deformations around a micropipe.

Fig 2 and Fig 3 are zebra patterns recorded after the epitaxy and after the metallization respectively. Of course, the defects as such the micropipes and the misoriented domains remain in the crystal. A more profound analyze shows that no structural defects have been created during the process. Only the curvature radius was modified. After the epitaxy, it was about 50 m and was 11 m after the Schottky device process. The first change probably comes from an annealing phenomenon during the epitaxy. And the second one is certainly due to stress provoked by a polishing of the back face of the wafer made after the epitaxy. This polishing is necessary to obtain a good metal-semiconductor contact.

Fig 4 is a white beam reflection topograph of a part of the wafer after all the process (0001 reflections). The white spot indicated by an arrow correspond to a micropipe [2]. Smaller spots in the image are elementary screw dislocations. Because the boundary of the diodes are visible, probably due to stress introduced by the metal, we were able to locate each diode on the topography. So we made the relation between the electrical properties of the diodes and the structural defects in the wafer. We will discuss about the agreement between electrical and structural defects.



Figure 1



Figure 2

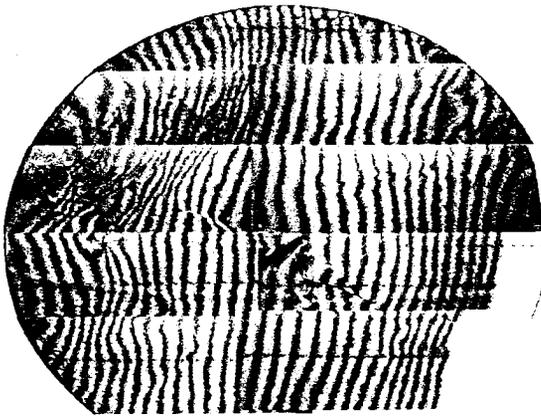


Figure 3

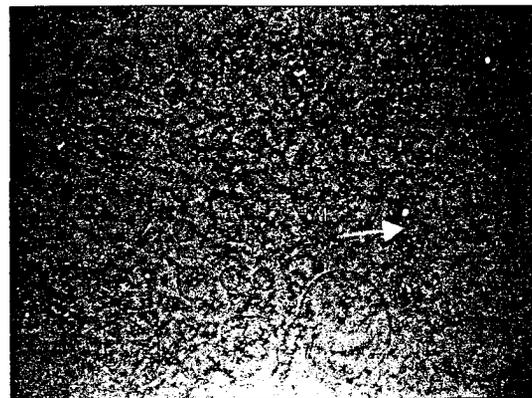


Figure 4

## References

- [1] R. Madar, M. Anikin, K. Chourou, M. Labeau, M. Pons, E. Blanquet, J.M. Dedulle, C. Bernard, S. Milita, J. Baruchel; *Diamond and Related Materials*, 6, (1997) 1249-126.
- [2] X.R. Huang, M. Dudley, W.M. Vetter, W. Huang, S. Wang, C.H. Carter; *Appl. Phys. Lett.* Vol. 74, 3, (1999) 353-355.

### Hysteresis in Transfer Characteristics in 4H-SiC Depletion /Accumulation-Mode MOSFETs

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Accumulation-mode 4H-SiC MOSFETs are being investigated to circumvent the poor inversion-layer mobility problem. In this work, we report on unusual hysteresis in transfer characteristics in n-channel depletion/accumulation-mode 4H-SiC MOSFETs. Hysteresis in transfer characteristics is observed between forward (depletion to accumulation bias) and reverse gate voltage sweeps (accumulation to depletion bias). For the reverse gate voltage sweep, the MOSFET has a positive pinch-off voltage ( $\sim 7V$ ), i.e., the depletion/accumulation-mode MOSFET is normally-off.

N-channel depletion/accumulation-mode MOSFETs have been fabricated on p-type 4H-SiC epilayers with nominal epilayer thickness and doping concentration of  $10\mu m$  and  $\sim 7 \times 10^{15} cm^{-3}$  respectively. The source/drain regions were implanted with phosphorus, and the channel region was implanted with nitrogen. The implants were annealed at  $1200^{\circ}C$  for one hour in argon. The deposited gate oxide underwent oxidation and anneals in wet and dry ambient. The channel region was implanted to a junction depth of  $\sim 0.2\mu m$  with a total dose of  $1 \times 10^{12} cm^{-2}$  in the wet oxide sample and  $3 \times 10^{12} cm^{-2}$  in the dry oxide sample.

Measurements were taken on circular geometry MOSFETs with  $(W/L)=8$  and  $L=100\mu m$ . The hysteresis observed in the transfer characteristics for the forward and reverse gate voltage sweeps is shown in Fig. 1. For large gate voltages, under accumulation, the transfer characteristics for the forward and reverse voltage sweep are the same. No hysteresis was observed in the transfer characteristics on inversion-mode MOSFETs fabricated on the same chip, indicating that mobile ion contamination is not the cause of the hysteresis.

Fig. 2 shows the transfer characteristics for forward voltage sweep with different starting gate voltage. As the starting gate voltage becomes more negative, the  $I_D-V_G$  curves shift to the left and the channel pinch-off voltage is more negative. The channel cannot be pinched off for reverse voltage sweep with  $V_G=-30V$  to  $70V$ . Similar shift in the  $I_D-V_G$  curves was also observed for reverse voltage sweeps with different starting gate voltages. For less positive starting gate voltages, the  $I_D-V_G$  curves shifted to the left (Fig. 3). For both the forward and reverse voltage sweep, the end voltage did not have any effect on the  $I_D-V_G$  characteristics. Fig. 4 compares the hysteresis observed between forward and reverse voltage sweeps at  $25^{\circ}C$  and  $100^{\circ}C$ . The pinch-off voltage is more negative at higher temperatures due to an increase in the channel doping concentration due to increasing ionization. Table 1 compares the pinch-off voltage at different temperatures; the hysteresis decreases at higher temperatures. Similar results were also obtained on depletion/accumulation-mode MOSFETs on the dry oxide sample.

The hysteresis and the shift in transfer characteristics are attributed to changes in the effective oxide charge because of changes in interface state occupancy. The interface state occupancy changes depending on the magnitude of the starting gate voltage and the direction of gate voltage sweep resulting in hysteresis in the transfer characteristics.

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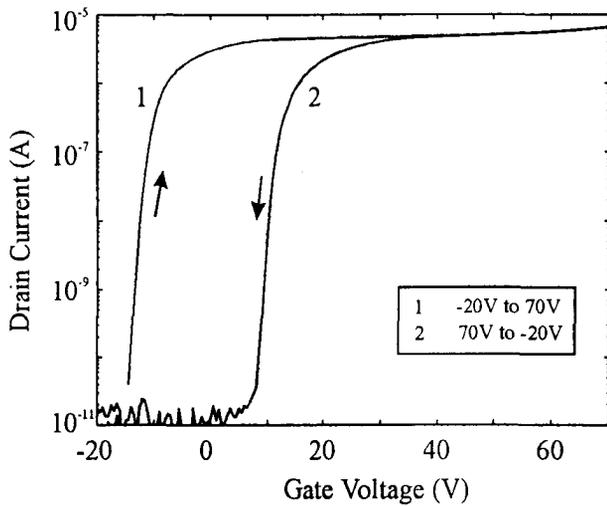


Fig. 1: Hysteresis in transfer characteristics for forward and reverse gate voltage sweeps.

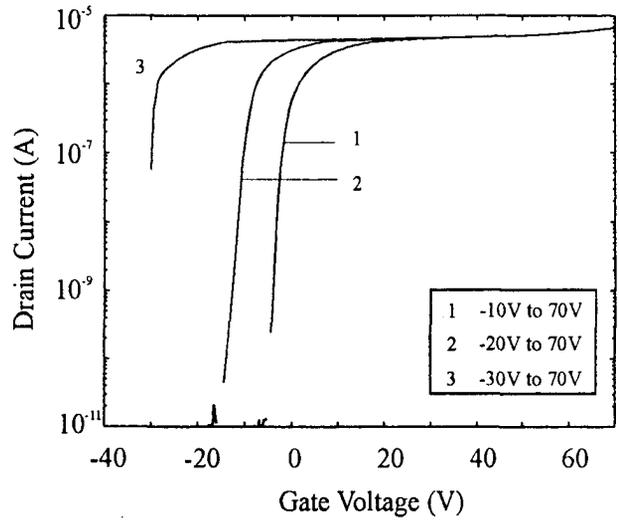


Fig. 2: Shift in transfer characteristics for different starting gate voltages in forward gate voltage sweep.

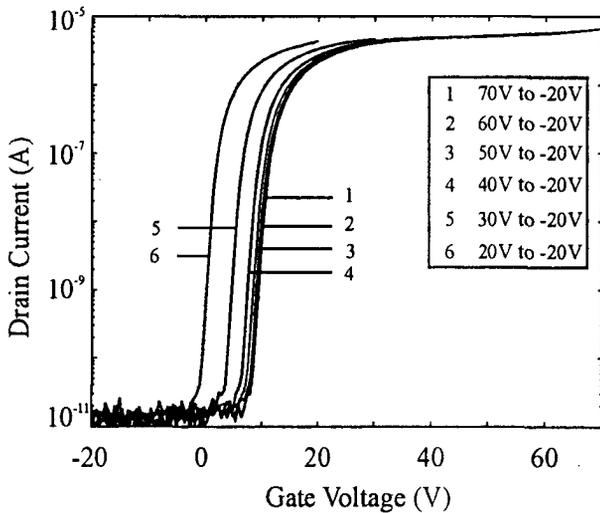


Fig. 3: Shift in transfer characteristics for different starting gate voltages in reverse gate voltage sweep.

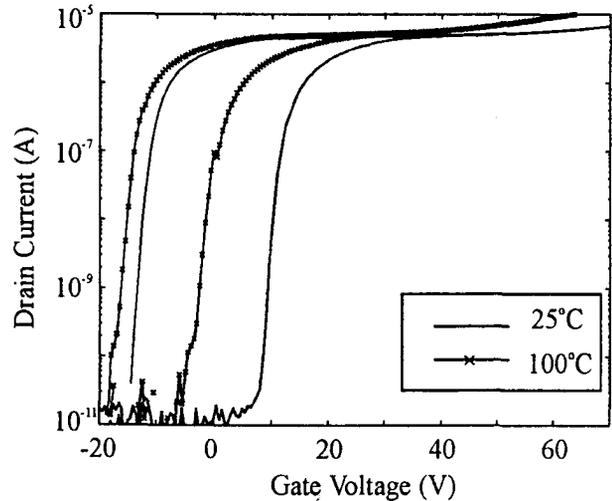


Fig. 4: Comparison of hysteresis in transfer characteristics at 25°C and 100°C.

Table 1: Comparison of pinch-off voltage between forward and reverse gate voltage sweep at different temperatures.

Temperature (°C)	$V_{P,F}$ (Forward Sweep)	$V_{P,R}$ (Reverse Sweep)	$\Delta V_P = V_{P,R} - V_{P,F}$
25	-14.5	7.0	21.5
50	-17.5	1.5	19.0
75	-18.5	-3.0	15.5
100	-17.0	-6.5	10.5
125	-17.5	-9.5	8.0
150	-18.5	-11	7.5

## Depth Distribution of Lattice Damage related $D_I$ and $D_{II}$ Defects after Ion Implantation in 6H-SiC

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Lattice damage related defects responsible for the famous  $D_I$  and  $D_{II}$  optical emission were previously attributed to a silicon di-vacancy and a carbon di-interstitial respectively.<sup>1,2,3</sup> However, no clear understanding of the mechanism for their formation during implant anneal is available yet. In addition, no experimental data was reported on the depth distribution of the  $D_I$  and the  $D_{II}$  centers, which could help to better understand the mechanism for the defect formation as well as could be important from the point of view of SiC devices performance.

In this letter, the depth distribution of the  $D_I$  and the  $D_{II}$  defects that were formed by high temperature annealing of nitrogen implanted samples was investigated by etching the samples to different depths. The etching removed consequently increasing portion of the near-surface layer in which the corresponding defects resided, which allowed to use PL to probe consequently deeper in the bulk of the epilayer. The PL spectra of a sample before and after the top 0.45 microns of the material were removed by reactive ion etching are shown in Fig. 1. The intensities of the  $D_I$  lines  $L_1$ ,  $L_2$ , and  $L_3$  are still strong after the etching - as much as about 60% of what was measured from the sample before etching. This indicates that the corresponding defects penetrate well beyond 0.45  $\mu\text{m}$  in the depth of the material during the defects formation. On the other hand, the  $D_{II}$  photoluminescence has completely disappeared after the etching. In order to obtain a more quantitative picture of the depth distribution of the  $D_I$  and the  $D_{II}$  defects, a group of samples was subjected to a series of RIE etches followed by PL measurements. Intensities of the  $D_I$  and the  $D_{II}$  photoluminescence normalized to their initial values before etching are plotted versus the etch depth in Fig. 2. The  $D_I$  PL did not disappear till significantly beyond the end of the ion penetration range (vertical dashed line in Fig. 2). The  $D_{II}$  PL disappeared with depth much earlier than the  $D_I$ .

The observed localization of the  $D_{II}$  PL in the region that does not extend beyond the ion penetration range indicates that there is neither a significant diffusion of the  $D_{II}$  defects themselves nor a significant diffusion of initial intrinsic defects that combine together to form the  $D_{II}$  center. More systematic "profiling" shown in Fig. 2 confirms this statement. Contrary, the  $D_I$  PL emission was still observed significantly beyond the end of the ion penetration range. This means that the distribution of the  $D_I$  centers is determined not only by the penetration depth of initial defects after the implantation but also by a higher diffusivity of the initial defects that combine together to form the  $D_I$  center during the annealing. The described difference in the distribution of the  $D_I$  and the  $D_{II}$  defects after the implant annealing in 6H-SiC will be discussed in a possible connection with the mobility of the original lattice damage defects as well as with the efficiency of their pairing to form the  $D_I$  and the  $D_{II}$  complexes.<sup>4,5,6</sup> Additional experiments are conducted to verify also a possible role of the different implanted species and their tendency to occupy different lattice sites during implant annealing. The pattern of the depth distribution of the

$D_I$  and the  $D_{II}$  centers should be taken into account in studying the influence of lattice damage defects on the performance of SiC devices.

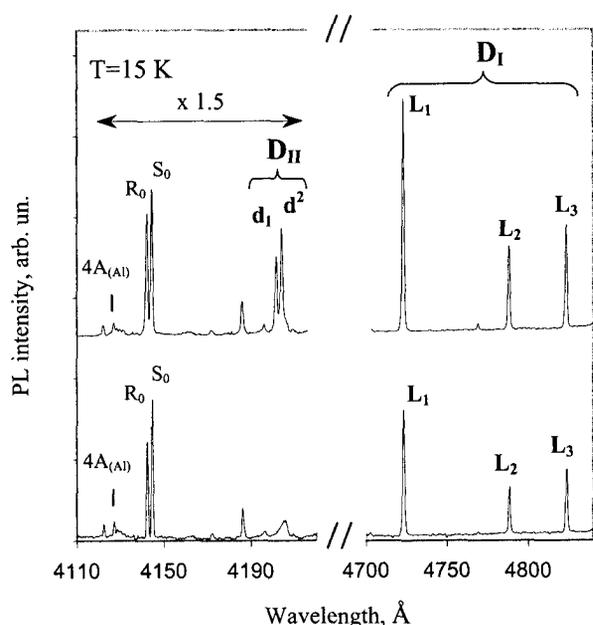


Fig. 2 PL spectra of a nitrogen implanted and annealed sample before (top) and after (bottom) 0.45  $\mu\text{m}$  etch. At this depth, intensities of  $D_I$  lines are still very strong, while  $D_{II}$  PL is completely disappeared.

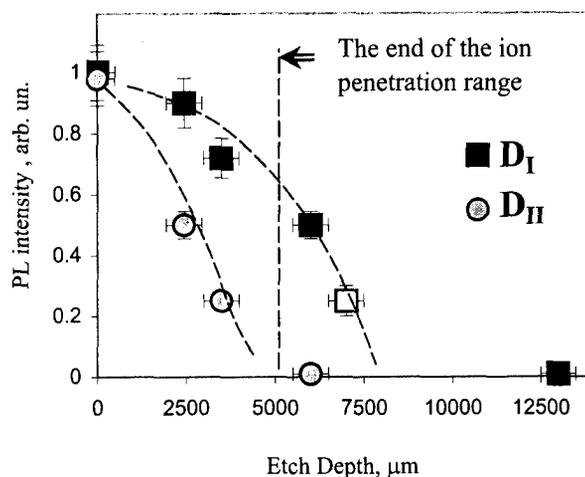


Fig. 2 Normalized PL intensity of  $D_I(L_1)$  and  $D_{II}(d_1)$  defect lines measured after a few consecutive etches of the surface of a SiC sample.  $D_I$  PL could still be observed even after the sample was etched beyond the end of the ion penetration range. The empty square was measured on a different sample.

<sup>1</sup> L. Patrick and W.J. Choyke, Phys. Rev. B **5**, 3253 (1972)

<sup>2</sup> S.G. Sridhara, D.G. Nizhner, R.P. Devaty, V.J. Choyke, T. Dalibor, G. Pensl and t. Kimoto, Mater. Sci. Forum, **264-268** (1998), 493

<sup>3</sup> H. Itoh, T. Troffer, C. Peppermuller, and G. Pensl, Appl. Phys. Lett. **73**, (1998) 1427

<sup>4</sup> J.W. Steeds, F. Carosella, G.A. Evans, M.M. Ismail, L.R. Danks and W. Voegeli, Mater. Sci. Forum **353-356** (2001), 381

<sup>5</sup> J.W. Steeds et al, Diamond and Relat. Mat. **8** (1999), 94

<sup>6</sup> T. Ohshima, A. Uedono, H. Itoh, K. Abe, R. Suzuki, T. Ohdaira, Y. Aoki, M. Yoshikawa, T. Mikado, H. Okumura, S. Yoshida, S. Tanigawa and I. Nahiyama, Mater. Sci. Forum, **264-268** (1998), 745

## Influence of Junction Potential Distribution on Effective Impurity Ionization Time Constants in SiC for Admittance Spectroscopy Data Analysis

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Thermal admittance spectroscopy is a useful tool which allows one to obtain important information, such as activation energy and capture cross-section, about impurity levels in semiconductors [1-7]. Admittance spectroscopy was extensively used to find the activation energies of technologically important SiC impurities [4-7]. The technique is based on a strong dependence of the semiconductor junction differential admittance on the temperature and measurement ac signal frequency in the case of a semiconductor with an incompletely ionized impurity. The real part of the junction admittance, the conductance, exhibits a peak in its temperature dependence when the impurity ionization time constant is comparable with the ac measurement signal period. The imaginary part of the admittance, the capacitance, has an inflection point in the same temperature range.

In most variants of the admittance spectroscopy technique the natural logarithm of the measurement frequency is plotted versus the corresponding conductance peak positions on a  $1/T$  scale. The resulting Arrhenius plot is then approximated by a straight line whose slope is proportional to the impurity activation energy and intercept determines the capture cross-section. Linearity of the Arrhenius plot follows from a rather simplified assumption of proportionality of the measurement signal frequency and the average impurity emission coefficient, for which the conductance has a peak, with the proportionality coefficient being either equal to 1 [Ref. 1] or equal to 2 [Ref. 2]. In a recent paper [8] we showed that this proportionality coefficient depends on the impurity ionization probability in the semiconductor bulk and on the junction potential distribution. These factors lead to the nonlinearity of the Arrhenius plot. The impurity ionization probability depends on temperature and impurity atom concentration, while the potential distribution additionally depends on the measurement signal parameters. In the Ref. [8] we derive an equation which describes the influence of the impurity occupation in the semiconductor bulk on the effective impurity time constant. In the present work we investigate the influence of the junction potential distribution on the effective impurity time constant. Using our general model of the junction admittance [9] we show that the proportionality coefficient between the impurity ionization time constant and the emission coefficient is a strong function of the potential distribution, which is important to take into account in the Arrhenius plot analysis.

Junction admittance is proportional to the space charge region charge change in response to a bias change. The proportionality coefficient, or the susceptibility function, is a complex quantity, which reflects the delayed response of the impurity ionization processes to bias changes. Obviously, this delay causes the junction potential to be complex as well. Junction conductance is proportional to the imaginary part of the integral over the space charge region of the product of the potential and the susceptibility function. Traditional analysis takes into account only the real part of the junction potential. However, calculations show that the product of the imaginary part of the potential and the real part of the susceptibility function may be comparable to the product of the real part of the potential and imaginary part of the susceptibility function;

these two products have opposite signs. Since conductance is determined by the sum of these products, it may differ greatly from the value of conductance predicted by the traditional analysis. This statement is illustrated by Figure 1. On this figure, integrals of the cross-products of the real and imaginary parts of the potential and susceptibility function and their sum are plotted versus temperature for N-doped 6H-SiC (the activation energy is taken equal to 0.14 eV, which corresponds to two k-sites).

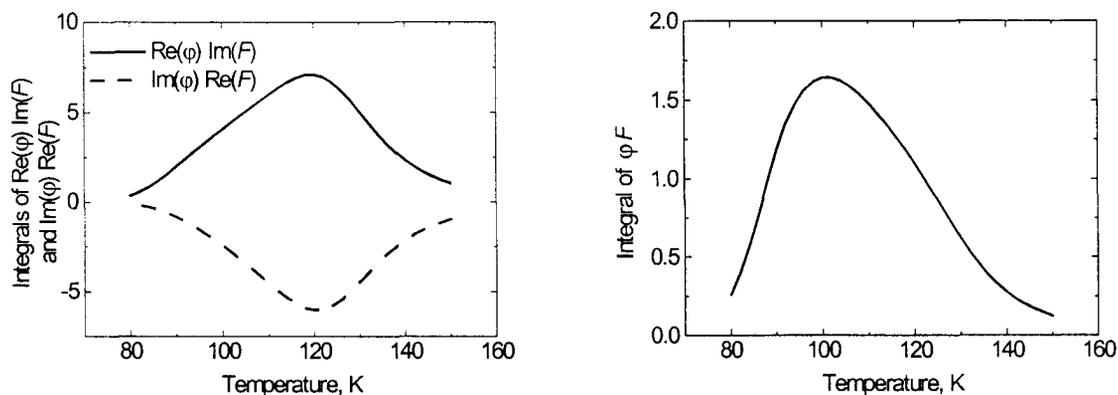


Figure 1. Components of the product of the junction potential  $\phi$  and the susceptibility function  $F$  in N-doped 6H-SiC.  $E_A=0.14$  eV,  $N=10^{16}$  cm<sup>-3</sup>,  $\sigma=2.7\times 10^{-16}$  cm<sup>-2</sup>,  $\omega=4\pi\times 10^4$  Hz.

The product of the real part of the potential and the imaginary part of the susceptibility function has a maximum at about 120 K. At this temperature, in accordance with the traditional theory, the impurity emission rate is approximately equal to half the measurement frequency. However, the other product also has an extremum at about the same temperature, and the sum of the two is maximal at a significantly lower temperature of 101 K, where the emission rate is 18 times smaller than at 120 K. Thus, neglecting to take into account the potential distribution in Arrhenius plot analysis produces erroneous values of impurity activation energy and capture cross-section.

We report on a detailed analysis of the impurity time constant behavior in SiC as a function of impurity parameters (activation energy and concentration) and experimental conditions (temperature, bias frequency and amplitude).

- [1] D. L. Losee, J. Appl. Phys., **46**, 2204 (1975).
- [2] G. Vincent, D. Bois, and P. Pinard, J. Appl. Phys., **46**, 5173 (1975).
- [3] J. L. Pautrat, B. Katircioglu, N. Magnea, D. Bensahel, J. C. Pfister and L. Revoil, Solid-State Electron. **23**, 1159 (1980).
- [4] A. O. Evwaraye, S. R. Smith, W. C. Mitchel, and H. McD. Hobgood, Appl. Phys. Lett., **71**, 1186 (1997).
- [5] A. O. Evwaraye, S. R. Smith, and W. C. Mitchel, J. Appl. Phys., **75**, 3472 (1994).
- [6] S. R. Smith, A. O. Evwaraye, W. C. Mitchel, and M. A. Capano, J. Electron. Mater., **28**, 190 (1999).
- [7] C. Raynaud, F. Ducroquet, P. N. Brounkov, G. Guillot, L. M. Porter, R. F. Davis, C. Jaussaud, and T. Billon, Materials Science and Technology **12**, 94 (1996).
- [8] Andrei V. Los, Michael S. Mazzola, J. Appl. Phys. **89**, 3999 (2001).
- [9] A. V. Los, M. S. Mazzola, S. E. Saddow, Materials Science Forum **338-342**, 745 (2000).

## Radiation Induced Defects in p-type Silicon Carbide

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### Introduction

Single crystalline silicon carbide (SiC) is expected to be an excellent material for making high power electronic devices used under severe environment such as intense ionizing radiation field with high temperature. There is considerable interest in the mechanism of radiation damage in electronic semiconductor devices, which can be operated under intense ionizing radiation field. Therefore it is necessary to understand the characteristics of the radiation damage and annealing properties of the defects. However, only a little has been known about radiation induced defects in p-type SiC. In this study, we have performed electron spin resonance (ESR) measurements of p-type 4H and 6H-SiC irradiated with reactor neutrons or high-energy electrons.

### Experimental

The samples used in this study were obtained from Cree Research Incorporation. The carrier density of Al-doped p-type 4H and 6H-SiC used in the present experiment was the order of  $10^{18}/\text{cm}^3$ . The irradiations were performed at the low-temperature irradiation loop facility (LTL) of the Kyoto University Research Reactor Institute (KUR) and the electron linac (LINAC) of the KUR. At the LTL, SiC samples were irradiated with the fast neutron fluence of  $6 \times 10^{16} \text{n}/\text{cm}^2$ . The LINAC was operated under the following conditions: accelerating voltage; 22 or 30 MeV, pulse width;  $3 \mu\text{s}$ , repetition; 30pps, and peak current; 500mA (average current about  $40 \mu\text{A}$ ). The neutron fluence was monitored by the activation method with Ni foils. Isochronal annealing was performed in the temperature range between  $100^\circ\text{C}$  and  $1500^\circ\text{C}$  for 5 minutes in helium atmosphere. Electron spin resonance (ESR) spectra were measured at room temperature (RT) and liquid nitrogen temperature (LNT) with an X-band (9GHz) microwave incident on a  $\text{TE}_{110}$  cylindrical cavity using the JEOL JES-TE200.

### Results and discussion

Figure 1 shows ESR spectra at (a) RT and (b) LNT for electron(22MeV)-irradiated p-type 4H-SiC with  $10^{18} \text{n}/\text{cm}^2$ . The ESR signals termed K1(Vsi), K12, K11(Vc), K1(Vsi) + K13 and K14 are observed. The K1 and K11 signals are similar to those for silicon vacancies and carbon vacancies found in electron-irradiated 3C-SiC(T1 center)<sup>1</sup>, 6H-SiC(PA center)<sup>2</sup> and 3C-SiC(T5 center)<sup>3</sup>, 6H-SiC(PB center)<sup>4</sup>, respectively. The K12 center observed at the room temperature appears at low dose irradiation. The K1(Vsi) + K13 center, which are overlapped each other, observed at LNT appears remarkably at low dose. Moreover, the K14 center observed at LNT is a radiation-induced defect, which was produced in the early stage of the irradiation. These defects change when the irradiation advances, and then these centers decrease. The K1(Vsi) becomes predominant when it is irradiated with electron(22MeV) fluence up to  $3 \times 10^{18} \text{n}/\text{cm}^2$ . In this case, the behavior of the K1, K2, K3, and K4 centers is similar with that observed on the n-type SiC on which we have reported previously<sup>5</sup>. Finally, K11(Vc) center is not observed with the high dose irradiation. Figure 2 shows the fluence-dependence of the K1(Vsi) and K11(Vc) centers. As

shown in this figure, the carbon vacancies decrease though the silicon vacancies increase with the irradiation. It is necessary to consider about the influence on the defect generation by electronic excitation under the irradiation.

Isochronal annealing behavior of the K1(Vsi), K12, K11(Vc), K1(Vsi) + K13 and K14 signals is shown in Fig.3. An almost part of the K1(Vsi) center disappears at 700°C and the K11(Vc) center at 300°C. An almost part of the K12 center disappears rapidly at about 400°C. After the K1(Vsi) center disappeared, the K1(Vsi) + K13 center disappears at about 1,200°C following it reached to its maximum at about 900°C. The K14 center disappears at about 1,200°C after reached to the maximum intensity at around 900°C.

From these facts, these defect centers are thought to be due to compound defects, which relate with the silicon vacancy.

- References**
- 1) H.Itoh et al., J. Appl. Phys. **66**, 4529 (1989).
  - 2) A. Kawasuso et al., Mater. Sci. Forum Vols. **264-268**, 611 (1998).
  - 3) H. Itoh et al., J. Electro. Mater. **21**, 707 (1992).
  - 4) D. Cha et al., Mater. Sci. Forum Vols. **264-268**, 615 (1998).
  - 5) S. Kanazawa et al., Mater. Sci. Forum Vols. **338-342**, 825 (2000).

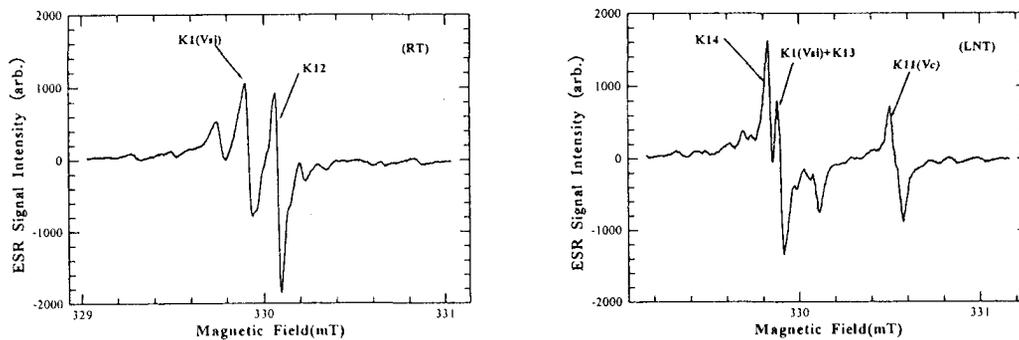


Fig. 1 ESR spectra observed at (a) RT and (b) LNT for 22MeV electron-irradiated p-type 4H-SiC.

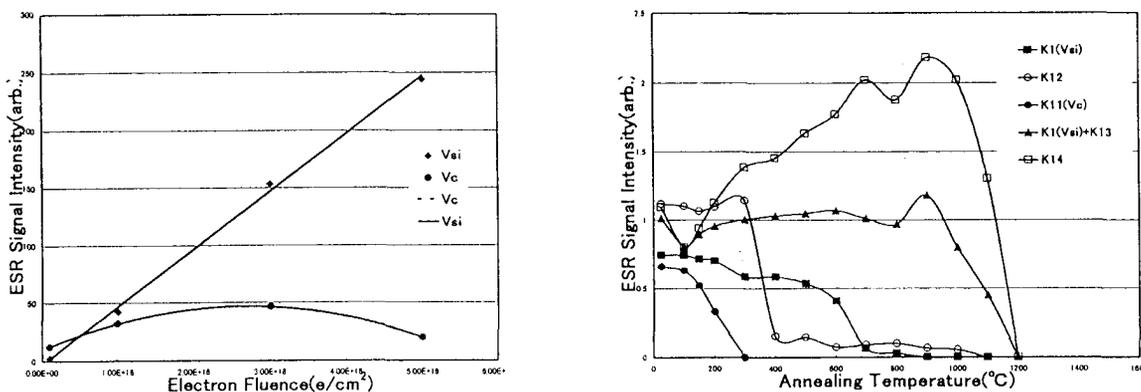


Fig. 2 The ESR signal intensities of K1(Vsi) and K11(Vc) centers in p-type 4H-SiC irradiated with 22MeV electrons as a function of the fluence.

Fig. 3 Isochronal annealing behavior of the ESR centers introduced in p-type 4H-SiC by 22MeV electron irradiation.

## Electrical Properties in Neutron-Irradiated Silicon Carbide

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**Introduction:** Silicon carbide (SiC) single crystal is expected as high power electronic devices used under severe environment such as intense ionizing radiation field with high temperature. However, the mechanism of radiation damage in electronic semiconductor devices, which can be operated under intense ionizing radiation field, has not been understood yet. Therefore, it is necessary to understand the characteristics of the radiation damage and annealing properties of the defects. In the present paper, we describe for electrical characteristics of n-type SiC irradiated with reactor neutrons.

**Experimental arrangement:** The SiC single crystal used in this study were manufactured by Nippon Steel Corporation. These SiC wafers were nitrogen-doped and the carrier densities were the order of  $10^{18}/\text{cm}^3$  and  $10^{19}/\text{cm}^3$ . Ohmic contacts were made on each n-type SiC wafer by evaporating Ni dots followed by annealing at 1,100°C for 30 minutes in Ar atmosphere.

The neutron irradiations were carried out using the low-temperature irradiation loop facility of Kyoto University Reactor(KUR-LTL). The irradiation in the LTL was carried out with the fast neutron fluence of  $6 \times 10^{17} \text{ n/cm}^2$  at 50K and 100K. The neutron fluence was monitored by the activation method using Ni foils.

The measurements of resistivity and Hall effect on n-type SiC were carried out at RT by the Van der Pauw method. Isochronal annealing of the irradiated samples was performed in the temperature range between 373K and 823K for 5 minutes in Ar atmosphere.

**Results and discussion:** It is well known that the electrical resistivity increases with fast neutron fluence. Though various factors are relative about how to increase the electrical resistivity, an initial carrier density of SiC would be favorable candidate.

Figure 1 shows the changes of electrical properties after the neutron irradiation as a function of the initial carrier density in n-type SiC. In this figure, the change rate of mobility becomes large with increasing of the initial carrier density, while that of the electrical resistivity small. On the other hand, the change rate of the carrier density is almost fixed.

Figure 2 shows the relation between the carrier density and mobility before and after the irradiation of the neutron. After neutron irradiation, the carrier mobility increases with the carrier

density, though the mobility has decrease according to increase the carrier density before the neutron irradiation. This is thought as follows; the donor decreases by the irradiation and consequently the ion scattering decreases. In any case, these results show that it is necessary to consider scattering with impurities.

The results of the isochronal annealing experiment are shown in Fig.3. The results indicated that the resistivity and the mobility were annealed at two recovery stages (350K, 500K) and that the carrier density did not change by the isochronal annealing up to 823K. The resistivity was recovered about 40% due to 823K annealing. These results contradict from the following experimental expectation; i.e. usually the carrier density recovers by a thermal annealing.

From these facts, these experimental results can be concluded to influence by the existence of a large amount of donor.

This work has been carried out in part under the Visiting Researcher's Program of the Research Reactor Institute, Kyoto University.

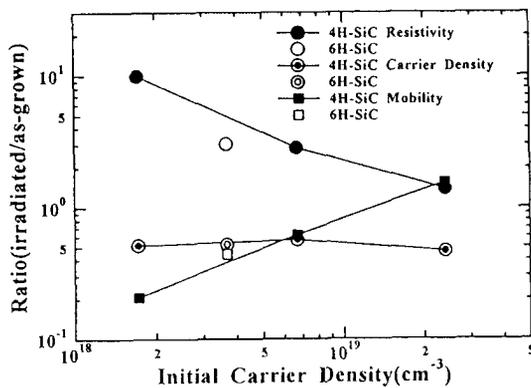


Fig.1 Changes in electric properties after neutron irradiation as a function of initial carrier density.

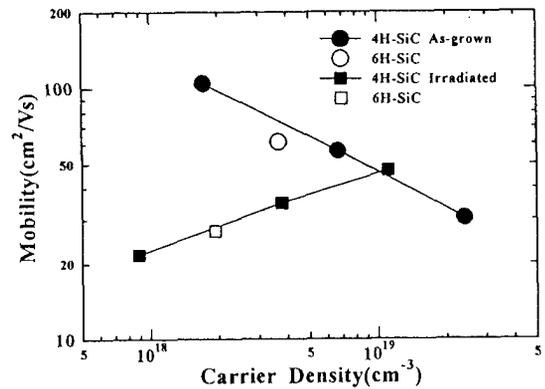


Fig.2 Carrier mobility as a function of carrier density.

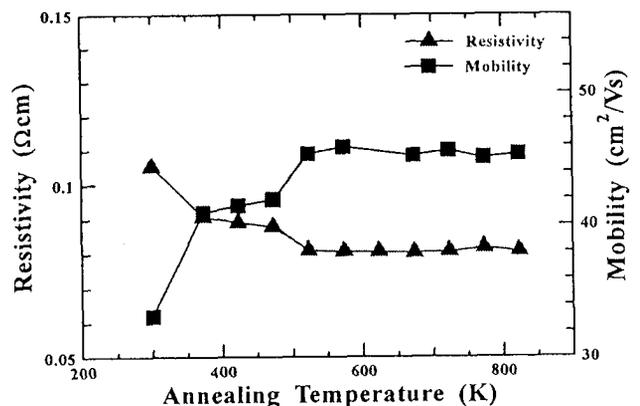
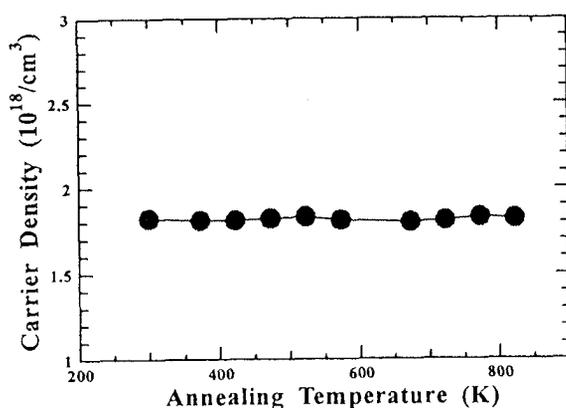


Fig.3 Isochronal annealing results of neutron-irradiated SiC.

## SIMS analyses of SiO<sub>2</sub>/SiC interface

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Establishment of reproducible and reliable control of SiO<sub>2</sub>/SiC interface was main issue for application of SiC to a power MOSFET. The detailed discussions of the SiO<sub>2</sub>/SiC interface are expected to open a new approach to make an applicable gate insulator for an SiC power MOSFET. In this paper, Secondary ion mass spectrometry (SIMS) analyses was undertaken to investigate the SiO<sub>2</sub>/SiC interface.

4H-SiC(0001) off-cut wafer 3.5° toward <1120> was used as the substrate for epitaxial growth of 4H-SiC(0001) films. N-type epitaxial film with nitrogen dopant was grown using the vertical hot-wall-type chemical vapor deposition (CVD) system.[1] The surface of the epitaxial film was cleaned by the sacrificial oxidation procedure prior to the formation of SiO<sub>2</sub> insulator film. Then the SiO<sub>2</sub> insulator film on the surface of the cleaned epitaxial film was formed by thermal oxidation with or without post-oxidation annealing(POA). Detailed SIMS analyses were undertaken upon three different samples of SiO<sub>2</sub> insulator layers formed by (a)3-hours wet oxidation at 1100°C, (b)3-hours wet oxidation at 1100°C followed by 3-hours POA at 900°C and (c) 40-minutes wet oxidation at 1190°C. Depth profiles of carbon were measured using SIMS. Carbon composition was normalized as those in SiC fit to 100% in the following SIMS analyses. Background of carbon in these SIMS measurements was less than 0.5%. The SiO<sub>2</sub>/SiC interface transition region, where carbon composition increased from 16% to the main component of SiC (84%), was observed as thin as 4.0 ~ 5.4 nm in our SIMS measurements including the apparatus limit of the depth resolution.

SIMS profile of the sample (a) shows the largest SiO<sub>2</sub>/SiC interface transition thickness of 5.4 nm. The SiO<sub>2</sub>/SiC interface of sample (a) includes carbon rich transition layer whose carbon concentration is 10% larger than the other two samples. Uniform carbon concentration of 2% is observed although the SiO<sub>2</sub> film of sample(c). While the carbon concentration at the SiO<sub>2</sub> surface of sample(b) is in background range, the closer the carbon concentration in the SiO<sub>2</sub> film gets to the SiO<sub>2</sub>/SiC interface, the larger it becomes up to 1%.

Oxidization forming SiO<sub>2</sub> film on SiC leaves residual carbon flux at the SiO<sub>2</sub>/SiC interface. The POA procedure accelerates diffusion of the residual carbon from the SiO<sub>2</sub>/SiC interface to the surface through the SiO<sub>2</sub> film. High temperature oxidation can diffuse the residual carbon at the SiO<sub>2</sub>/SiC interface during oxidation while a few % carbon concentration remains in the SiO<sub>2</sub> film.

**Reference:** [1]K. Takahashi, *et. al.*, Mater. Sci. Forum, 338-342 (2000) 726.

## Electroluminescence Analysis of Al<sup>+</sup> and B<sup>+</sup> Implanted pn-Diodes

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**Abstract:** Since pn junction is used in pn diode, edge termination in SBDs or channel formation in FETs, the reduction of leakage current in pn junction is one of the key issue to realize SiC devices. We have fabricated 4H-SiC pn diodes by Al<sup>+</sup> or B<sup>+</sup> implantation into n-type epitaxial layers. The electroluminescence(EL) is effective to obtain information of transition between donors, acceptors and defects[1][2]. We have measured EL spectra for these pn diodes with high leakage currents and those with low leakage currents. Diodes with low leakage current showed steep increase with current injection in 390nm peak compared to that from donor acceptor pair (DAP) recombination, whereas the diode with high leakage current showed a relatively slow increase in 390nm peak. We speculate that recombination through DAP or defects is the reason of high leakage current and small band-edge EL peak.

### Experiments:

4H SiC wafers were used in this work. Low doped n-type epitaxial layers were grown by hot wall LPCVD[3]. SiO<sub>2</sub> layer was formed by oxidation. Al<sup>+</sup> or B<sup>+</sup> was implanted to form p-type layer in n-type epitaxial layer, followed by high temperature activation annealing. Ni was sputtered for backside ohmic contact, followed by annealing. Contact holes were opened in SiO<sub>2</sub> layer. Al and Ti layers were sputtered subsequently, followed by annealing at 900°C to obtain ohmic contact to p-type layer. Current-Voltage characteristics were measured by HP4142B. EL spectra were measured at room temperature by Multi Channel Photo Detector (MCPD-1000).

Fig. 1 shows EL spectra of Al doped pn diodes with (a) low leakage current and those with (b) high leakage current. At lower voltages 480nm peak was dominant, and by increasing bias voltage a rapid increase in 390nm peak was observed in EL spectra for Al doped diodes. Diodes with low leakage current showed steep increase in 390nm peak, whereas the diode with high leakage current showed a relatively slow increase in 390nm peak.

EL spectra of B doped pn diodes with (a) low leakage current and those with (b)

high leakage current are shown in Fig. 2. Two peaks around 530nm peak and 780nm were observed for B doped diodes at low injection current. By increasing the current injection 390nm peak appeared. Diodes with low leakage current showed steep increase in 390nm peak compared to those with high leakage current, which showed a relatively slow increase in 390nm peak and and higher 780nm peak than 530 nm peak.

Peak around 400nm is attributed to free to bound transitions[2]. The peak around 480nm is assigned to DAP recombination involving the nitrogen donor and a deep acceptor level[3]. The peak around 500nm is attributed to DAP from the nitrogen donor and the deeper boron acceptor[3]. And peak at 514nm is attributed to optical transitions of conduction electrons to neutral deep B acceptor.[2] We speculate that the red peak correlates with the origin of high leakage current.

### References

- [1] A. Galeckas, et. al., Mat. Sci. Forum, Vols. 338-342(2000) pp.683
- [2] F. H. C. Carlsson, et. al., Mat. Sci. Forum, Vols. 338-342(2000) pp.687
- [3] H. Tsuchida, et. al., 1<sup>st</sup> Int. Workshop on Ultra-Low-Loss Power Device Technology, (2000), p37

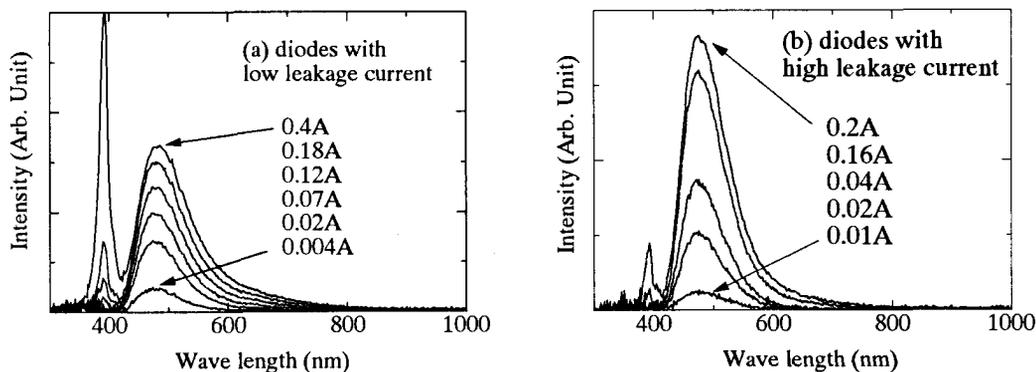


Fig. 1, EL spectra of Al doped pn diodes

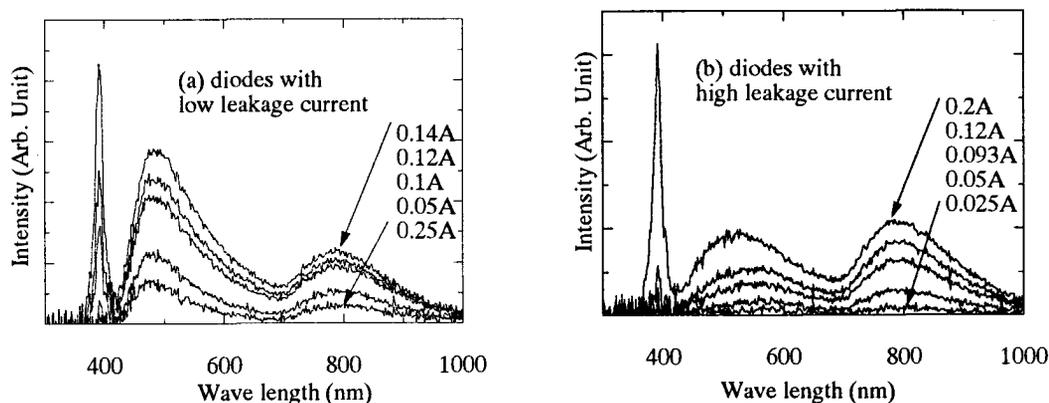


Fig. 2, EL spectra of B doped pn diodes

## ON THE LOCATION OF ER ATOMS IN IMPLANTATION DAMAGED SiC BEFORE AND AFTER ANNEALING

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Ion implantation for doping of SiC has attracted increasing attention and it is known that annealing is necessary both to remove the implantation damage and to electrically activate the dopants [1]. Ion-implantation as a method for nanostructure fabrication within SiC [2] has the advantage over other methods that nanocrystals can be created in a well-defined matrix. In the latter case the dose has to be about three orders of magnitude higher (about  $10^{17} \text{cm}^{-2}$ ) and therefore the process is accompanied by excessive matrix damage [3]. The control of defect-enhanced diffusion during annealing is thought to be the key both to an understanding of distinct doping related defect levels in SiC and to a successful implantation-based nanostructure technology.

6H and 4H-SiC(0001) was implanted with 400keV Er ions to a dose of  $1 \times 10^{17} \text{cm}^{-2}$  at 700°C, followed by rapid thermal annealing at 1600°C for 3min under Ar atmosphere. Cross-sectional samples before and after annealing were prepared for transmission electron microscopy (TEM) using mechanical polishing, dimpling and low-angle Ar-ion milling and in one case just by tripod polishing. Conventional and high-resolution (HR) TEM was carried out in a JEOL 3010 and atomic-resolution high-angle annular dark-field scanning TEM (ADF-STEM) in a FEG-JEOL2010 equipped with electron energy loss spectrometer (EELS).

TEM and EDX-analysis on as-implanted specimen show that the most strained SiC region contains the region of Er content shows that Er is not clustered there but statistically distributed within the SiC matrix. Prevailing defects are interstitial loops in basal planes. After annealing, it was revealed by atomic-resolution ADF-STEM that single Er atoms collect and that there are at least 3-5 single Er atoms in one column. Together with strain analysis on HRTEM images it can be followed that the foreign atoms place preferably in the core of lower strain of SiC matrix defects. Fig. 1 shows one typical defect in atomic resolution Z-contrast and in high-resolution contrast. The chemical nature of the atoms confirmed EELS by scanning along a single Er atom column (see Fig. 1). Typical locations of Er atom columns will be described and their connection to ErSi<sub>2</sub> nanocrystal creation will be discussed. Moreover wider conclusions will be made to the case of Ge ion implantation.

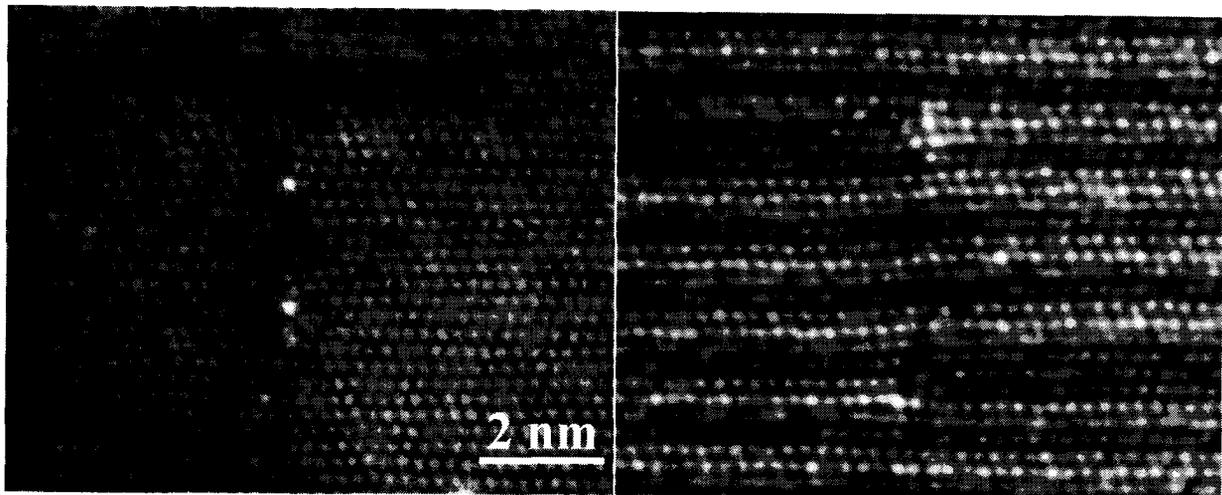


Fig. 1 Atomic-resolution ADF-STEM image showing Er atom columns at the ends of interstitial loops on the left and a corresponding defect imaged in HRTEM.

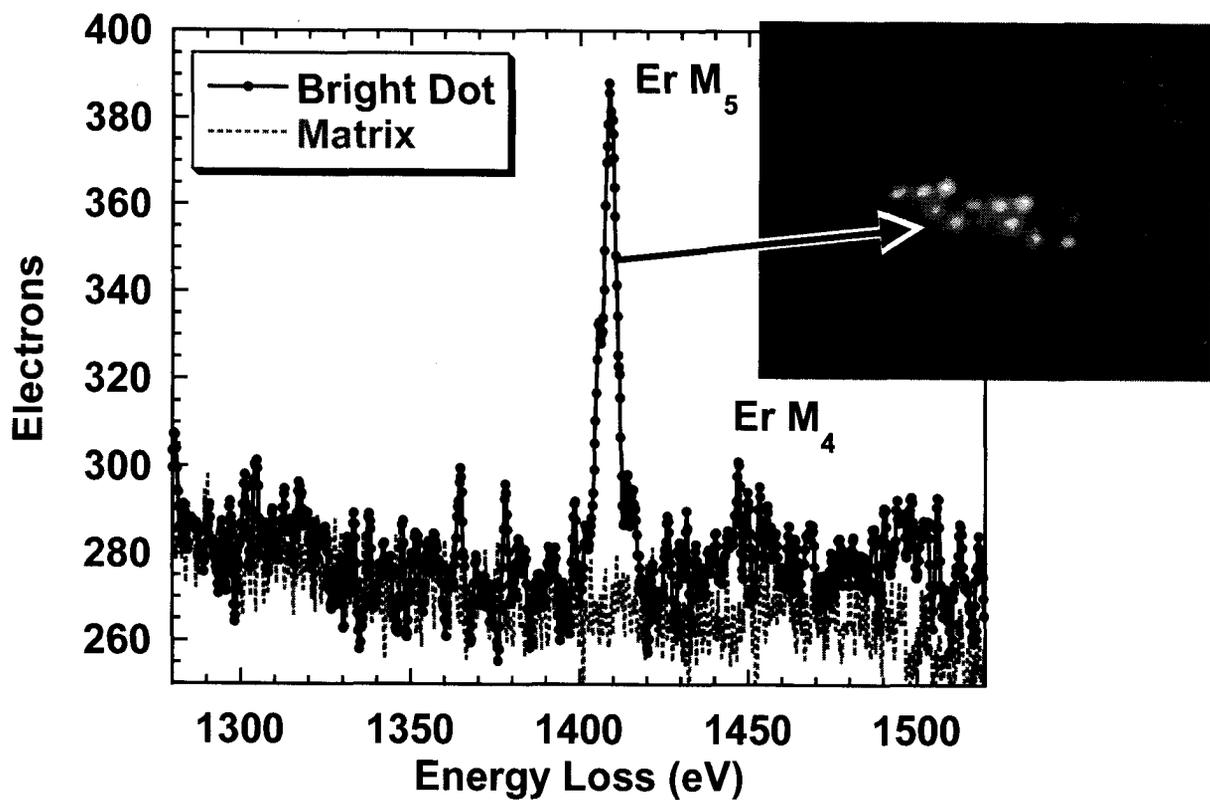


Fig. 2 A typical SiC matrix defect decorated by Er-atom columns together with the EELS spectrum of the Er M edge obtained from the single Er atom column, the arrow is pointing to.

#### References

- [1] R. P. Devaty, W. J. Choyke, Phys. Stat. Sol. (a) 162 (1997) 5
- [2] U. Kaiser, J. Electron Microscopy 50 (2001)
- [3] O. I. Lebedev, G. Van Tendeloo, A. A. Suvorova, I. O. Usov, A. V. Suvorov). J. Electron Microscopy 46: (1997) 271

## Direct Observation of the Solid Phase Recrystallization of Self-Implanted Amorphous SiC Layer on (11 $\bar{2}$ 0), (1 $\bar{1}$ 00), and (0001) Oriented 6H-SiC

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### 1. Introduction

The ion implantation method is used for selective doping in SiC device formation. In order to remove defects induced by ion implantation into the (0001) Oriented 6H-SiC, that is carried out at the substrate temperature over 500 °C, additional annealing is necessary at the high temperature above 1500 °C.<sup>1</sup> Satoh showed that the solid phase growth process is dependent on the crystal orientation.<sup>2</sup> It is clear that information of this type is essential to an understanding of the mechanism in which ion-implantation induced defects disappear. The present paper discusses the substrate orientation dependence on the kinetics of furnace-annealing induced solid phase recrystallization (SPR) of self-implanted amorphous layers on SiC substrate. We report on the use of an *in situ* time resolved optical reflectivity (TROR) measurement to monitor the position and roughness of the amorphous-crystal interface in real time.

### 2. Experimental

Samples of n-type ( $N_D - N_A \simeq 10^{17}/\text{cm}^3$ ) (11 $\bar{2}$ 0), (1 $\bar{1}$ 00), and (0001) oriented 6H-SiC were ion implanted with Si (40 keV  $1.5 \times 10^{15}/\text{cm}^2$  + 80 keV  $2 \times 10^{15}/\text{cm}^2$  + 110 keV  $5 \times 10^{15}/\text{cm}^2$ ) and C (20 keV  $1.5 \times 10^{15}/\text{cm}^2$  + 40 keV  $2 \times 10^{15}/\text{cm}^2$  + 60 keV  $4 \times 10^{15}/\text{cm}^2$ ) to create a self-implanted amorphous layer ( $\sim 150$  nm) on the wafer surface. Figure 1 shows the Si and C depth profiles calculated by TRIM program. Furnace induced SPR was accomplished on the resistively heated stage at 700 °C in air environment. The recrystallization kinetics was observed by the TROR technique.<sup>3</sup> The TROR signals provides a continuous, and sensitive measurement of a position and roughness of amorphous-crystal interface during SPR. A He-Ne laser ( $\lambda = 633$  nm) is used for the probe light.

### 3. Results and Discussion

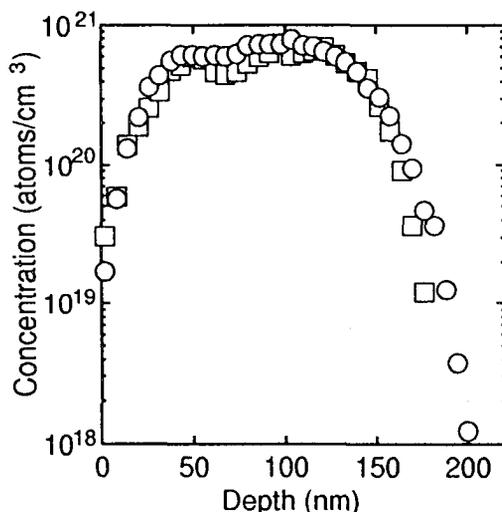


Fig. 1. Calculated profiles using TRIM of Si (○) and C (□).

In the TROR technique, oscillations of the reflectivity signal, due to interfering optical reflections from the surface and from the moving interface between the surface amorphous layer and the recrystallized SiC, are observed. Figure 2 shows a calculated reflectivity of amorphous SiC as a function of amorphous thickness on crystal SiC. Amorphous and crystalline SiC indices used in the calculation are  $4 - 0.612i$  and  $2.63 - 1.2 \times 10^{-5}i$ , respectively.<sup>4</sup> A complex reflective index of amorphous SiC was estimated by the comparison with the reflectivity of the silicon.

Figure 3 gives the shape of the TROR signals in each case for all orientations  $(11\bar{2}0)$ ,  $(1\bar{1}00)$ , and  $(0001)$ . In the  $(11\bar{2}0)$  orientation, the TROR signal is closed to the calculated curve in comparison with Fig. 2. By comparison of the TROR signal and the calculated curve, the interference maxima and minima are assigned at the depth of interface. The recrystallization rate estimated to be about 3.9 nm/min near initial amorphous-crystal interface. When the growth interface reached near the surface, TROR signal shows attenuation of the last reflectivity oscillation. It is shown that the roughness of the growth interface increases with the recrystallization from amorphous phase to crystal phase. Comparing the  $(1\bar{1}00)$  orientation growth with the case of  $(11\bar{2}0)$ , the recrystallization rate is late, and it estimated to be about 2nm/min. In addition to this property, the oscillation of the reflectivity observed around the surface has collapsed. It seems that whether the SPR stopped near surface layer or roughness of the regrowth interface increases severely. In the case of the  $(0001)$  orientation, the TROR oscillation nearly disappears, which shows a very rough regrowth interface induced by furnace annealing. We observed directly that the recrystallization interface was greatly roughened during annealing process of ion-implantation induced amorphous layer in the  $(0001)$  orientation SiC.

In conclusion, we have succeeded the observation of the recrystallization process of SiC amorphous layer using the *in situ* TROR technique, that strongly depends on the crystal growth orientation.

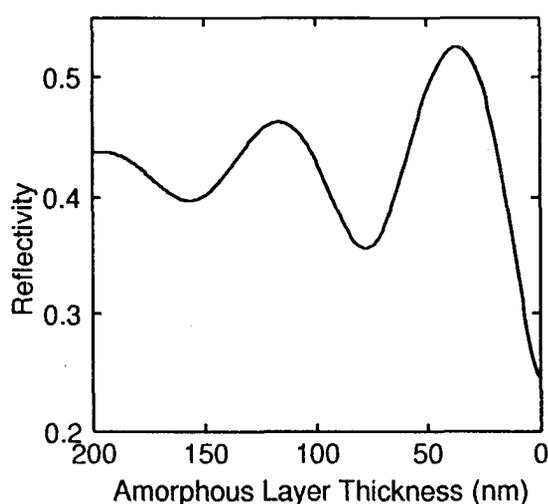


Fig. 2. Calculated reflectivity of amorphous SiC on crystal SiC as a function of amorphous layer thickness.

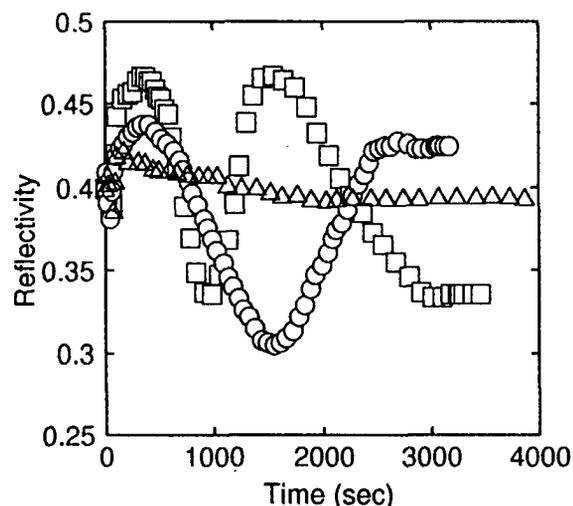


Fig.3. The TROR signals during SPR on  $(11\bar{2}0)$ (□),  $(1\bar{1}00)$ (○), and  $(0001)$ (△) oriented 6H-SiC.

#### References

- 1) T. Kimoto, A. Itoh, N. Inoue, O. Takemura, T. Yamamoto, T. Nakajima, and H. Matsunami, Mater. Sci. Forum **264-268**, 675 (1998).
- 2) M. Satoh, Y. Nakaike, and T. Nakamura, J. Appl. Phys. **89**, 1986 (2001).
- 3) G.L.Olson, S.A.Kokorowski, R.A.McFarlane, and L.D.Hess, Appl.Phys.Lett.**37**, 1019 (1980).
- 4) W. J. Choyke and E. D. Palik, in "Handbook of Optical Constants of Solids" (E. D. Palik, eds.), p. 587. Academic Press, Orlando, 1985.

## **Photoemission electron imaging of transition metal surface on Si and SiC**

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The introduction of ultra-high-vacuum (UHV) technology in emission microscopy had made photoemission electron microscopy (PEEM) a high-resolution surface-sensitive technique for the study of surface structures. The image in the PEEM system is based on the lateral photoemission intensity distribution from a solid sample surface. The contrast mechanisms of PEEM such as topographical, elemental, chemical, magnetic, and orientation contrasts allowed a real-time view on surface reactions such as islanding and agglomeration of metals as well as their dynamics. In this study, we have conducted a real-time imaging on the annealed surfaces of transition metal films on Si and SiC surfaces and have studied the morphological variations after in-situ annealing.

Thin metal films (1nm, 2 nm, 4 nm, 10 nm, and 50 nm) of Ti, Ni, and Pd were deposited either on Si or SiC and annealed inside the PEEM chamber at  $\sim 10^{-9}$  Torr by filament heating and electron bombardment. The images were taken after sequential annealing from RT to over 900 °C.

The PEEM system uses either high-pressure Hg arc lamp or synchrotron radiation for photoelectron emission and is attached to beamline BL-5 of Hiroshima Synchrotron Radiation Facility (HiSor), Hiroshima, Japan. The resolution of the system is about 15 nm and the field of view (FoV) can be varied from 2  $\mu\text{m}$  to 150  $\mu\text{m}$ .

We have imaged the formations of metals-nanostructures on Si and SiC surfaces, initial surface reactions as well as formations of islands (in ring-clusters) with sizes in order of microns. Also we have observed variations of brightness at elevated temperatures and contrast-reversal on some films that were due to deoxidation of the surface films and/or formation of reacted products such metal silicides and carbides/graphite. Figure 1 shows PEEM images of Ti on Si(100) surface at RT and after annealing at 700°C which is the formation temperature of Ti silicides. And Figure 2 shows Ni surface on 3C-SiC at (a) 200° and (b) 240°C.

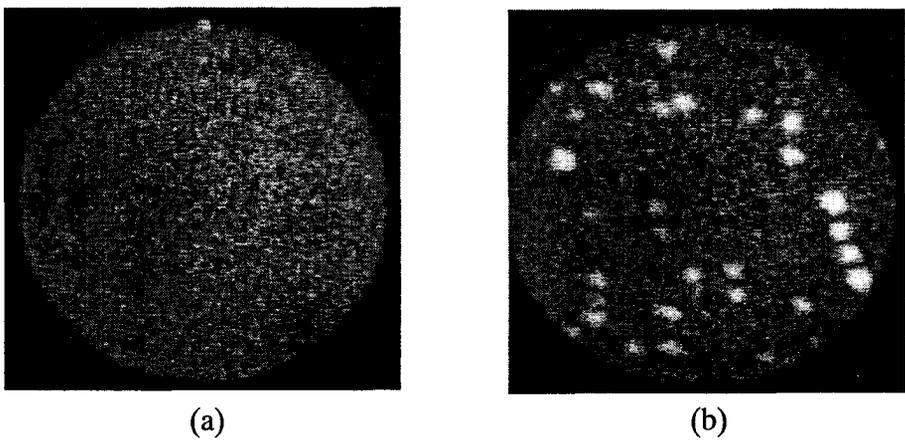


Figure 1. PEEM images of Ti (40nm)/Si(100) taken at (a) RT and (b) after 700°C.

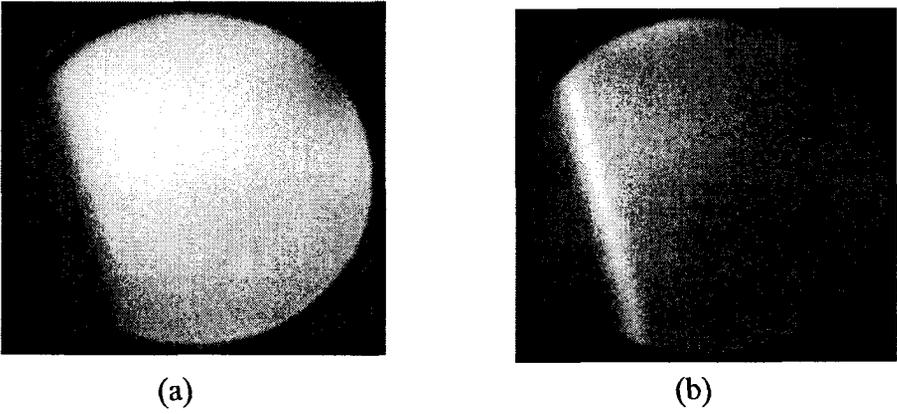


Figure 2. PEEM images of Ni (4nm)/3C-SiC taken at (a) 200 °C and (b) 240°C.

## HOLE ESCAPE FROM $\text{Ga}_{1-x}\text{In}_x\text{N}/\text{GaN}$ QUANTUM WELLS AND $\text{InAs}/\text{GaAs}$ QUANTUM DOTS.

V.A. Voitenko

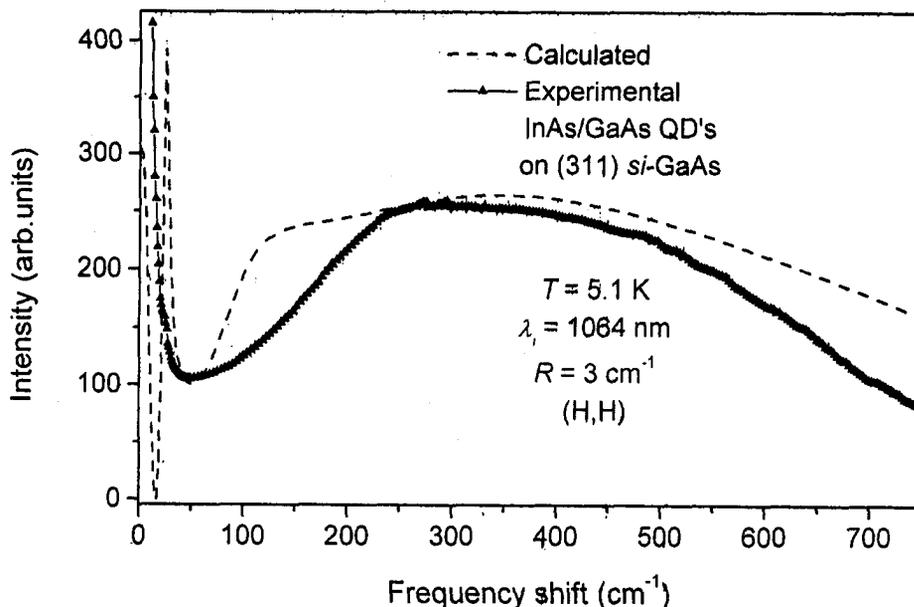
Technical State University, 195251, St. Petersburg, Russia.

It is shown clearly the anomalous photoexcitation of carriers in the  $\text{Ga}_{1-x}\text{In}_x\text{N}$  with  $x < 0.15$  quantum wells (QW's) and in  $\text{InAs}$  quantum dots (QD's) and their unusual photoinjection to respectively  $\text{GaN}$  and  $\text{GaAs}$  barriers via strong Coulomb interaction results in creation of the nonequilibrium two-component electron-hole plasma in the appropriate  $\text{GaN}$  or  $\text{GaAs}$  layers. This plasma seriously affects the performance of various III-nitrides based devices since it expands through the whole specimen marking the deepest place by light emission.

One of the most important and rich phenomena exhibited advances in solid state physics of nanometer-sized semiconductor layers embedded by QD's, or QW's in which electrons are confined in one or in all three directions of space, is the role of physical mechanisms determining the efficiency of optical transitions and carrier dynamics. Electron ( $e$ ) and hole ( $h$ ) wave functions and their overlapping in such heterostructures across well barriers control the dynamic strength of carrier fluctuations as well as  $e$ - $h$  and polar optical interactions and determine the transport and optoelectronic properties. A large spectral misfit existing between photoluminescence (PL) maximum and PL excitation (PLE) edge in  $\text{Ga}_{1-x}\text{In}_x\text{N}/\text{GaN}$  QW's is usually associated with punctuated island growth mode applied for these heterostructures. A localization of photoexcited carriers into the deepest QD-like potential fluctuation is responsible for light emission. The problem is how do carriers find their way and penetrate inside such a unique potential fluctuation. Related physical items are clarified already during recent development of  $\text{InAs}/\text{GaAs}$  based QD systems.

We have investigated slabs embedded with QD's consisting of 10 periods of 1.8 MLs  $\text{InAs}$  and 5.1 nm  $\text{GaAs}$  and also sets of  $\text{Ga}_{1-x}\text{In}_x\text{N}/\text{GaN}$  multiple QW structures. The effective diameter (base size) of  $\text{InAs}$  QD's was  $\approx 12$  nm and the distance between neighbor dots was 25 nm. Five 3 nm thick  $\text{Ga}_{1-x}\text{In}_x\text{N}$  QW's were embedded in 9 nm  $\text{GaN}$  barriers. Double difference in heterostructure constants is effectively compensated by respective ratio of base material dielectric constants:  $\epsilon_{\text{GaN}}/\epsilon_{\text{GaAs}} \approx 2$ . One of the most important points of this work is that we observed unconventional quasi- and inelastic electronic light scattering spectra in an intrinsic  $\text{GaAs}$  nanometer-sized layers embedded by QD's using a selective resonant excitation above the  $\text{InAs}$  band gap but below the  $\text{GaAs}$  band gap and respective absorption of  $\text{GaN}$ -based heterostructure. Giant enhancement (by a factor of  $10^6$ ) of optical transitions efficiency in such mesoscopic systems is registered. Despite much larger band offsets and relaxation of selection rules in  $\text{Ga}_{1-x}\text{In}_x\text{N}/\text{GaN}$  QW's as compared with the previous heterostructure respective enhancement is only accessible for a small number of interband transitions. The experimental observation of the enhanced in oscillator strength interband transitions results in the creation of unexpected for the case of intrinsic heterostructures the two-component nonequilibrium electron-hole plasma. We excite this novel plasma by photocreation of electrons and holes as Wentzel et. al.<sup>[1]</sup> do with the same (1064 nm line of  $\text{Nd}^{+3}$ :YAG laser, or Xe-white lamp with 0.25 m monochromator) source used for the detection of scattering or luminescence spectra. For the excitation density employed the electron-hole occupation number of the QD's itself should be approximately equal or less than 1 and the respective quantity for QW's is even more questionable. Therefore, an experimental observation of unexpected collective excitations of electron-hole pairs in QD's system unambiguously demonstrate that the two-component plasma is initially

induced by the two populations of free carriers separated in the real space. Such modes reveal the strong Coulomb electron-hole interaction. Electrons and holes are photoexcited in the QD's or QW's, but they are captured (trapped) or released due to overlapping of hole wavefunctions between neighbor QD's or QW's. Such processes can lead to a fluctuating charge distribution (configuration) outside the QD's or QW's. Thus, present experiments break the news about the most important phenomena leading to a fluctuating charge distribution outside the QD's or QW's and formation of free electrons and holes in the GaAs or GaN layers with efficient direct electromagnetic coupling between the carriers. The piezoelectricity in such strained and polarized low symmetry heterostructures causes the unexpected enhancement of the coupling strength as compared to the bulk case. Therefore the transport is determined by the properties of those carriers that are injected from the QD's or QW's into the undoped GaAs or GaN barriers. Summing up the intra-subband including quadrupole momentum scattering lineshape and zero temperature approximation acoustic plasmon (AP) peak with inter-subband contribution of scattering intensity, leads to the line shape presented in figure by dashed line. Measured light scattering spectra obtained for polarized configuration from InAs/GaAs QD's structure at a lattice temperature  $T_l = 5.1$  K [2] is plotted by solid line. Calculated spectrum describes well both AP peak position around  $25$   $\text{cm}^{-1}$  and quasielastic tail and fits well inter-sub-band maximum around  $250$ - $270$   $\text{cm}^{-1}$ . Successful comparison between experimental and theoretical scattering spectra provides an evidence of plasma homogeneity.



Though relative scaling of AP intensity to inter-sub-band continuum is evidently overestimated as compared with the experimental result preference for AP formation is much more effective than for the ordinary high-frequency optical plasmons in this nonequilibrium two-component uniform e-h plasma. There is a good chance to proceed with present Raman investigation for  $\text{Ga}_{1-x}\text{In}_x\text{N}/\text{GaN}$  multiple QW structures using polyphenil dye laser provided respective photodetector will be available.

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[1] C. Wetzel, T. Takeuchi, H. Amano, and I. Akasaki. *Phys. Rev. B* **62**, 13302(2000)

[2] B. H. Bairamov, V. V. Toporov, V. A. Voitenko, B. P. Zakharchenya, M. Henini, and A. J. Kent, submitted to *Phys. Rev. Lett.*

## Abnormal Hysteresis Property of SiC Oxide C-V Characteristics

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**Abstract.** In this paper, the electrical characteristics of the thermal oxide grown on SiC were discussed. For these studies, the MOS capacitors with the size of about  $31,400 \mu\text{m}^2$  were fabricated on a 6H-SiC wafer which had a  $5 \mu\text{m}$  thick n-type epi-layer with a doping concentration of  $3 \times 10^{15} \text{cm}^{-3}$ . An about 35 nm thick oxide layer was thermally grown in wet  $\text{O}_2$  at  $1150^\circ\text{C}$  for the dielectric layer.

The high frequency C-V measurement results of the MOS capacitors showed an abnormal hysteresis property, which was believed to be due to the movement of the electrons trapped inside the oxide layer. In addition, it was found that the oxide had quite a large low-level leakage caused by the trap-assisted tunneling and most of the traps were located in the region near the bottom of the gate oxide.

### II. Experiments

The MOS capacitors with the size of about  $31,400 \mu\text{m}^2$  were fabricated on a 6H-SiC wafer which had a  $5 \mu\text{m}$  thick n-type epi-layer with a doping concentration of  $3 \times 10^{15} \text{cm}^{-3}$ . An about 35 nm thick oxide layer was thermally grown in wet  $\text{O}_2$  at  $1150^\circ\text{C}$  for the dielectric layer. In addition, a 200 nm thick Al layer were deposited on the wafer and patterned by wet etching to form the gate electrode, and a 100 nm thick Ni layer were deposited on the backside of the wafer to form the ohmic contact on the substrate. Then the high frequency C-V characteristics and the leakage current were

measured using the HP4284A LCR meter and the HP 4156A parameter analyzer.

### III. Conclusions

An abnormal hysteresis property was observed from the high frequency C-V characteristics of the MOS capacitor with the thermal oxide grown on the SiC substrate as its dielectric layer. This was believed to be due to the movement of the electrons trapped in the deep level traps inside the oxide layer. The electrons might move back and forth from the trap sites near the bottom side of the gate oxide to those near the top side depending on the polarity of the gate bias voltage mainly during the holding time among the measurement steps.

On the other hand, quite a large low-level leakage was observed when the gate bias voltage was positive, while it was not when the gate bias voltage was negative. The large low-level leakage with the positive voltage gate bias was believed to be caused by the trap-assisted FN tunneling, where most of the traps were located in the region near the bottom of the oxide layer.

### Acknowledgments

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This work was also done as a part of SiC Device Development Program (SiCDDP) supported by MOCIE (Ministry of Commerce, Industry and Energy), Korea.

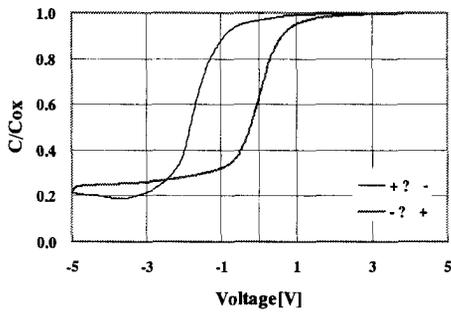


Fig. 1 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from +5V to -5V and consecutively from -5V to +5V and each step of 0.02V

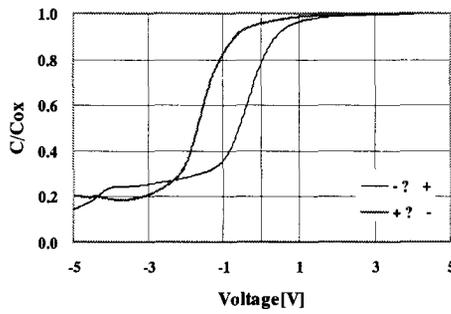


Fig. 2 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from -5V to +5V and consecutively from +5V to -5V and each step of 0.02V

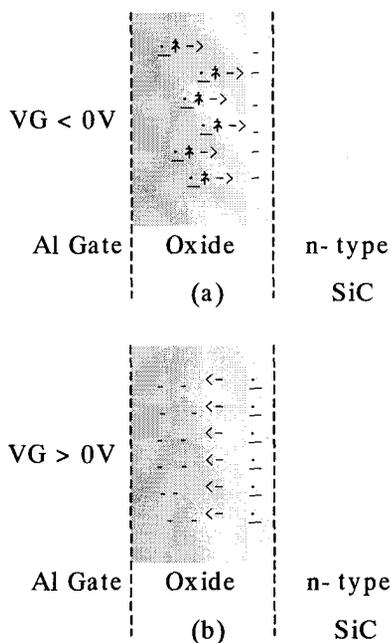


Fig. 3 Schematic diagram for trap-assisted

carrier transport (a) negative voltage and (b) positive negative voltage

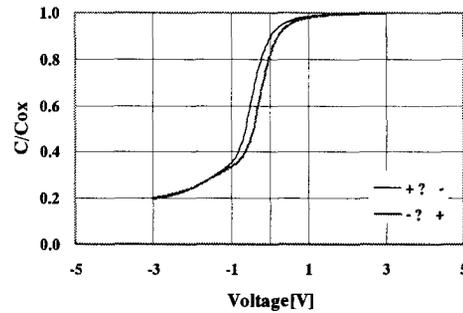


Fig. 4 High frequency C-V characteristics of SiC oxide with the gate voltage bias sweep from +3V to -3V and consecutively from -3V to +3V and each step of 0.02V

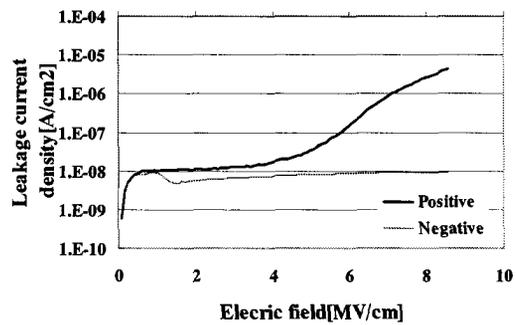


Fig. 5 Leakage Current of the SiC oxide of 35nm

**Electrical characteristics of 4H-SiC pn diode grown by LPE method**N. Kuznetsov,<sup>1,2</sup> D. Bauman,<sup>2</sup> A. Gavrilin<sup>1</sup><sup>1</sup> Ioffe Physico-Technical Institute, 26 Polytechnicheskaya str., St. Petersburg, 194021 Russia<sup>2</sup> Crystal Growth Research Center, 26 Polytechnicheskaya str., St. Petersburg, 194021 Russia

Recently, considerable progress in fabricating high power devices using SiC has been reached. It is well known that the basis of a bipolar device is a pn junction. In order to reach the excellent electrical characteristics of the bipolar devices it is necessary to improve quality of the pn junctions. The objective of the research is to study the electrical characteristics of pn diode grown by LPE method.

4H-SiC  $p^+pn_0n^+$  structures were grown by LPE method. First, a  $n^+$ -layer was grown on commercial 2-inch (0001)Si  $8^\circ$ -off 4H-SiC wafers. The  $n^+$ -layer serves as the layer for closing micropipe defects that usually exist on commercial substrates. The thickness of  $n^+$ -layer was 10 micron.  $N_d-N_a$  uncompensated impurity concentration in this layer was determined to be  $3 \times 10^{18} \text{ cm}^{-3}$ . An undoped  $n_0$ -layer was deposited on the  $n^+$ -layer. The thickness of  $n_0$ -layer was found to be (10-15)  $\mu\text{m}$ .  $N_d-N_a$  uncompensated impurity concentration in this layer was determined to be  $(9 \times 10^{15} \div 3 \times 10^{16}) \text{ cm}^{-3}$  for different samples. Al doped and Al heavily doped epitaxial layers were grown on  $n_0$ -layer in that order. The thickness of Al doped layers was (2.0 $\div$ 2.5) and (1.0 $\div$ 1.5) micron for p-layer and  $p^+$ -layer, respectively.  $N_a-N_d$  concentration in the p-layer was found to be  $(3 \div 6) \times 10^{18} \text{ cm}^{-3}$ . The  $N_{Al}$  concentration in the  $p^+$ -layer was determined using SIMS technique to be in order of  $1 \times 10^{20} \text{ cm}^{-3}$ .

To study the electrical characteristics of the 4H-SiC pn structures mesa-diode with ohmic contacts were formed. Cr/Al was used as backside ohmic contact to n-type substrate, and Al as ohmic contact to top LPE  $p^+$ -layer. Al and Cr metallization was deposited by thermal vapor evaporation. The top Al metallization was patterned by conventional photolithography to form dots with diameter of 150-1500  $\mu\text{m}$ . Mesa-diodes were fabricated by reactive ion etching in  $\text{SF}_6/\text{O}_2$  gas mixture.

The position of the pn junction in the epitaxial  $p^+pn_0n^+$  structure was determined using electron beam induced current (EBIC) measurements. A diffusion length of minority carriers in the  $n_0$ -layer (holes) was estimated by EBIC to be 1.5-3 microns for different samples.

The C-V characteristics of the pn junction were measured at different frequencies of 10 kHz and 1 MHz. The C-V characteristic of the pn junction was liner when plotted in  $C^2$ -V coordinates, which is typical for an abrupt junction. The cut-off voltage of the C-V characteristics was  $2.97 \pm 0.02 \text{ V}$ . The value of built-in potential was calculated to be  $\sim 3.0 \text{ eV}$ , which is close to theoretical value of the built-in potential for a 4H-SiC pn structure doped with nitrogen and aluminum.

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Low current forward – bias testing was performed in the temperature range from 300 to 700 K (Fig.1). The forward I-V characteristics contain an exponential region:  $I_f = I_s \times \exp(V/V_0)$ , where  $I_f$  is forward current,  $I_s$  is the saturation current. The value  $V_0$  was found to be independent on temperature and was determined to be about 0.1 V. The  $I_s$  showed exponential behaviour depending on temperature (Fig.2):  $I_s = I_{s0} \times \exp(T/T_0)$ , where  $I_{s0}$  is saturation current independent on temperature. The value of  $T_0$  was determined to be 38.4 K. The basic property of the forward I-V characteristics is the fact that the slope of the exponential curve  $\log(I)$  vs  $V$  doesn't change as a function of temperature (Fig.1). To explain such experimental results, we suppose that the electronic transport in the investigated pn junction is limited by the tunneling rate of electrons from the conduction band of n-type material into the deep traps with subsequent recombination with holes through the deep traps. We propose that there is defect layer between n<sub>0</sub>- and p-layers. The deep traps are proposed to be located in the defect layer. Thus, the according experimental data the forward I-V characteristics for current range from  $10^{-10}$  to  $10^{-3}$  A in the temperature range from 300 to 700 K may be described by tunneling model of carrier transport.

The reverse I-V characteristics showed an abrupt breakdown at voltages around 150 – 500 V for different samples. Breakdown voltage,  $V_b$ , was determined as the voltage at which an abrupt change in the reverse current occurred. It was evaluated that the breakdown electrical field for the pn junction was  $\sim(1.3 \div 1.8) \times 10^6$  V/cm.

The investigation of electrical characteristics of pn diode grown by LPE method will be presented in detail.

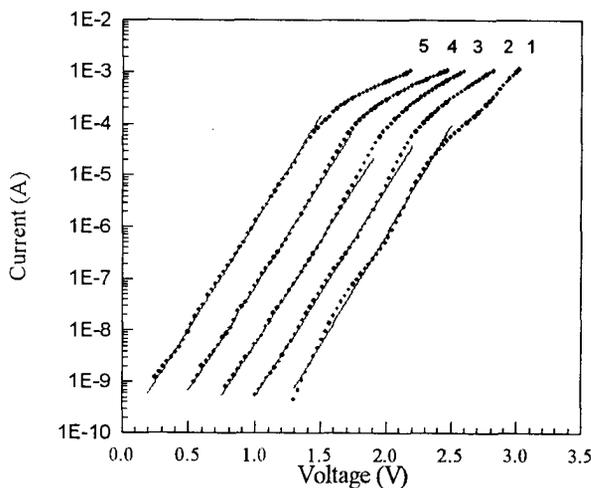


Fig.1. Forward I-V characteristics for a 4H-SiC pn diode measured at different temperatures: 1-300 K, 2-400 K, 3-500 K, 4-600 K, 5-700 K.

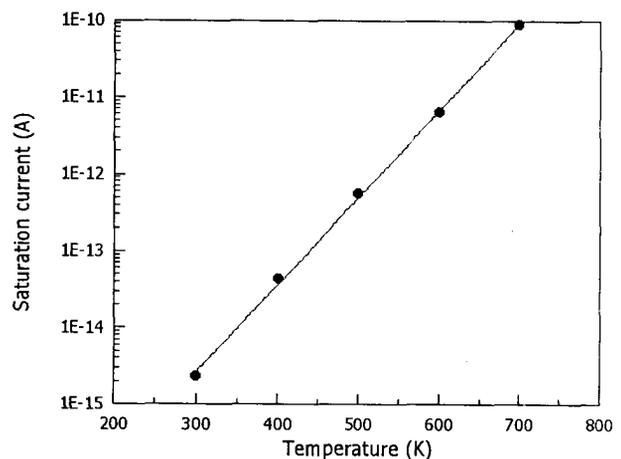


Fig.2. Saturation current as a function of temperature for a 4H-SiC pn diode.

### Acknowledgements

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## Wet-chemical preparation of silicate adlayer reconstructed SiC(0001) surfaces as studied by PES and LEED

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We have studied the effect of a wet-chemical cleaning procedure on SiC(0001) surfaces by photo electron spectroscopy (PES) using synchrotron radiation, and low-energy electron diffraction (LEED). This procedure is normally applied prior to the hydrogenation of SiC. [1-3] The four-step procedure [4] consists of step A: 10 minutes in a 4:1 mixture of H<sub>2</sub>SO<sub>4</sub> (97%) and H<sub>2</sub>O<sub>2</sub> (30%) at 180°C; step B: 10 minutes in HF (40%) at room temperature; step C: 10 minutes in a 4:1:1 mixture of H<sub>2</sub>O, H<sub>2</sub>O<sub>2</sub> (30%), and HCl (37%) at 80°C; step D: 5 minutes in HF (5%) at room temperature. Each step is followed by rinsing in deionized water. Photoelectron spectroscopy reveals that the wet-chemically prepared surfaces contain considerable amounts of oxygen. The amount of oxygen was found to be highest after step A of the wet-chemical procedure. The hydrogenation process allows the oxygen content to be pushed below the detection limit as was shown previously. [1-3]

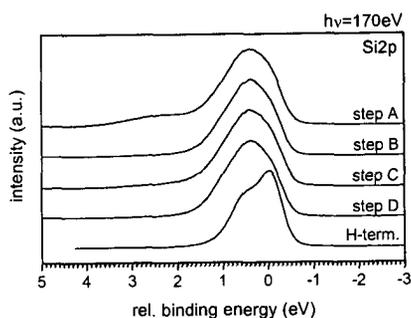


Fig. 1: Si2p spectra taken after the subsequent preparation steps at 170 eV photon energy.

preparation	Si <sup>+</sup> / SiC	Si <sup>4+</sup> / SiC
Step A	1.30	0.50
Step B	1.52	0.13
Step C	1.33	0.20
Step D	1.45	0.07

Table 1: Relative (to bulk SiC) contributions of the Si<sup>+</sup> and Si<sup>4+</sup> components to the Si2p spectra measured at 170eV photon energy.

intensity of the Si<sup>+</sup> component is almost constant. On the other hand, the Si<sup>4+</sup> component is highest after step A of the wet-chemical cleaning procedure. As expected, it is smallest after the HF etches (steps B and D) and has an intermediate value after step C which is also an

In figure 1, Si2p core level spectra are shown which were taken after each wet-chemical preparation step and after hydrogenation. Whereas the spectrum taken from the hydrogenated surface shows one single line due to stoichiometric SiC, [1-3] the wet-chemically treated surfaces contain Si in higher oxidation states. This is evident from the shape of the Si2p signals which extend to higher binding energies.

The corresponding C1s spectra (not shown here) revealed two components, one of which is due to the SiC, and the other one is originating in weakly adsorbed hydrocarbons which are absent in *in-situ* experiments. [1-3]

Fig. 2(a) displays a deconvolution of the Si2p spectrum taken after step A (topmost spectrum in fig. 1) into three Voigt doublets. The fit reveals that considerable amounts of Si<sup>+</sup> and Si<sup>4+</sup> are present at the surface. This is evident from the additional components which are shifted with respect to the bulk line by 0.5 eV and 2.0 eV, respectively. The intensity ratios determined for all four wet-chemical preparation steps are compiled in table 1. As can be seen from the table the relative

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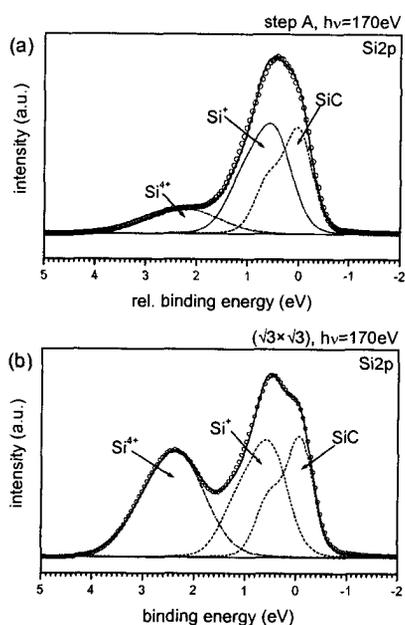


Fig. 2: Deconvolution of the Si<sub>2p</sub> spectrum obtained from (a) the SiC(0001) surface after preparation step A and (b) of a SiC(0001) surface with silicate adlayer.

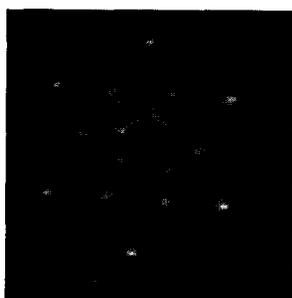


Fig. 3: LEED pattern taken at 70eV from a SiC(0001) surface after a modified preparation step A.

time that the silicate adlayer reconstruction was observed after a wet-chemical treatment. The results will also be discussed in the light of recent oxidation studies on SiC(0001) [8,9].

#### References:

- [1] N. Sieber, B.F. Mantel, Th. Seyller, J. Ristein, L. Ley, T. Heller, D.R. Batchelor, and D. Schmeißer, *Appl. Phys. Lett.* 78 (2001) 1216.
- [2] N. Sieber, Th. Seyller, B.F. Mantel, J. Ristein, and L. Ley, *Mater. Sci. Forum* 353-356 (2001) 223.
- [3] N. Sieber, B.F. Mantel, Th. Seyller, J. Ristein, and L. Ley, *Diamond Relat. Mater.* 10 (2001) 1291.
- [4] W. Kern, *Handbook of semiconductor wafer cleaning technology* (Noyes Publications, Park Ridge, 1993).
- [5] U. Starke, Ch. Bram, P.-R. Steiner, W. Hartner, L. Hammer, K. Heinz, and K. Müller, *Appl. Surf. Sci.* 89 (1995) 175.
- [6] N. Sieber, M. Hollering, J. Ristein, and L. Ley, *Mater. Sci. Forum* 338-342 (2000) 391.
- [7] J. Bernhardt, J. Schardt, U. Starke, and K. Heinz, *Appl. Phys. Lett.* 74 (1999) 1084.
- [8] F. Amy, H. Enriquez, P. Soukiassian, P.-F. Storino, Y.J. Chabal, A.J. Mayne, G. Dujardin, Y.K. Hwu, and C. Brylinski, *Phys. Rev. Lett.* 86 (2001) 4342.
- [9] C. Virojanadara and L.I. Johansson, *Surface Science* 472 (2001) L145.

oxidizing step.

Wet-chemically treated surfaces were previously shown to be terminated by OH groups. [5] Thus, the Si<sup>+</sup> signal observed after steps B, C and D can be assigned to Si-OH units. The fact that the Si<sup>+</sup>/SiC ratio is constant points towards a monolayer coverage with OH as was also suggested by Starke et al. [5]

The Si<sup>+</sup> signal after step A has at least partially to be assigned to a different bonding arrangement. The fingerprint of the spectrum is very similar to the one observed on a silicate adlayer-terminated SiC(0001) surface with ( $\sqrt{3}\times\sqrt{3}$ )-R30° periodicity. [6] This silicate adlayer reconstruction is an oxygen rich termination of both, SiC(0001) and Si(000 $\bar{1}$ ) surfaces and its structure was studied by Bernhardt et al. [7] using LEED. Figure 2(b) shows the deconvoluted Si<sub>2p</sub> spectrum of such a surface, which was prepared in a hydrogen plasma. On this surface, the Si<sup>+</sup>/SiC ratio is 1.21. The Si<sup>4+</sup>/SiC ratio, however, is 1.39 and thus three times larger than on the wet-chemically prepared surface, indicating that on the latter surface about one third of the surface is covered with the silicate adlayer reconstruction.

Indeed, despite the fact that only about one third of the surface was covered with the silicate adlayer, a weak ( $\sqrt{3}\times\sqrt{3}$ )-R30° LEED pattern was observed on that surface. The quality of the LEED pattern, and thus the degree of surface order, depends on the conditions of the preparation, e.g. the etch time, temperature and the composition of the Piranha solution. A clear ( $\sqrt{3}\times\sqrt{3}$ )-R30° LEED pattern (figure 3) was observed after a modified preparation Step A (10 minutes, H<sub>2</sub>SO<sub>4</sub> : H<sub>2</sub>O<sub>2</sub> = 3:1, 200°C). To our knowledge this is the first

## Some of comparative properties of diffusion welded contacts to 6H- and 4H-silicon carbide

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In the paper submitted at the last ECSCRM'2000 conference we had reported about our initial results in forming thick and large area aluminium contacts to 6H- and 4H-SiC using diffusion welding (DW) technique [1].

The favourable points of the work determining the practical clearness for the further R&D, in our opinion, are the follows:

- the possibility to perform by DW reliable, homogeneous large area thick Al contacts both to 6H- and 4H- silicon carbide;
- the possibility to make the Al / SiC Schottky contacts with evident non-linear I-V characteristics.

All the above gives every reason to continue the work in diffusion welded contacts to silicon carbide since there are the prospect to form in comparatively simple way the Schottky contacts able for commutation of heavy currents and on the other hand such metallization technique can be propagated on the other types of SiC p-n structures for power semiconductor devices.

The n-type wafers used in our early experiments were from Cree Research, Inc.: 6H-SiC substrates of  $3.6 \times 10^{18} \text{ cm}^{-3}$  doping concentration without epilayer, and 4H-SiC(I) with 5  $\mu\text{m}$ . thick epilayer of  $2 \times 10^{17} \text{ cm}^{-3}$  doping concentration. In both cases the doping concentrations were too high for operating Schottky diode, so for the next series of experiments the epiwafer of 4H-SiC(II) was purchased from Sterling Semiconductor, Inc. The nitrogen dopant in 6.75  $\mu\text{m}$ . epilayer was  $4.75 \times 10^{15} \text{ cm}^{-3}$  net concentration and the surface treatment was as Si-face polished and C-face ground.

The expert examination was made for the wafer to reveal the structural defects, their densities and distribution upon the surface area. Hence, it was determined the sections of the wafer surface most favourable for Me contacts. The macro – and microprofiles of Si- and C- faces of the wafer was measured to estimate the conformity of wafer configuration for DW process.

The I-V characteristics for Al / SiC Schottky contacts were measured in temperature range  $20^\circ \div 600^\circ \text{ C}$ .

On the special prepared specimens the specific series contact on-state resistance (R<sub>sp</sub>) was carried out for 6H-SiC substrate and for 4H-SiC(II) epiwafer. R<sub>sp</sub> was determined by surface potential distribution measurement near by the spot of metal contact (S.C. extrapolation method [2]).

It is clear from the Fig. 1 that the Schottky contact formed in relatively free of defects area of the 4H-SiC(II) wafer with low dopant concentration ( $4.75 \times 10^{15} \text{ cm}^{-3}$ ) has 20 times as large the reverse voltage than that in defected 4H-SiC(I) wafer with donor concentration  $2 \times 10^{17} \text{ cm}^{-3}$ .

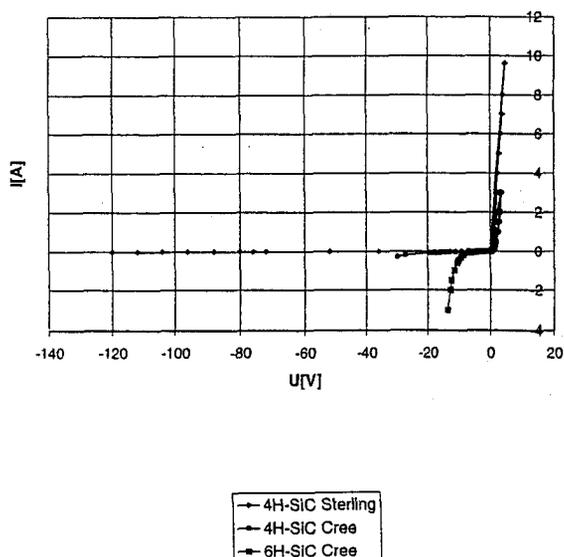


Fig. 1. I-V characteristics for 6H- and 4H-SiC structures at room temperature.

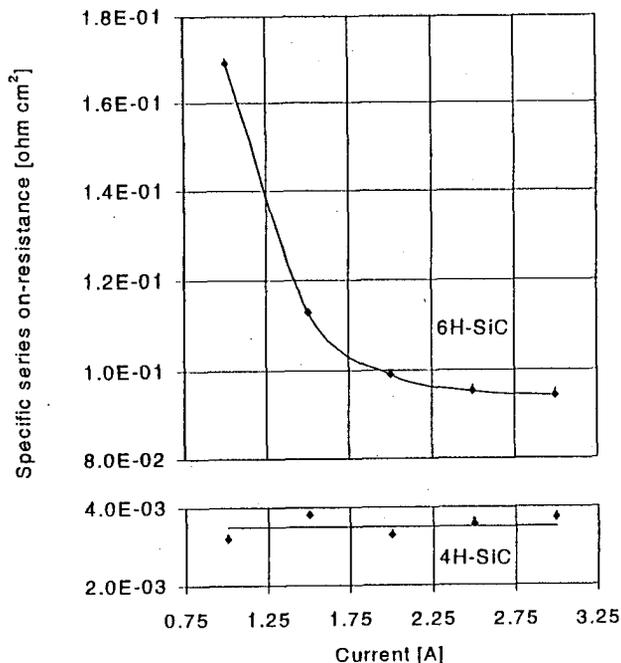


Fig.2. Variation of specific series on-resistance vs. measurement current.

Non-linearity of I-V characteristics becomes more evident not only in reverse branch but in forward branch too. For  $I_F = 3A$  -  $U_F = 3.45V$  for 4H-SiC(I) and  $U_F = 1.86V$  for 4H-SiC(II).

Increase in non-linearity is to be in confirmation with the results of series contact resistance measurement. Fig.2 shows the variation of the series on-state contact resistance for 6H-SiC substrate and for 4H-SiC(II) epiwafer. It is clear that the contact on-resistance for 4H-SiC(II) is more than order lower than that of 6H-SiC substrate, indicating more or less constant on-resistance with increase in measurement current (at least in a current range of 1 to 3A).

By this time experience in using of **DW** technique applied to metal contacts for semiconductors it is possible to predict with confidence that the manufacturing of power semiconductor devices based on silicon carbide will be determined not so much as by the possibilities of **DW** technique, but by the imperfections in SiC wafers. Thus, the dimensions of metal contacts and therefore the power dissipation at high on-current as well as reverse leakage will depend on the dimensions of relatively free of defects area of silicon carbide wafers.

## References

- [1] O.Korolkov, T. Rang, In abstract ECSCRM'2000, Kloster Banz, Germany Sept. 3-8, 2000, p.188.
- [2] H.H.Berger: J.Electrochem.Soc., vol 119, № 4, 1972, 507-514.

## Reliable ohmic contacts to LPE p-type 4H-SiC for high power p-n diode

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Silicon carbide is a semiconductor material in which a unique combination of wide bandgap, high saturation electron velocity, high breakdown field, low dopant diffusivity and high thermal conductivity is observed. These properties and a recent progress in the device processing determine SiC as the most appropriate material for high power microelectronics.

Despite the successful solution of many technology problems in the SiC device fabrication, the reliability of the ohmic contacts remains as a factor that restrict the high power device applications. The combination of good electrical and physical characteristics with stability at high operating temperatures is the principal requirement to the ohmic contacts and a prerequisite for the reliability of the power SiC devices.

Two kinds of p-type ohmic contacts to SiC, namely Al-based and Pd-based, have been studied in respect to their application in the high power p-n diode. The Al-based contacts, which have been the subject of our investigation, are the widely used Ti/Al contacts together with the Al/Si and AlSiTi ones. Pd is a very promising metal for low resistivity p-type ohmic contacts to SiC. For that reason, Pd-based contacts such as Pd, Pd/Ti, Pd/Al and new Pd/Si and Pd/Ti/Pd ones have been studied concerning their thermal properties as an alternative of the Al-based contacts for high temperature and high power applications.

The contacts investigated were formed on p-type 4H-SiC layers grown by liquid phase epitaxy (LPE) with a thickness of 0.5  $\mu\text{m}$  and a doping concentration of  $3 \times 10^{19} \text{ cm}^{-3}$  -  $1 \times 10^{20} \text{ cm}^{-3}$ . The LPE layer was grown on a commercially available structure having a top p-type ( $1 \times 10^{19} \text{ cm}^{-3}$ ) 1  $\mu\text{m}$  thick CVD epitaxial layer grown on n-type substrates. The contact deposition was performed by a subsequently electron beam evaporation of the metals in vacuum of  $1 \times 10^{-6}$  torr or by sputtering in argon at pressure of  $3 \times 10^{-3}$  torr. The annealing was carried out in a resistance furnace in an argon atmosphere at temperatures necessary to obtain the lowest resistivity of each contact type. A contact resistivity in the range of  $10^{-5} \Omega \cdot \text{cm}^2$  has been obtained for both Al-based and Pd-based contacts. Therefore, the reliability of the contacts at high temperature treatments is considered as the critical factor determining their power device applications.

The reliability of the contacts has been examined by investigation of their thermal stability. The latter has been estimated by the contact resistivity behaviour during the ageing test, temperature-dependence test and temperature-current treatment test.

Ageing of the contacts for a long time has been carried out at a constant temperature ranging from 500  $^{\circ}\text{C}$  to 700  $^{\circ}\text{C}$  in an inert atmosphere ( $\text{N}_2$ ) and in air. In fixed time intervals the contacts are cooled to the room temperature and the contact resistivity has been determined. The contact resistivity has been measured always at room temperature.

In the temperature-dependence test the measurements have been proceeded at a temperature increasing smoothly from 25  $^{\circ}\text{C}$  to 450  $^{\circ}\text{C}$  in air. This study gives information on the contact reliability at the corresponding operating temperature as the contact resistivity has been measured during the heating.

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During the temperature-current treatment a current with a pre-set density (up to  $10^4$  A/cm<sup>2</sup>) is passed for a fixed time through the contacts at a constant temperature (up to 500 °C). This test has been also performed in air and contact resistivity has been measured at the corresponding temperature.

The experiments on ageing of the contacts developed started with heating at 500 °C in nitrogen for 100 hours. Al-based contacts as well as the Pd-based ones did not change the contact resistivity during this treatment indicating a good thermal stability (fig.1). The both contact types were also stable at operating temperatures up to 450 °C in air (fig.2). The preliminary results show that Al-based and Pd-based contacts can be used in power diodes. For that reason, the following experiments on the ageing test in air and the temperature-current test will be ultimate for the suitable contact system determination.

The results obtained on the reliability of the ohmic contact to p-type LPE 4H-SiC will be summarized and discussed in respect to their application in a high power p-n diode.

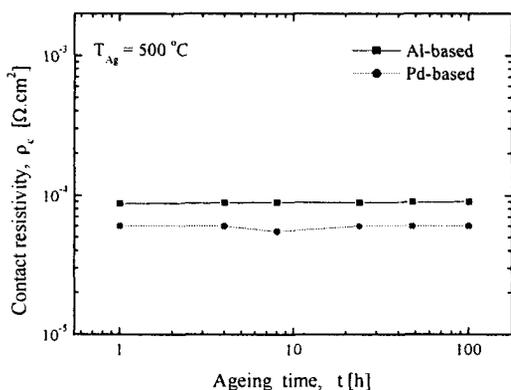


Fig. 1 Resistivity values of Al-based and Pd-based ohmic contacts to LPE p-SiC at an ageing temperature of 500 °C.

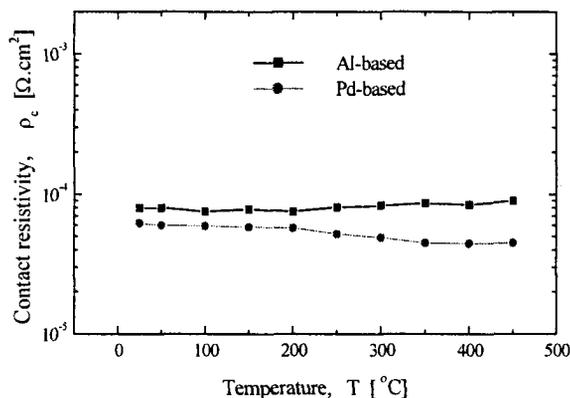


Fig. 2 Resistivity values of Al-based and Pd-based ohmic contacts to LPE p-SiC at different operating temperatures.

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## Ti ohmic contact on p-type 4H-SiC

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Formation of ohmic contacts to p-type SiC semiconductor is known to be difficult, since it has a large Schottky height. Limited work has been reported about the ohmic contacts to p-type 4H-SiC, in which aluminum based metals have been used. The aluminum-based metals have drawbacks of low melting point and high driving force of oxidation in the full procedure of device fabrications. Titanium has a relatively high melting point, thus Ti-based metal contacts were attempted in this study.

Material and electrical properties of Ti ohmic contacts on p-type 4H-SiC were investigated depending on the post-annealing and the metal covering conditions. Best results are obtained as  $2 \times 10^{-4}$  ohm/cm<sup>2</sup> for a Pt/Si/Ti metal structure after a vacuum annealing at 900 C for 90 sec. The contact resistance was measured by a transmission line technique, and the contact resistances were improved more than one order compared to Ti and Si/Ti contacts for the annealed samples at the same conditions. Auger depth profile data shows that the Pt layer effectively reduce the oxidation of Ti films, and X-ray diffraction pattern presents that the silicon layer plays a role of diffusion barrier to the intermixing of Ti and Pt atoms, which was considered as a major cause for the large contact resistance.

### Acknowledgements

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### References

1. S.K. Lee, C.M. Zetterling, M. Ostling, J.P. Palquit, H. Hogberg, and U. Jansson, *Solid-State Electronics*, 44 (2000) 1179.

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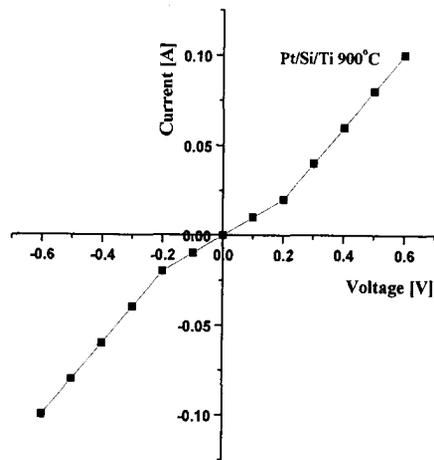


Fig. 1. I-V Characteristics Pt/Si/Ti/ p-type 6H-SiC after annealing at 900°C for 60sec.

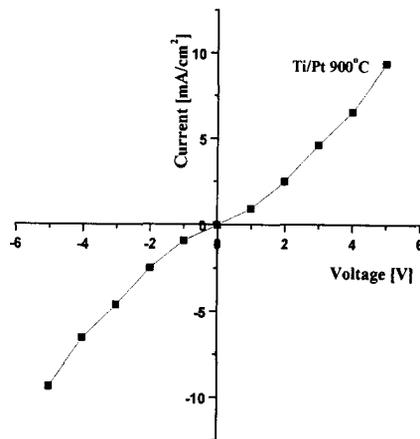


Fig. 2. Pt/Ti/ p-type 4H-SiC after annealing at 900°C for 90sec.

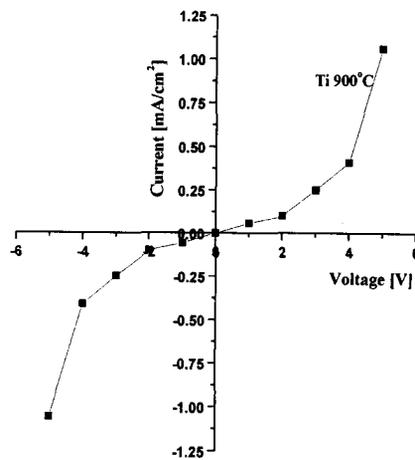


Fig. 3. Ti/ p-type 4H-SiC after annealing at 900°C for 90sec.

## NiSi<sub>2</sub> ohmic contact to n-type 4H-SiC

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4H-SiC is of great attractive for high power control and high frequency devices in polymorphism SiC because of high electron mobility and wide band gap. In this study, we investigated the structural and the electrical properties of NiSi<sub>2</sub> ohmic contact to n-type 4H-SiC. We have been reported NiSi<sub>2</sub> ohmic contact to n-type 6H-SiC, which is synthesized by annealing the deposited Ni and Si films at 900 °C without the reaction between Ni and SiC substrate and reveals the ohmic characteristic for the carrier concentration above  $1 \times 10^{16}$  cm<sup>-3</sup>[1].

Samples used in this study were a 0.2-um-thick, N-doped epitaxial layer, with a carrier concentration of  $2 \times 10^{18}$  cm<sup>-3</sup>, grown on p-type 4H-SiC substrate. After a sacrificial oxidation and HF treatment, Si film with a thickness of 92.5 nm and Ni film with a thickness of 25 nm were deposited on (0001) Si face of the sample by mean of E-gun evaporation in a vacuum of the order of  $10^{-5}$  Pa. The thicknesses of Si and Ni films were designed to produce the stoichiometric NiSi<sub>2</sub> alloy. The samples were annealed at 900 °C for 10 min in a flow of Ar gas containing 5 wt.% H<sub>2</sub> gas. The composition of the formed alloy was investigated using Rutherford Backscattering spectrometry (RBS) with 1.5 MeV <sup>4</sup>He<sup>+</sup> ions at a scattering angle of 150°. Current-voltage (I-V) characterizations were performed using Keithley 2400 source-meter combined with a micro-probe equipment at room temperature. The contact resistances were evaluated using transmission line model (TLM) method.

Figures 1 shows RBS spectra taken from Ni/Si/SiC sample before and after annealing at 900 °C for 10 min, respectively. The decrease in yield and the increase in energy width of backscattering signals from Ni and Si atoms are caused by the annealing. This result indicates that the deposited Ni film reacts with Si film by annealing at 900 °C for 10min. The atomic ratio of reacted Ni and Si was estimated to be 1:2, which corresponds to the stoichiometry of NiSi<sub>2</sub>. Since the composition of the formed Ni-silicide is in good agreement with the ratio of amounts of deposited Si and Ni atoms, the deposited Ni and Si films form NiSi<sub>2</sub> alloy without the reaction with 4H-SiC substrate. As described in our previous paper, in Ni-Si system, since NiSi<sub>2</sub> alloy is the most Si-rich Ni-silicide, the stoichiometric deposition of Ni and Si films restricts the reaction of Ni and SiC substrate. The sharp edge of lower energy side in Ni signals from NiSi<sub>2</sub> indicates that the interface between NiSi<sub>2</sub> and SiC

substrate is abrupt as well as the case of 6H-SiC.

NiSi<sub>2</sub> contact showed a good ohmic characteristic to n-type 4H-SiC. Figure 2 shows the plot of resistance vs electrode distance for the NiSi<sub>2</sub> contact formed on 4H-SiC. The contact resistance ( $R_c$ ) and the specific contact resistance were estimated to be 5.0  $\Omega$  and  $2.7 \times 10^{-6} \Omega \text{ cm}^2$  using TLM-method, respectively. The specific contact resistance of NiSi<sub>2</sub> contact to n-type 4H-SiC is about three orders of magnitude smaller than that of 6H-SiC with the same carrier concentration. It is suggested that the Schottky barrier height of NiSi<sub>2</sub> contact to n-type 4H-SiC is estimated to be about 0.3 eV in according with the thermionic emission model, which is lower than that for n-type 6H-SiC (0.44 eV).[2]

In conclusion, we reported the structural and electrical properties of NiSi<sub>2</sub> ohmic contact to n-type 4H-SiC. NiSi<sub>2</sub> contact restricts the reaction between Ni metal and 4H-SiC substrate and forms the abrupt NiSi<sub>2</sub>/4H-SiC interface as well as the case of 6H-SiC. NiSi<sub>2</sub> contact shows good ohmic characteristics with a low specific contact resistance of  $2.7 \times 10^{-6} \Omega \text{ cm}^2$ , which is attributed with the low Schottky barrier height at the interface.

#### Reference

- [1] T. Nakamura, H. Shimada, and M. Satoh, Mater. Sci. Forum Vols., **338-342**, 985(2000)  
 [2] T. Nakamura and M. Satoh, submitted to J. Appl. Phys.

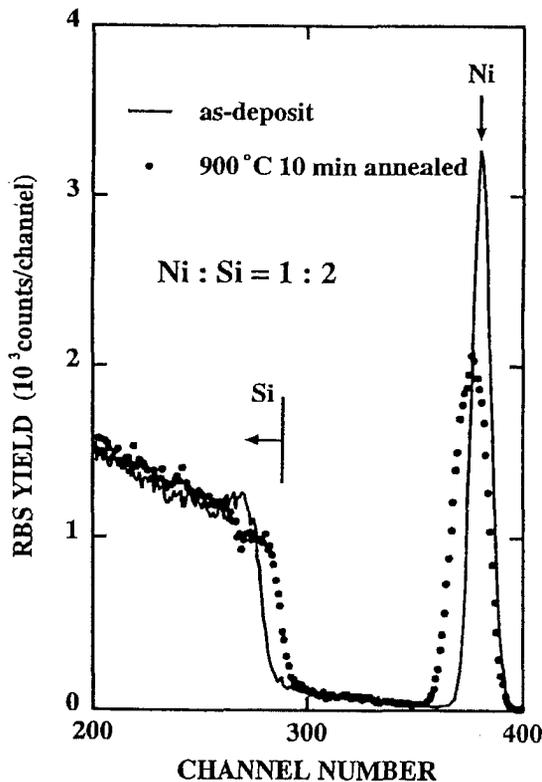


Figure 1

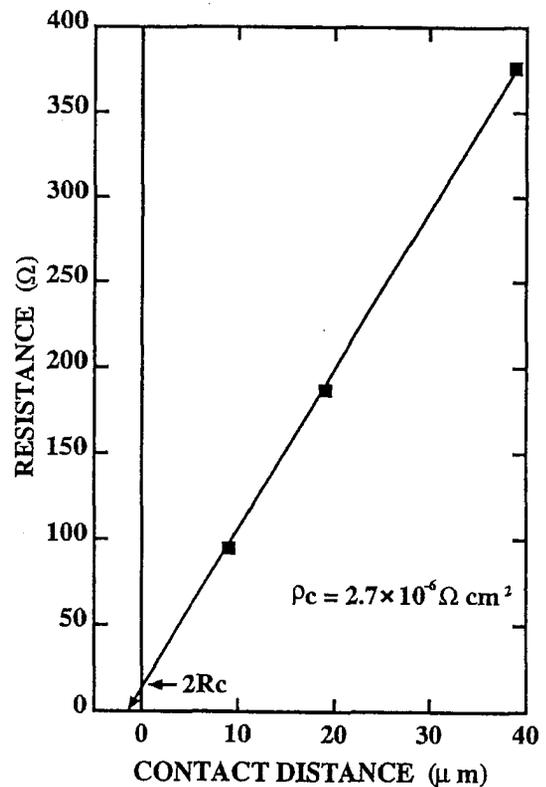


Figure 2

### **Influence of RTA on Ni/6H-SiC contact formation**

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Rapid thermal annealing (RTA) of metal contacts has more advantages as compared with conventional techniques of heat treatment. In this research an influence of various temperatures of RTA on Ni/6H-SiC contact formation on both (0001) and (0001) faces is presented<sup>1,2</sup>.

Single crystals samples of n-6H-SiC grown by Lely method with doping concentration of  $1-3 \times 10^{17} \text{ cm}^{-3}$  were used. In first, a Ni film has been deposited on a back side of the sample followed by annealing at 1100°C. After that, Ni contacts 300x300 microns in size were formed by photolithography on the front side. The annealing has been performed in vacuum during 10 sec at the temperatures from 400 to 1100°C in the ITA-18M system with a heat rate of 100 °C/sec<sup>3</sup>.

Current-voltage characteristics of the formed contacts after annealing at different temperatures for both Si- and C-face are presented in Fig.1. It is seen that before annealing and after annealing at 400°C the contacts have nonsymmetrical I-V characteristics. After annealing at the temperature more than 750°C, current-voltage characteristics become symmetrical. The temperature range from 400 to 750°C is, so called, intermediate range which is associated with transient processes in the metal-semiconductor interface. Based on the measured I-V characteristics, the barrier height, specific contact resistance, saturation current as well as series resistance have been extracted<sup>3</sup>.

Analysis of the obtained data showed that at the temperatures up to 400°C structural transformations in a Ni film, at the Ni-SiC interface, and at the near-surface region occur. This results in changing of a barrier height and surface state density. In the intermediate temperature range metastable fractions of nickel silicide are formed, while at the temperatures above 750°C the stable phase of NiSi and NiSi<sub>x</sub> are formed. Also, as it is shown, an influence of the type of a face on I-V characteristics is significantly less at the temperatures over 750°C, when the parameters of contacts mostly depend on properties of the interface NiSi<sub>x</sub>/SiC.

The obtained results have shown that characteristics of an interface of one- or multiplayer metal contacts depend on the annealing temperature and a heat rate as well<sup>4</sup>.

### References

1. R. Singh, *J. Appl. Phys.*, vol. 63, N 8, p. R59 (1988).
2. O.A. Agueev, A.M. Svetlichny, S.I. Soloviev, *Semiconductor Physics, Quantum Electronics & Optoelectronics*, vol 3, N 3, p. 379 (2000).
3. D.A. Sechenov, A.M. Svetlichny et al. *Elektronnaya Promyshlennost'*, N 3, p. 6, (1991) (in Russian).
4. M.W. Cole, P.C. Joshi et al. *J. Appl. Phys.*, vol. 88, p. 2652 (2000).

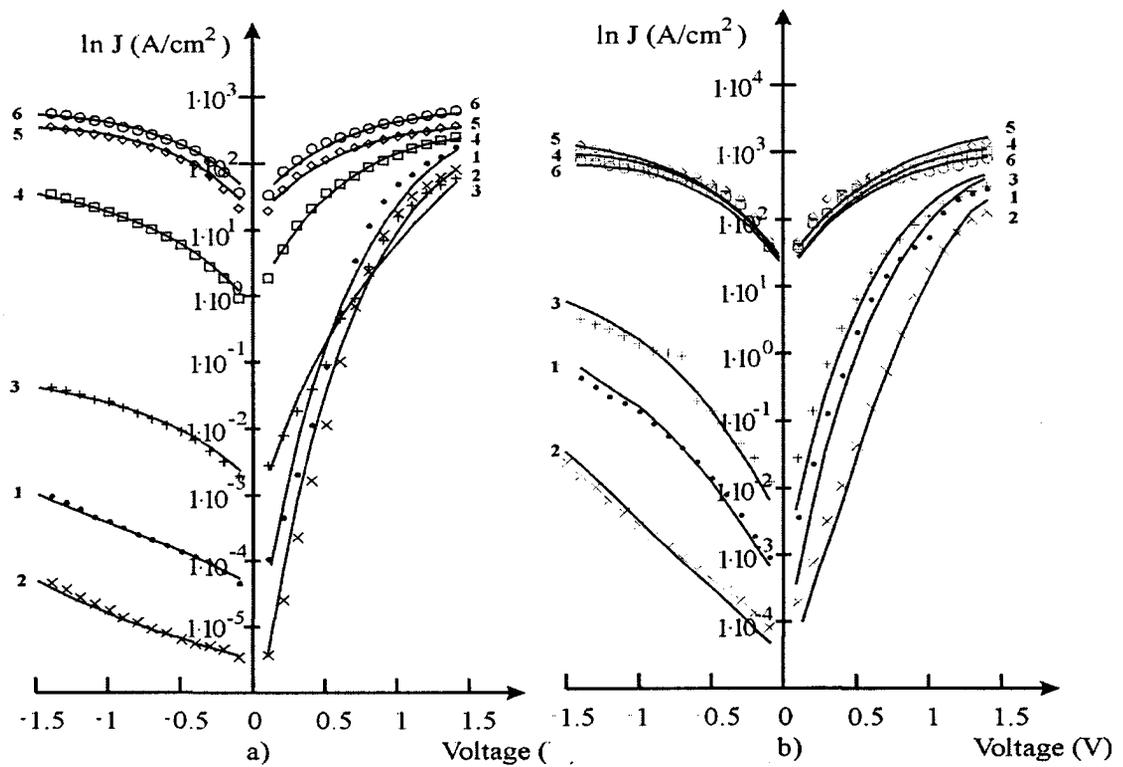


Fig.1. Current-voltage characteristics of contacts Ni/6H-SiC on (0001) face (a) and on (0001) face (b) after RTA at different temperatures: 1- as deposited; 2 – 400°C; 3 – 600°C; 4 – 750°C; 5 – 900°C; 6 – 1100°C.

### Effect of Rapid Thermal Annealing on Parameters of Ni/21R-SiC Contacts

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At present different SiC polytypes are finding ever-widening application in manufacturing of various devices of high-temperature electronics. The heating modes of choice for retention of the SiC phase composition are those using rapid thermal annealing (RTA) with incoherent IR radiation [1]. Here we present, for the first time, the results of investigation of the effect of RTA modes on the parameters of Ni contacts to 21R-SiC (0001) and 21R-SiC (000 $\bar{1}$ ) over a wide annealing temperature range.

The Leli-crystals of *n*-type 21R-SiC (electron concentration of  $3 \cdot 10^{18} \text{ cm}^{-3}$ ) were studied. At the first stage the Ni films 100 nm thick were formed on (0001) and (000 $\bar{1}$ ) faces using resistive sputtering. Then they were annealed in vacuum at a temperature  $T = 1100 \text{ }^\circ\text{C}$  for 10 s. After this similar Ni films were deposited onto the opposite faces and contacts (300×300  $\mu\text{m}$  in size) were formed using photolithography. The structures obtained were annealed in vacuum at different temperatures for 10 s (the rate of change of temperature was  $100 \text{ }^\circ\text{C/s}$ ) using the ITO-18MB set [2]. We checked the contact parameters after every annealing by measuring and analyzing the  $I$ - $V$  curves; besides, Auger (spectrometer LAS-2000) and structural investigations (atomic force microscope DI Nanoscope IIIa and roughness indicator Dektak 3030) were performed.

Shown in Fig.1 are the  $I$ - $V$  curves of the Ni/21R-SiC (000 $\bar{1}$ ) contacts after RTA at different temperatures. When the annealing temperature is below  $400 \text{ }^\circ\text{C}$ , then the contact  $I$ - $V$  curves are of the form of those for a Schottky diode. After annealing at temperatures over  $750 \text{ }^\circ\text{C}$  the  $I$ - $V$  curves become of the ohmic type. An analysis of the presented curves has shown that when the annealing temperature is increased, then the barrier height in contacts drops from 0.73 down to 0.38 eV, the saturation current grows and contact resistivity decreases down to  $2 \cdot 10^{-3} \text{ } \Omega \text{ cm}^2$ . It's remark, contact resistance estimated from  $I$ - $V$  characteristics is some overstated. The Auger concentration depth profiles taken for the Ni/21R-SiC (000 $\bar{1}$ ) contacts (as-deposited and after RTA at  $T = 1100 \text{ }^\circ\text{C}$ ) are given in Fig.2.

An analysis has shown that the above results are in qualitative agreement with those obtained by other authors [3,4]. When the annealing temperatures are over  $400 \text{ }^\circ\text{C}$ , then the processes in contacts are related to the interactions at interfaces. In this case several metastable nickel silicide phases appear with temperature growth. At high temperatures and under presence of excess Si stable NiSi and NiSi<sub>x</sub> phases can be formed [4]. It is shown that when the annealing temperature becomes over  $750 \text{ }^\circ\text{C}$ , then the parameters of contacts to 21R-SiC are determined by the blurred NiSi<sub>x</sub>-SiC interface and do not depend on the crystallographic orientation of the face. These results correlate with those concerning study of Ni surface morphology and Ni-SiC (000 $\bar{1}$ ) interface before and after RTA. At  $T = 1100 \text{ }^\circ\text{C}$  substantial changes have been observed at the Ni surface and interface (Fig.3). This is supported by the features of etching of the Ni-SiC structure. Up to  $T = 900 \text{ }^\circ\text{C}$  the Ni surface morphology demonstrates no substantial changes; contrary to this, at the Ni-SiC interface the morphology changes can be observed after RTA at  $T = 750 \text{ }^\circ\text{C}$ .

An analysis of the results of our investigations shows that one should exert thorough control over the annealing modes during thermal processing of contacts. This is necessary for regulation of both phase formation in the one- and multilayer contacts and carbon and silicon redistribution in the near-surface layer [5].

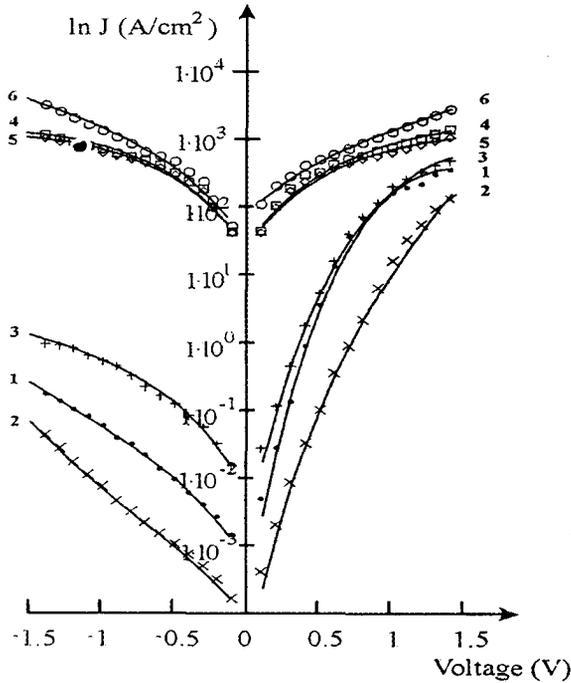


Fig.1.  $I$ - $V$  curves for the Ni/21R-SiC ( $000\bar{1}$ ) contacts before (as-deposited) (1) and after RTA at 400 (2), 600 (3), 750 (4), 900 (5) and 1100 °C (6).

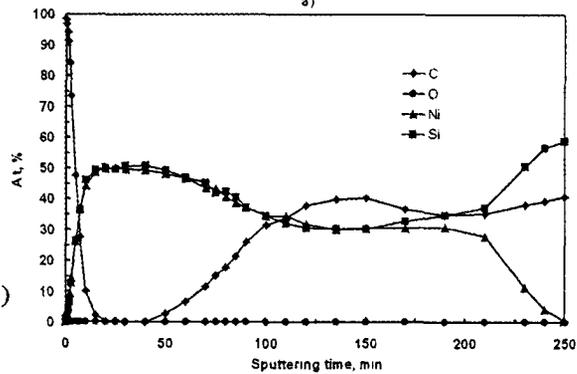
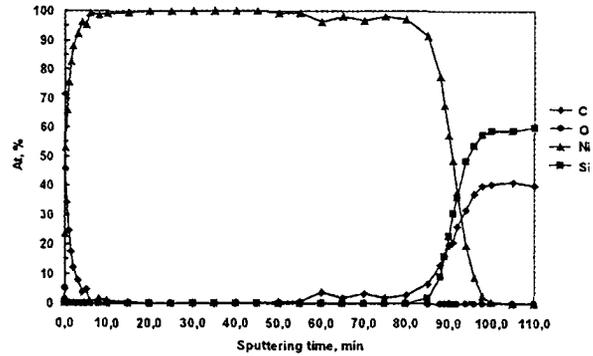


Fig.2. Auger concentration depth profiles taken for the Ni/21R-SiC ( $000\bar{1}$ ) contact: as-deposited (a) and after RTA at 1100 °C (b).

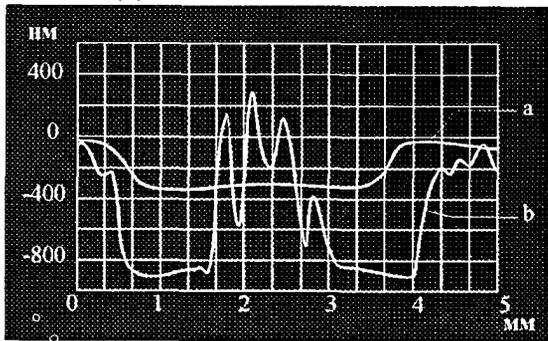


Fig.3. Auger crater profiles taken with the roughness indicator Dektak 3030 for the Ni/21R-SiC ( $000\bar{1}$ ) contact: as-deposited (a) and after RTA at 1100 °C (b).

## References

1. O.A. Agueev, A.M. Svetlichny, S.I. Soloviev, *Semiconductor Physics, Quantum Electronics & Optoelectronics*, vol.3, N 3, p. 379 (2000).
2. D.A. Sechenov, A.M. Svetlichny et al., *Elektronnaya Promyshlennost'*, N 3, p. 6 (1991) (in Russian).
3. S. Hara, T. Teraji et al., *Appl. Surf. Sci.*, vol. 117/118, p. 394 (1997).
4. A. Kakanakova-Georgieva, Ts. Marinova et al., *Thin Solid Films*, vol. 343-344, p. 637 (1999).
5. M.W. Cole, P.C. Joshi et al., *J. Appl. Phys.*, vol. 88, p. 2652 (2000).

## CoAl Ohmic contact materials with improved surface morphology for p-type 4H-SiC

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In order to manufacture high performance SiC electronics devices, development of low resistance Ohmic contact materials for p-type SiC is one of the key issues. TiAl Ohmic contact material provided contact resistivity ( $\rho_c$ ) as low as around  $10^{-6} \Omega\text{-cm}^2$ . However, this contact showed rough surface morphology after annealing at high temperatures due to excess Al addition to the TiAl contacts from the  $\text{TiAl}_3$  compound stoichiometry, which was required to obtain low contact resistivity. To improve the surface morphology of this contact, we investigated CoAl contacts, because Co was reported to react with SiC at lower temperature of  $600^\circ\text{C}$ . Also, the Co silicide contacts to p-type 6H-SiC were reported to have a low  $\rho_c$  value of  $10^{-6} \Omega\text{-cm}^2$  [Ref.1]. In addition, Co silicide is Ohmic contact materials have been extensively used in Si ULSI devices and would be easily applied to manufacturing SiC devices.

The purpose of this study is to develop the low resistance CoAl Ohmic contacts for p-type 4H-SiC with smooth surface morphology. We investigated the effect of the annealing temperature and the Al concentration on the electrical property and microstructure of CoAl Ohmic contacts.

A p-type epilayer ( $5\mu\text{m}$  thick) doped with  $1.0 \times 10^{19} \text{ Al/cm}^3$  was grown on the n-type 4H-SiC(0001) substrate by Cree Research, Inc. After chemical cleaning, the 10 nm thick  $\text{SiO}_2$  layer was formed on the substrate by dry-oxidation. The electrode pattern were made on the SiC surface by photolithography technique and the  $\text{SiO}_2$  layer was etched by diluted HF solution. Al and Co layers were sequentially deposited on the substrate in the high vacuum chamber by a resistance heater and an e-beam, respectively. A total typical layer thickness of Al and Co contacts was aimed to be 180 nm. After lifting off the photoresist, the samples were annealed at temperatures ranging from  $800^\circ\text{C}$  to  $1000^\circ\text{C}$  in the ultra high vacuum chamber. The annealing was carried out at  $800^\circ\text{C}$  for 10 min,  $900^\circ\text{C}$  for 5 min, or  $1000^\circ\text{C}$  for 2min. The electrical properties of the contacts were evaluated by the current-voltage (I-V) measurements. The specific contact resistivities were measured by the circular

transmission line model (TLM). Microstructure was analyzed by an x-ray diffraction (XRD), and the surface morphology was observed by a field emission scanning electron microscope (FE-SEM) and a stylus surface profiler.

Figure 1 shows I-V characteristics of the CoAl contacts after annealing at 800°C for 10 min. The Co contact without Al shows Schottky behavior and the contact resistance is extremely large. The CoAl contact with 10 nm or 40 nm Al layer shows Ohmic I-V behavior. However, the contact with 120 nm Al layer shows leaky rectifying behavior. After annealing at 900°C for 5 min, the I-V behaviors of the contacts with 10 nm or 120 nm Al layer changed to non-Ohmic and Ohmic behavior, respectively. After annealing at 1000°C for 2 min, both the contacts with 40 nm and 120 nm Al layer show the Ohmic behavior.

Figure 2 shows dependence of the specific contact resistivities of the CoAl contacts on the annealing temperature. The  $\rho_c$  values of the samples with 40 nm and 120 nm Al layers decrease with increase in annealing temperature. The minimum  $\rho_c$  value of  $4 \times 10^{-4} \Omega\text{-cm}^2$  is obtained for the contact with 40 nm Al layer after annealing at temperatures higher than 900°C. The spread of the measured  $\rho_c$  values for the CoAl contacts was much smaller than that of the TiAl contact. In addition, the surface morphology of the CoAl Ohmic contact was very smooth compared with that of the TiAl Ohmic contact even after annealing at 1000°C.

In summary, the CoAl Ohmic contacts with the smooth surface and the contact resistivity as low as  $10^{-4} \Omega\text{-cm}^2$  were obtained after annealing at 900°C. The annealing temperature and the amounts of Al added to the CoAl Ohmic contact were lower than those prepared for the TiAl Ohmic contact.

[Ref.1] N. Lundberg, *et al.*, Solid-State Electron. **39**, 1559 (1996).

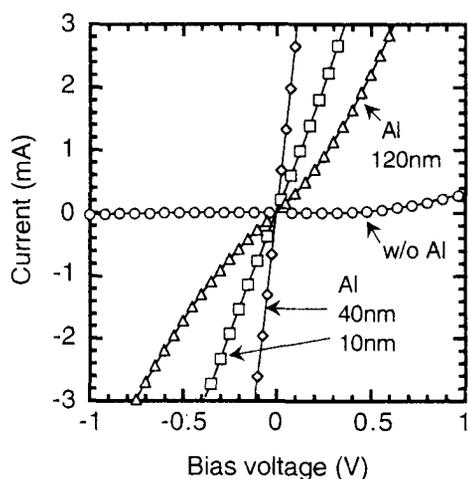


Fig. 1. The current-voltage characteristics of CoAl contacts after annealing at 800°C.

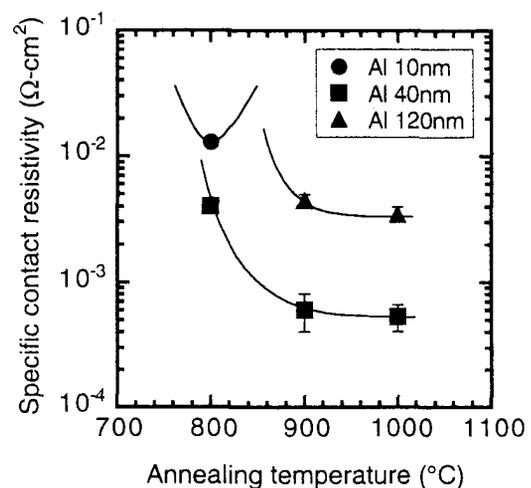


Fig. 2. The annealing temperature dependence of the specific contact resistivity of the CoAl contacts.

## Effect of the temperature treatment on Au/Pd Schottky contact to 4H-SiC

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The excellent electrical and thermal properties of 4H-SiC, such as a high breakdown field, a high electron mobility, a high electron saturation velocity and high thermal conductivity make it a preferable semiconductor material for high-power Schottky rectifiers. The efficiency of these devices depends on the barrier behaviour at high operating temperatures. For that reason the good electrical characteristics of metal/SiC contacts with their thermal stability and reliability are very important for the device performance.

Different metals (Ni, Ti, Au, Pt) have been reported as Schottky contacts in 4H-SiC diodes [1-3]. The metal used as a Schottky contact in the rectifiers should combine a low resistivity and high thermal conductivity with a not very large barrier height (about 1-1.3 eV). The latter is necessary to reduce the power loss in the operating device [4].

In the present work we propose and study for the first time Pd as a suitable metal for Schottky contact to n-type 4H-SiC. The wafers used for Schottky contact formation consisted of n-type 4H-SiC layers grown by sublimation epitaxy on the Si-face of commercial n-type, approximately  $(7-10) \times 10^{18} \text{ cm}^{-3}$ , 4H-SiC substrates. The growth was performed in a high purity graphite crucible at temperatures between 1600°C and 1800°C and base pressure of either  $1.5 \times 10^{-5}$  or  $4.5 \times 10^{-6}$  torr. Due to the specifics of the sublimation epitaxy process the layers contain Al, B, and N as typical residual impurities, resulting in compensated material. Epilayers with two carrier concentrations,  $2 \times 10^{16} \text{ cm}^{-3}$  and  $8 \times 10^{16} \text{ cm}^{-3}$ , were utilised in this study. They were cleaned using a standard cleaning procedure in organic solvents and etching. Prior to the metal deposition the surface was cleaned in Ar discharge. The deposition of all metals was performed by electron-beam evaporation in vacuum of  $1 \times 10^{-6}$  torr. The low resistance ohmic contact was formed to n-SiC substrate. It included 100 nm thick Ni annealed at 950 °C. After annealing Ti/Au (100 nm/100nm) layers were evaporated subsequently. The Schottky contact consisted of consecutively evaporated Pd (100nm) / Au (80nm) layers. The upper Au layer was deposited to protect Pd during the thermal treatments. The contact pads in a diameter of 0.6 mm were formed using shadow mask. The samples investigated have a vertical configuration. The Schottky contact was annealed in a resistance furnace in an argon atmosphere for 5 min at temperatures ranged from 200 °C to 600 °C.

The Schottky barrier was electrically characterized by I-V and C-V characteristics. The barrier height and the ideality factor have been determined from the I-V characteristics measured on the as-deposited samples and after annealing at each temperature in the interval investigated (Fig.1). The results showed that the annealing temperature increase caused a slight increase of the barrier height up to 500 °C. The following annealing at 600 °C did not change it (Fig.2). More pronounced effect of the annealing temperature was observed on the ideality factor. It decreased up to 500 °C heating but further annealing at 600 °C did not

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improve it. These results determined the annealing temperature of 500 °C as a suitable for the Schottky contact formation. The barrier height was calculated to be 1.05 eV before annealing and 1.11 eV after annealing at 500 °C for the sample with the higher carrier concentration. For the same sample a barrier height of 1.2 eV has been determined from the C-V characteristics. An increase of the barrier height has been observed with the sample having a lower carrier concentration. The I-V measurement determined 1.14 eV and 1.2 eV before and after annealing respectively. The value of 1.31 eV has been measured from the C-V characteristic of the annealed sample. In order to explain the observed effect of the annealing on the barrier height an Auger analysis of the interface Au/Pd/SiC has been carried out. The obtained barrier height values correspond to the requested ones for the reduction of power loss in the Schottky diode [4]. These results as well as the high thermal conductivity (71.6 W/m-K) and the low resistivity ( $1.06 \times 10^{-5} \Omega \cdot \text{cm}$ ) of Pd illustrate that it is a suitable metal for Schottky contacts to n-type 4H-SiC. Additional experiments on thermal stability of Au/Pd/SiC Schottky contacts at high operating temperatures will also be presented.

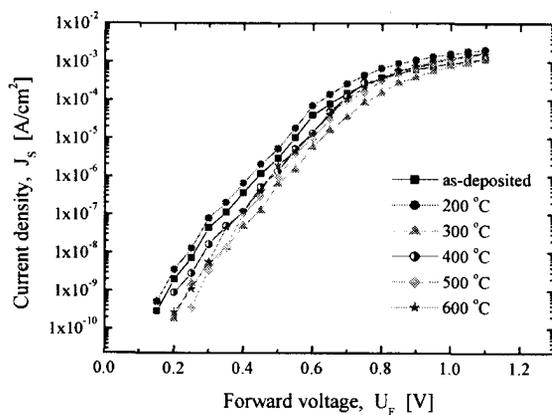


Fig.1 I-V characteristics of Au/Pd/SiC Schottky contacts after treatment at different temperatures for 5 min.

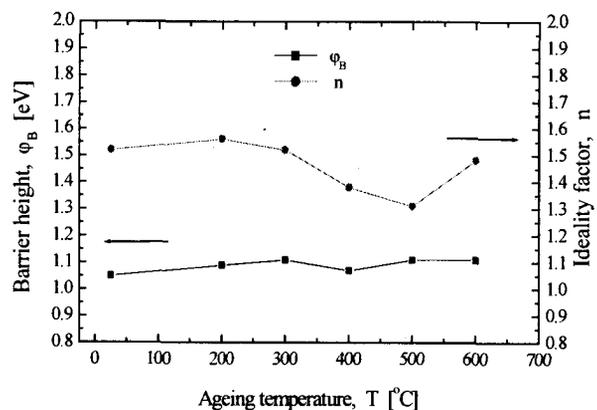


Fig.1 Values of the barrier height and the ideality factor of Au/Pd/SiC Schottky contacts after treatment at different temperatures for 5 min.

### References

1. V.Saxena, A.J.Steck, Mater.Sci.Forum, **Vol. 264-268** (1998) 937.
2. D.J.Morrison et al., Mater. Sci.and Engin., **B 61-62** (1999) 345.
3. M.Tren et al., Mater.Sci.Forum, **Vol. 353-356** (2001) 679.
4. A.Itoh et al., IEEE Electr. Device Lett., **16**, 6 (1995) 280.

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## ELECTRICAL CHARACTERISATION OF NICKEL SILICIDES CONTACTS ON SILICON CARBIDE

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Large bandgap semiconductors have been widely investigated and utilised for optoelectronic applications. However, research and commercial interest in large bandgap semiconductor and SiC electrical devices have recently increased due to the availability of high-quality SiC wafers and general advance in material fabrication techniques. SiC is a promising power semiconductor because of its large bandgap (3.0 eV for 6H and 3.2 eV for 4H) and thermal conductivity (4.9 W/cmK for 6H and 4H)<sup>1</sup>. For power applications, SiC large bandgap translate into a high electrical field and that allows device designs that have lower series resistance and lower power dissipation.<sup>2,3</sup> The great potential of SiC as a semiconductor in electronic device applications is challenged by the difficulty of controlling metal contact properties.<sup>4,5</sup> These properties of the metal/SiC interfaces include uniformity and thickness of the interfacial region, stability at high temperatures, and most importantly the Schottky Barrier Height (SBH) or the energy barrier for electrons traversing the interface. The Schottky barrier height determines the electrical behaviour of an ohmic or Schottky contact. An ohmic contact, important for making outside communication to a device, is defined as having: (a) a linear and symmetric current-voltage relationship for positive and negative voltages; and (b) negligible resistance compared with the bulk of the device. Therefore a low Schottky barrier is necessary to create a good ohmic contact. However, a large SBH is necessary to obtain a good Schottky, or rectifying contact.

In this paper we reported the specific contact resistance and Schottky barrier measurements of Ni/SiC-6H annealed in the range between 600 and 950 °C. The ternary phase diagram of this system<sup>6</sup> shows that the only stable silicide phase is the Ni<sub>2</sub>Si. This behaviour has been confirmed in a previous paper<sup>7</sup> where we have shown that the Ni<sub>2</sub>Si phase can be formed in the temperature range between 600 and 950 °C. The carbon present in the consumed silicon carbide layer precipitates in small (4 nm) clusters.

On this system several experiments have been performed to determine both the specific contact resistance and the Schottky barrier height but in these studies a simultaneous determination has not been performed in the same experimental conditions.

The specific contact resistance measurements were performed on some Transmission Line Method (TLM) structures consisting of six contact pads separated by 100 to 400 µm realised on high doped SiC substrates. The doping of the substrate was ranged between  $5 \cdot 10^{17}$  and  $7.4 \cdot 10^{18}$  cm<sup>-3</sup>. On these substrates a SiO<sub>2</sub> layer, 50 nm thick, was grown by dry oxidation at 1150 °C. The TLM structures were realised by a photolithographic process and the oxide layer was finally etched by a Reactive Ion Etch (RIE) apparatus. On these structures the Ni film was deposited and subsequently reacted at 950 °C for 60 s. After the reaction the unreacted film on the silicon oxide layer was etched by a selective etch. The self aligned TLM structures were characterised on a Wentworth probe station with a Keitley 236 and a Keitley 619.

On a n<sup>+</sup> substrate ( $N_d = 7 \cdot 10^{18}$  cm<sup>-3</sup>) an epitaxial layer 4 µm thick with a doping concentration of  $2.8 \cdot 10^{15}$  cm<sup>-3</sup> was grown by CREE Res. Inc. On these wafers a Chemical Vapour Deposited (CVD) oxide was deposited. Circular structures were opened in the oxide by a photolithographic process in the range between 100 and 240 µm diameters. Then a 200 nm Ni film was deposited, with the

previously reported parameters, and finally the metal layer was defined with a second mask to form a field plate over the oxide. These diodes were characterised in a Cascade probe station before and

after an annealing process at 600 °C for 60 s.

Several TLM structures have been prepared with the process previously described. A Ni film has been deposited and reacted with the silicon carbide substrate at 950 °C. The total resistance  $R_T$  measured between two TLM pads of width  $W$ , placed at distance  $d$ , can be written as:

$$R_T = 2R_C + (R_S/W)d \quad (1)$$

where  $R_C$  is the metal/SiC contact resistance and  $R_S$  is the sheet resistance of the SiC substrate.

By separating the two contributions of the contact and sheet resistance, the specific contact resistance  $\rho_c$  can be calculated<sup>8,9</sup>.

The data are reported in figure 1. Our data for the Ni<sub>2</sub>Si are very close to the values reported from Crofton et al.<sup>10</sup> with a similar process.

The fabrication process of the Schottky diodes was explained in the experimental section. After diodes formation, these devices were characterised by I-V, I-T and C-V measurements. From the I-V data it has been observed that the characteristics were nearly ideal ( $n=1.07$ ) and the Schottky barrier height was in the range of  $1.30 \pm 0.01$  eV.

This result was further confirmed by the I-T characteristic reported in figure 4. The Schottky barrier height was exactly the same also with this technique and the effective Richardson constant ( $A^{**}$ ) was determined to be equal to  $5.25 \text{ A}/(\text{cm}^2\text{K}^2)$ .

Low resistance ohmic contacts ( $3\text{-}4 \times 10^{-5} \Omega\text{cm}^2$ ) in n-type SiC were fabricated by performing rapid thermal annealing of Ni/SiC samples in N<sub>2</sub> at 950°C. This kind of thermal process leads to rectifying contacts for substrate carrier concentration lower than  $5 \times 10^{17} \text{ cm}^{-3}$ .

The analysis of the Schottky diodes with the Ni<sub>2</sub>Si show that this system has a Schottky barrier of 1.3 eV.

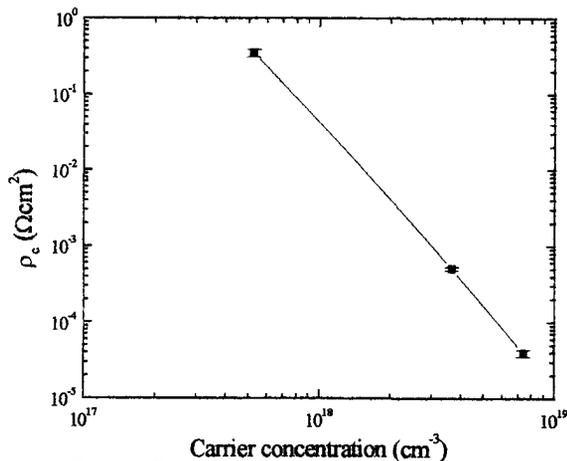


Fig. 1 - Specific contact resistance as a function of the substrate carrier concentration for Ni/SiC samples, annealed at 950°C in N<sub>2</sub> for 60s. The line connecting the points serves to guide the eye only

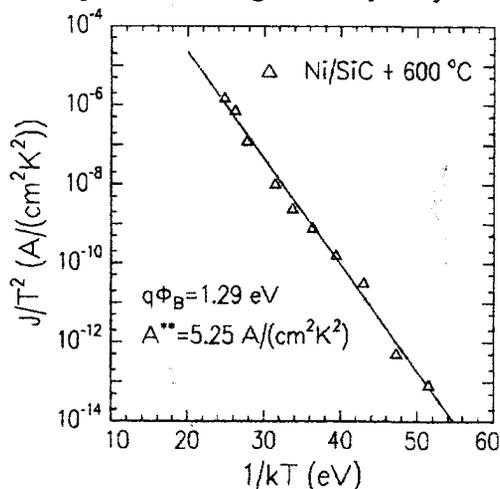


Fig. 2 - Arrhenius plot of the forward current of the Ni<sub>2</sub>Si/SiC Schottky diode. The experimental Schottky barrier height ( $q\Phi_B$ ) and the Richardson constant ( $A^{**}$ ) are indicated in the figure.

## References

- <sup>1</sup> P.G. Neudeck, J. Electron. Mater., 24, 283 (1995)
- <sup>2</sup> M. Bhatnager and B.J. Baliga, IEEE Trans. Electron Devices, 40, 645 (1993)
- <sup>3</sup> B.J. Baliga, IEEE Trans. Electron Devices 43, 1732 (1996)
- <sup>4</sup> L.M. Porter, R.F. Davis, Material Science and Engineering B34, 83 (1995)
- <sup>5</sup> J. Crofton, L.M. Porter and J.R. Williams, Phys. Sta. Sol. (b) 202, 581 (1997)
- <sup>6</sup> R. Schiepers, "The interaction of SiC with Fe, Ni and their alloys", Thesis presented to the Eindhoven University of Technology
- <sup>7</sup> F. La Via, F. Roccaforte, V. Raineri, P. Musumeci, L. Calcagno, Microelectronics Engineering, in press.
- <sup>8</sup> G. K. Reeves, H.B. Harrison, IEEE Electron Device Lett. Vol 3 n.5, 111 (1982)
- <sup>9</sup> H.H. Berger, Solid-St. Electron. 15, 145 (1972)
- <sup>10</sup> J. Crofton, P.G. McMullin, J.R. Williams and M.J. Bozack, J. Appl. Phys. 77(3), 1317 (1995)

## Characteristics of Schottky diodes on 6H-SiC surfaces after sacrificial anodic oxidation

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With extensive investigation for 6H-SiC device processes, commercial electronic devices are supposed to be realized soon. However, there are some difficulties in the processes. One of the difficulties is slow thermal oxidation rate of 6H-SiC, especially at (0001) Si face.<sup>1)</sup> This slow rate makes oxidation process time-consuming. In this work, we tried to perform anodic oxidation as a sacrificial oxidation process before contact formation. It has a great advantage that the anodic oxidation can be performed at room temperature.

n-type 6H-SiC samples with a net donor concentration of  $10^{18} \text{ cm}^{-3}$  were oxidized by applying voltage with a constant current of  $1 \text{ mA/cm}^2$  in an electrolyte, which is a mixed solution of ethylene-glycol, water and  $\text{KNO}_3$ , for 4, 20 and 100 min. Then the oxide films were etched by HF. The Au and Ni were evaporated as Schottky contacts on the oxidized-etched surface, and Al contacts were also formed as ohmic contacts without annealing. As references, the metals were also evaporated on an as-received surface and a sacrificial thermal-oxidized-etched surface. Before the evaporation, each sample was dipped in HF and boiling water. We measured I-V and C-V characteristics for the Schottky contacts and evaluated contact resistances for Al ohmic contacts by the 4-point-pattern method.

Figure 1 shows the I-V characteristics for the Ni Schottky contacts on each surface. The Ni contacts on the as-received surface have an average ideality factor  $n$  of 1.1. The Ni contacts on the surfaces after sacrificial anodic oxidation show ideality factors  $n$  scattered within 1.1–1.4, and the Ni contacts on the surface after sacrificial thermal oxidation show  $n$  of about 1.1. The barrier heights  $\phi_{I,V}$  obtained from I-V curves are 0.95 V for the as-received surface and 1.0–1.3 V for both oxidized-etched surfaces. The estimation of  $\phi_{I,V}$  is somewhat unreliable due to deviation of  $n$  value from 1, but barrier heights measured from C-V characteristics  $\phi_{C,V}$  show the same trend as  $\phi_{I,V}$ . The leakage current densities at a reverse bias of 20 V are of the order of  $10^2 \text{ A/cm}^2$ .

Figure 2 shows the I-V characteristics for the Au Schottky contacts on each surface. The  $n$  values for the Au contacts are larger than that for Ni contacts, in a range of 1.2–1.8. The  $\phi_{I,V}$  for the Au contact on the as-received surface shows the lowest value of 0.90 V as in the case for the Ni contacts, while it is within 0.98–1.3 V for both oxidized-etched surfaces. The  $\phi_{C,V}$  was also increased by the oxidation and subsequent etching. The leakage current densities at a reverse bias of 20 V are of the order of  $10^3 \text{ A/cm}^2$ , which is one order of magnitude larger than that for the Ni contacts.

Figure 3 shows contact resistances for the Al contacts on each surface. The contact

resistance is  $1\text{--}10\ \Omega\text{cm}^2$  on the as-received surface and  $10^{-2}\text{--}10^{-1}\ \Omega\text{cm}^2$  on the oxidized-etched surfaces. Thus both the anodic and thermal oxidation processes reduce the Al contact resistance by about two orders of magnitude.

The above results show that both the anodic and thermal sacrificial oxidation processes have similar effects on the properties of the metal contacts. It has been reported that sacrificial thermal oxidation removes low crystallinity layer at the SiC surface.<sup>2)</sup> The sacrificial anodic oxidation can also remove the defective layer and thus is expected to substitute for the sacrificial thermal oxidation.

- 1) A. Suzuki, H. Ashida, N. Furui, K. Mameno and H. Matsunami, *Jpn. J. Appl. Phys.*, **21** (1982) 579.
- 2) S. Hara, T. Teraji, H. Okushi and K. Kajimura, *Appl. Surf. Sci.*, **117/118** (1997) 394.

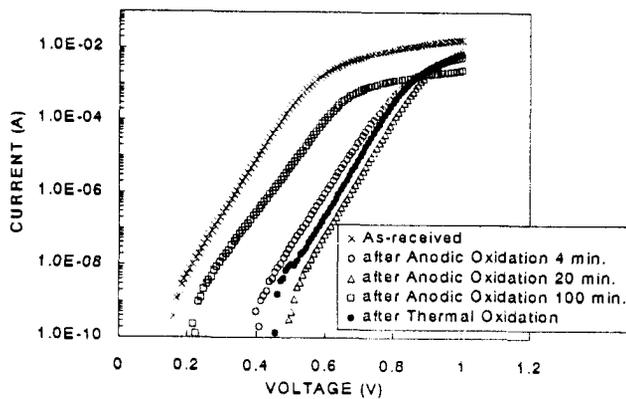


Fig. 1 I-V characteristics for Ni Schottky contacts on each surface.

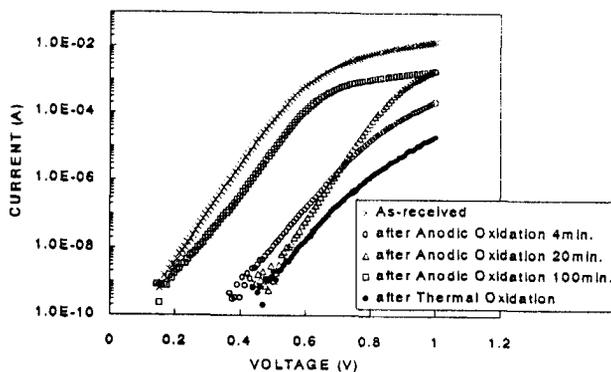


Fig. 2 I-V characteristics for Au Schottky contacts on each surface.

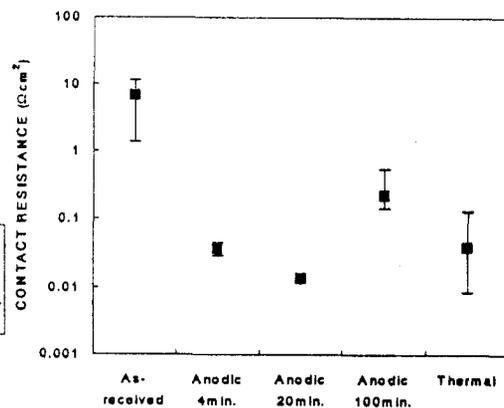


Fig. 3 Contact resistances for Al ohmic contacts on each surface.

## Electrical Properties of Graphite/n- and p-Type Homoepitaxial Diamond Contact

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One important technological requirement for diamond based electronic devices is the production of reliable ohmic contacts. Graphitization of diamond induced by ion implantation is one of the commonly used methods for realization of ohmic contacts to semiconducting diamond. The details of the electrical properties, such as specific contact resistance between graphite and diamond, have not been clarified. This research exhibits the electrical properties of the graphitic electrodes formed in n-type and p-type homoepitaxial diamond films, respectively. Sulfur-doped diamond films with sheet resistance of  $10^8 \Omega/\square$  were achieved by ion implantation in undoped homoepitaxial diamond (100) films grown by chemical vapor deposition (CVD) method. p-Type diamond films were synthesized by using trimethylboron (TMB) gas as a doping source in the CVD system. The graphitic electrode was formed by Ar<sup>+</sup> implantation with energy of 40keV and dose of  $1 \times 10^{16}/\text{cm}^2$  at room temperature. The Au/Pt/Ti layers were deposited onto the electrodes and then annealed at 700°C in Argon. The electrical properties at graphitic electrode/diamond interfaces were investigated mainly by using the current-voltage (I-V) and the capacitance-voltage (C-V) measurements. It was clearly seen that the contacts gave a linear I-V characteristic from low voltage (0V) to high voltage (1500V), indicating that these interfaces have an ohmic property. The specific contact resistance (SCR) for graphite/n-type film was characterized to be in the order of  $10^3 \Omega \cdot \text{cm}^2$ . This SCR value seems to be relatively high, but it is reasonable and enough to show the ohmic property for the present high resistive n-type diamond film. The more detailed results for n-type film as well as for p-type film will be discussed based on the electrical properties in graphite/n-type and p-type diamond films, which were characterized and compared by using linear transmission line model (TLM) and circular TLM extrapolation method (to avoid lateral current crowding effect).

## Hydrogen incorporation in SiC using plasma-hydrogenation

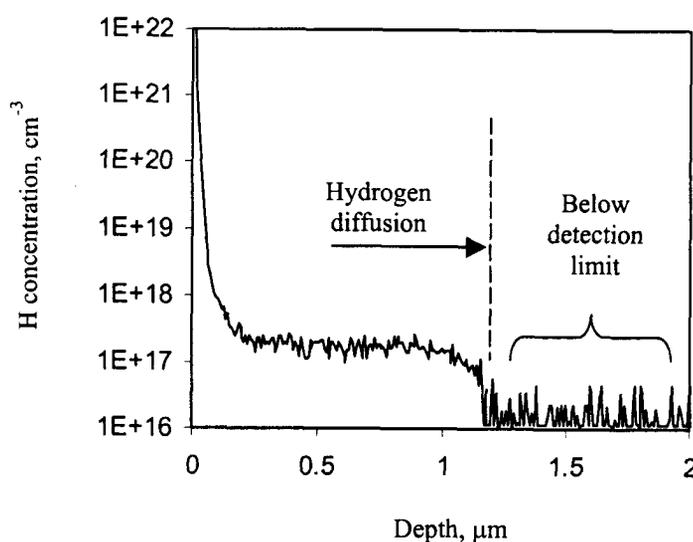
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A possibility to introduce hydrogen in SiC has been extensively investigated due to the importance of this topic for doping control during SiC device fabrication. The Ion Implantation technique was successfully used to study acceptor passivation in 4H and 6H samples [1]. A high temperature annealing in H<sub>2</sub> atmosphere was also applied to investigate passivation of nitrogen donors [2]. However, a possibility to introduce hydrogen in SiC samples by plasma hydrogenation stays an attractive alternative due to its ability to minimize surface damage inherent to the ion implantation approach as well as due to its much shorter processing times than for the case of high temperature annealing. Previous data on plasma deuteration showed a relatively shallow hydrogen penetration that could not be improved by subsequent high temperature annealing [3]. Annealing led instead to a significant reduction of the hydrogen concentration due to its outdiffusion from the samples.

It is suggested that the temperature of the plasma hydrogenation of 300°C used in Ref. 3 is not enough to stimulate a sufficient level of H diffusion that requires much higher temperatures and/or processing times [4]. In this work we investigate the role of the sample temperature during its exposure to the hydrogen plasma on the efficiency of achieving hydrogen diffusion into the bulk of SiC crystals. Hydrogenation is performed in two different systems operating in the reactive ion etching (RIE) and the Inductively Coupled Plasma (ICP) modes at different microwave powers and pressures. Results of hydrogenation in an ICP plasma (750 W and 250 W microwave power on the top and the bottom electrodes respectively, 50 mTorr pressure) for 1 hr are shown in Fig. 1. In addition to the less than 0.1 μm deep shallow region similar to that observed after plasma deuteration in Ref. 1, a rather distinct diffusion front can be observed from this SIMS profile. An efficient passivation of Al acceptors was observed in this sample by low temperature photoluminescence spectroscopy [5]. This result is different from the SIMS profile observed after performing hydrogenation in the system operating in the RIE mode at the estimated temperature of about 300°C. A denser plasma generated in the ICP system is expected to produce a higher degree of sample heating, which could be the reason for the much more significant level of hydrogen diffusion in this case.



Results of hydrogenation experiments at different powers and pressures during the hydrogenation will be reported and the role of the process conditions on the efficiency of hydrogen penetration will be discussed.

- [1] N. Ahtziger, J. Grillenberger, W. Witthuhn, M. K. Linnarson, M. Janson, and B. G. Svensson, *Appl. Phys. Lett.* **73**, (1998) 945
- [2] G. Gendron, L.M. Porter, C. Porte, and E. Bringuier, *Appl. Phys. Lett.* **67**, (1995) 1253.
- [3] J.M. Zavada, R. G. Willson, F. Ren, S.J. Pearton, and R.F. Davis, *Solid-State Electronics*, **41**(5), (1997) 677
- [4] M.K. Linnarson, M.S. Janson, S. Karlsson, A. Schöner, N. Nordell, B.G. Svensson, *Mater. Sci. and Engineer. B.* **61-62** (1999), 275
- [5] Y. Koshka, M.S. Mazzola, to be published in *Appl. Phys. Lett.*

## Investigation of group IV nanocrystals formed by ion beam processing

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250 keV Ge ions were implanted into [0001] 4H-SiC bulk crystals or epitaxial layers at room temperature and 700 °C with an ion fluence of  $10^{16} \text{ cm}^{-2}$  causing a Ge peak concentration of approximately 1at% within the projected ion range (100...110 nm). After implantation thermal annealing was carried out at temperatures up to 1600 °C in Ar atmosphere (pressure 20 kPa) for 120 s with a double graphite strip RTA apparatus. The samples were analysed by means of Rutherford Backscattering Spectrometry (RBS), Cross Sectional Transmission Electron Microscopy (XTEM) methods and X-Ray Diffraction (XRD).

Whereas after room temperature implantation the implanted layers are amorphous, amorphization is prevented at 700 °C. A defect band occurs around 100...200 nm depth, i.e. deeper than the maximum of the Ge distribution (Fig. 1, left).

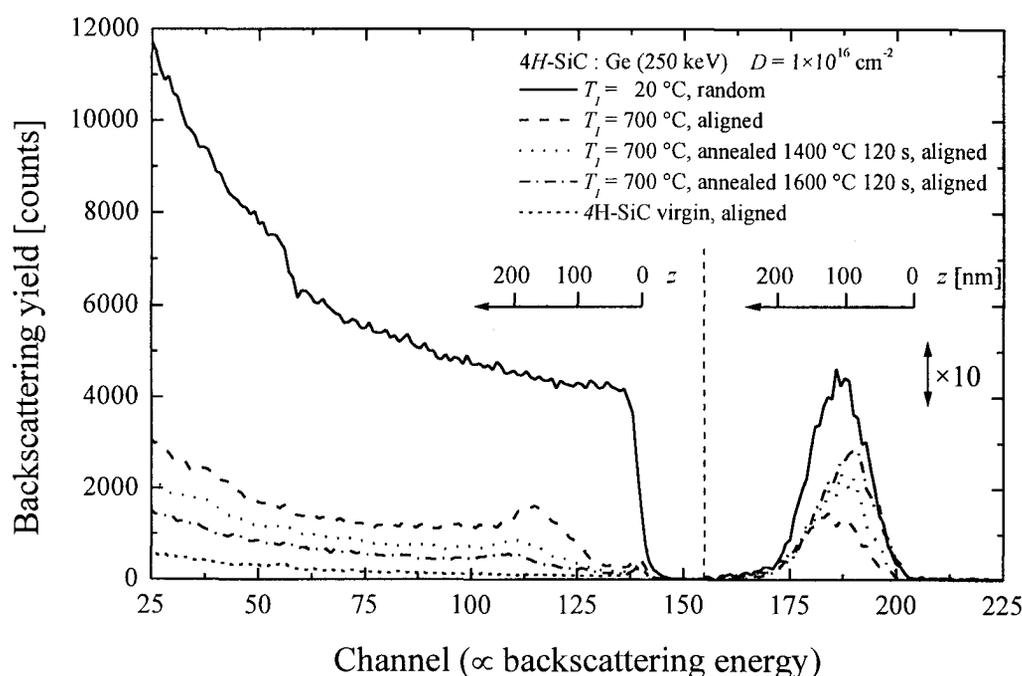
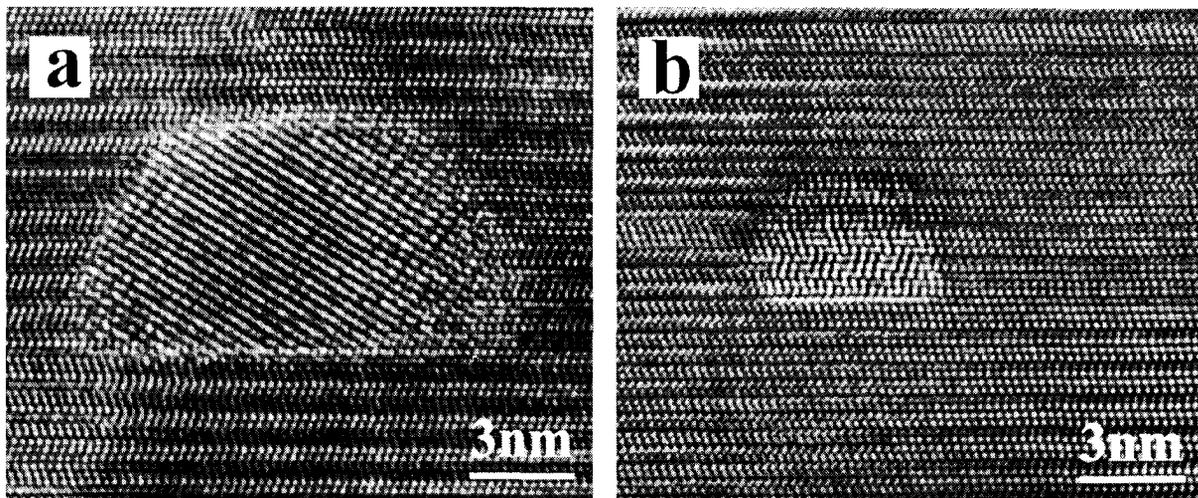


Fig. 1: RBS aligned and random spectra of a sample implanted at 700 °C and annealed 120 s at 1400 °C and 1600 °C.

The decrease of the aligned RBS yield in the energy region of backscattering on Ge atoms (Fig. 1, right) with respect to the random yield (full line) indicates that a significant part of the implanted Ge is incorporated into the SiC lattice along the [0001] direction. Annealing yields to a further decrease of the damage concentration (Fig. 1, left) and an increase of the Ge content visible by the ion beam (Fig. 1, right) mainly in the near-surface region. This can be explained by the formation of Ge precipitates within the SiC lattice leading to an enhanced ion backscattering. By means of a special Z-contrast method (STEM-HAADF) in the same depth region Ge clusters with lateral dimensions between 2 nm and 12 nm were detected (not shown). High-resolution TEM identifies these clusters as Ge-rich cubic nanocrystals containing stacking faults (Fig. 2).



*Fig. 2: HRTEM images of different Ge-rich nanocrystals formed after annealing at 1600°C (viewed along [11-20]-direction of the 4H-SiC matrix).*

The nanocrystals in most cases are not aligned with major SiC crystallographic directions which explains the increase of the RBS yield with respect to the as implanted case (Fig. 1). The existence of Ge-rich or Ge nanocrystals in Ge-implanted and annealed 4H-SiC layers is also confirmed by XRD analysis (not shown). The observed shift of the 111Ge reflection towards the value of crystalline Si may be the consequence of internal strain in the crystallites or be due to crystallites consisting of a mixture of Si and Ge.

The results show that Ge implantation into SiC in combination with subsequent annealing leads to the formation of Ge-rich nanocrystals.

Further investigations will be directed to the control of distribution, size and composition of the nanocrystals.

## Recent progress in the preparation of a-Si<sub>1-x</sub>C<sub>x</sub>:H by thermal evaporation in Glow Discharge Decomposition of Methane

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### ABSTRACT

Hydrogenated amorphous silicon carbide a-Si<sub>1-x</sub>C<sub>x</sub>:H films have been prepared successfully by thermal evaporation of silicon in an environment of glow discharge (G.D) decomposition of methane. The optimum conditions have been developed for the preparation of near stoichiometric thin films of a-Si<sub>1-x</sub>C<sub>x</sub>:H. The optimum conditions are, pressure of methane P<sub>CH<sub>4</sub></sub> = 5mbar, rate of deposition r<sub>d</sub> = 0.5 nm.s<sup>-1</sup>, substrate temperature T<sub>s</sub> = 473K. G.D technique was used to produce carbon and hydrogen atoms to be mixed and embedded in the silicon films using capacitance technique at 18 cm distance within residual methane gas. The amorphous structure of the as-deposited and the annealed a-Si<sub>1-x</sub>C<sub>x</sub>:H thin films have been determined using X-ray diffraction (XRD), while the influence of hydrogenation on these a-Si<sub>1-x</sub>C<sub>x</sub>:H films have been studied using infrared IR absorption spectroscopy to confirm the hydrogen bonding of a-SiC:H, CH and a-Si:H as well as a-Si-C bond.

The silicon content has been determined by atomic absorption spectrophotometer. The dependence of film structure and composition on the preparation condition was studied. The homogeneity of the films and the thickness have been examined by scanning electron microscopy SEM analysis. The optical band gap was found to increase up to 2.5 eV with increasing time of G.D (up to 60 min) decomposition of methane CH<sub>4</sub> using the capacitance technique with d.c biasing voltage = 20V. while it decreases down to 2.25eV for G.D time of 90 min.

The optical energy gap E<sub>g</sub><sup>opt</sup> has increased up to 2.48eV with increasing silicon content up to 60% with d.c biasing voltage but with a.c biasing voltage, E<sub>g</sub><sup>opt</sup> has decreased to its lowest value at 60 cubic centimeter per minute (ccm/min) as flow rate of methane, albeit we found that E<sub>g</sub><sup>opt</sup> increases with increasing annealing temperature T<sub>a</sub>. The carbon content was found to increase with increasing flow rate of methane. However the absorption edge has shifted to higher energies with increasing T<sub>a</sub>. The band width (Urbach band tails) was observed to decrease with increasing T<sub>s</sub>, albeit it shifted to higher values with increasing silicon content. The refractive index (n) and the real part of dielectric constant (ε<sub>1</sub>) were found to decrease with increasing wavelength while it decreases with increasing silicon content at λ = 780nm. The extinction coefficient (k') and the imaginary part of dielectric constant (ε<sub>2</sub>) decrease with increasing wavelength. The D.C conductivity (σ<sub>d.c</sub>) of a-Si<sub>1-x</sub>C<sub>x</sub>:H thin film was characterized by 3 transport mechanisms. The thermoelectric power and Hall effect at T<sub>a</sub> = 303K exhibit p-type for a-Si<sub>1-x</sub>C<sub>x</sub>:H thin film and then converted to n-type with increasing T<sub>a</sub> up to 473K. Hall mobility μ<sub>H</sub> of a-Si<sub>51</sub>C<sub>49</sub>:H increases methane up to 1113 cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> with increasing flow rate up to 60ccm/min and it decreased with time of G.D and also decreases with

increasing ( $T_a$ ). Hall carrier concentration ( $n_H$ ) is observed to decrease down to  $2.5 \times 10^{14} \text{ cm}^{-3}$  with increasing flow rate of methane up to 60ccm/min, and then increases above that rate. However it increased with increasing time of G.D and then started to decrease down to  $9.3 \times 10^{14} \text{ cm}^{-3}$ . on the other hand  $n_H$  has increased with increasing  $T_a$  up to 373K and then decreasing taking value of  $7.13 \times 10^{14} \text{ cm}^{-3}$ . A.C. conductivity [ $\sigma(\omega)$ ] of a-Si<sub>1-x</sub>C<sub>x</sub>:H films at  $T_a=473\text{K}$  was measured in the frequency range (100Hz — 10MHz) and at the annealing temperature range (305 - 453)K. The result is discussed in terms of the quantum mechanical tunneling QMT model of conduction,  $\sigma(\omega)$  at  $f = 100 \text{ KHz}$  increasing with increasing  $T_a$  up to  $4.2 \times 10^{-6} \Omega^{-1}.\text{cm}^{-1}$  at  $T_a = 473\text{K}$  and then  $\sigma(\omega)$  decreases with increasing silicon content down to  $1.3 \times 10^{-6} \Omega^{-1}.\text{cm}^{-1}$  at 40 at % Si and then increasing to  $2.3 \times 10^{-6} \Omega^{-1}.\text{cm}^{-1}$  at 50 at % Si.

### A Novel Technology for the Formation of a Very Small Bevel Angle for High Electric Field Edge Termination

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The edge termination is an indispensable technology to achieve the bulk avalanche breakdown. Of numerous edge termination technologies, the positive bevel edge termination is most desired because it is the only approach being able to achieve the ideal avalanche breakdown. Besides, the drastically reduced surface electric field in a positive bevel edge terminated structure is expected to improve the device reliability. In this report, we present a technology that can form a beveled edge termination with a very low bevel angle. 4H-SiC diodes terminated by a 2° positive bevel fabricated with this technology are also presented.

In this method, a thick photo-resist (PR) is first spun on the sample. After exposure and development, a short time hot plate baking is conducted. The baking temperature and time are adjusted to control the shape of the PR pattern until the desired shape is achieved. The PR is hardened after baking. Since etching rate of semiconductor is much lower than that of PR, a mesa with a small bevel angle can be achieved using edge beveled PR pattern as the etching mask for inductively coupled plasma (ICP) etching. Figure 1 (a) shows the top view of the patterned PR before hot plate baking. The dimensions of the pattern are 130µm x 130µm. The inset is the thickness profile of the PR pattern. The thickness of the PR is 10µm. Figure 1 (b) shows the pattern after 160°C 10-second hot plate baking. The asymmetric bright pattern in Fig.1 (b) is caused by lighting and shading effect. The actual shape of PR after baking is symmetric. The thickness profile is shown in the inset. The PR at the edge shrinks to the center after baking, resulting in a beveled edge with a bevel angle of 20°. After 10 minutes ICP etching by the O<sub>2</sub>/CF<sub>4</sub> plasma with a bias of 50V and a power of 700W, a beveled mesa with a depth of 0.9µm and a bevel angle of 2° is achieved. Figure 1 (c) shows the top view of the resulting beveled mesa after removing the PR. The inset is the thickness profile of the mesa. The

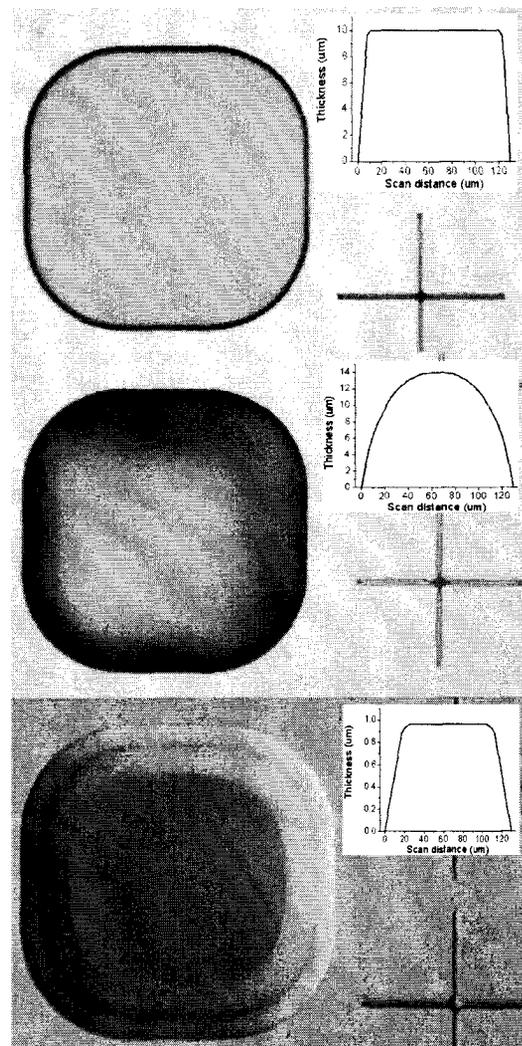


Fig.1: Thick PR pattern (a) before baking, (b) after a 160°C 10 second baking, (c) beveled mesa on 4H-SiC. Insets are thickness profiles

surface roughness of the bevel edge has been checked under SEM with 3000X magnification. No visible surface roughness has been observed.

The successful fabrication of very small bevel angle has been applied to the fabrication of 4H-SiC diodes on a wafer with SIMS profile shown in Fig.2. The wafer has a  $p^+pn$  structure grown on  $n^+$  substrate. The doping concentration and thickness of the  $p^+$ ,  $p$ , and  $n$  are  $4 \times 10^{19}/\text{cm}^3$  and  $0.1 \mu\text{m}$ ,  $2 \times 10^{18}/\text{cm}^3$  and  $0.2 \mu\text{m}$ , and  $3 \times 10^{18}/\text{cm}^3$  and  $2 \mu\text{m}$ , respectively, with varied doping densities between  $p^+$  and  $p$ , and  $p$  and  $n$ . Consider the varied low doping near the pn junction and the doping of the  $p$  layer being lower than the  $n$  layer, the resulting diodes have a positive bevel edge termination.

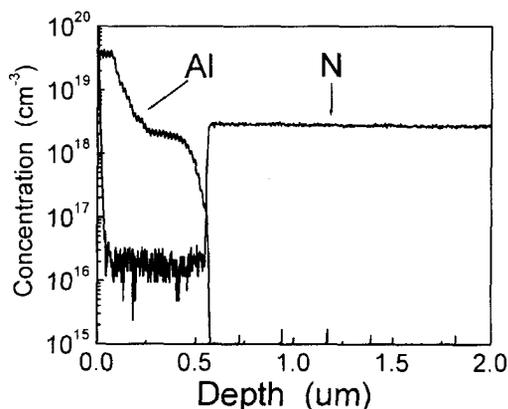


Fig.2: SIMS profile of 4H-SiC wafer

Figure 3 shows the reverse I-V characteristics of a fabricated 4H-SiC diode with  $300 \mu\text{m}$  diameter. Tests have been done at room temperature (RT),  $100^\circ\text{C}$ , and  $150^\circ\text{C}$ . The leakage current at 95% breakdown voltage is about  $1 \times 10^{-5} \text{ A/cm}^2$  at RT and  $1 \times 10^{-4} \text{ A/cm}^2$  at  $150^\circ\text{C}$ . This is comparable to the leakage current of avalanche photodiodes (APDs) with  $\text{SiO}_2$  passivation and multiple-step junction termination extension.<sup>1</sup> The diode runs very stably in deep avalanche at temperatures up to  $150^\circ\text{C}$ . Note that there is no passivation layer protecting the edge of this diode. As shown in the inset, the breakdown voltage increases as the temperature increases, suggesting a positive temperature dependence of the breakdown voltage. The breakdown voltage at RT at  $0.1 \text{ A/cm}^2$  is 63V.

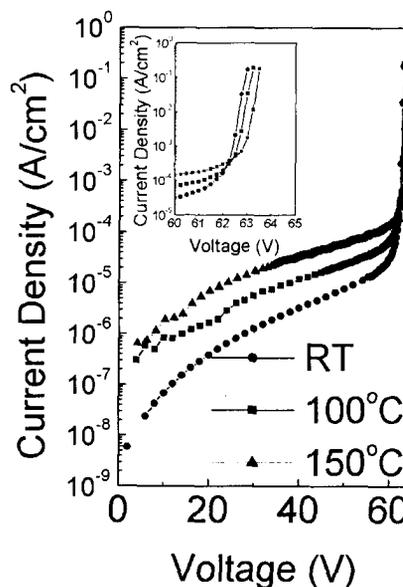


Fig.3: Reverse I-V characteristics of a  $300 \mu\text{m}$  diode terminated by a  $2^\circ$  positive bevel. The inset shows the details of breakdown at different temperatures.

#### Reference:

1. F. Yan, Y. Luo, J. H. Zhao, M. Bush, G. H. Olsen, and M. Weiner, submitted to IEE Electronics Letters.

## **Thermal analysis of GaN-based HFET devices Using the Unit Thermal Profile Approach**

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GaN-based electronic devices have been demonstrated to be ideal for high power and high frequency applications. It is primary due to a two-dimensional electron gas (2DEG) generated in the AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure. The 2DEG with a high mobility also permits low resistances and low noise performance not possible with SiC devices. However, GaN-based devices fabricated on the sapphire substrate are known to suffer from the serious heating effect due to the poor thermal conductivity. The thermal analysis for the GaN-based devices has been increasingly important since the heat dissipation can degrade the DC and the RF performance of devices, in particular during the high power operation. This study was motivated by the need for an accurate modeling tool for the prediction of device design to minimize the thermal effect and to optimize the device performance. This paper focuses on thermal analysis of particularly in AlGa<sub>N</sub>/Ga<sub>N</sub> Heterostructure Field-Effect-Transistors (HFETs). To simulate thermal profile of device surface, approximate solution was employed. Typical geometry for modeling devices is the rectangular structure consisting of multiple layers of different materials with a rectangular heat source and the infinite double Fourier series is the solution. In our simulation, a circular embedded source was adapted instead of square heat source. Approximation of circular heat source was demonstrated as accurate as square heat source solution. Appropriate physical material parameters and structural parameters of device were implemented in the simulation. Figure 1 shows the simulated device structure. The thermal distributions around the gate of the device are shown in Figure 2 (a) and (b). It was shown that the peak temperature for the device using the sapphire as a

substrate reaches to about 280 °C with the input power of 1.5 Watts. The peak temperature when using the SiC as the substrate was calculated to be about 140 °C for the same input power. It was shown that the results of simulation match well with the experimental data. We expect that our thermal simulation lead to optimization of device performance and revised device fabrication is in progress with consideration of our thermal simulation.

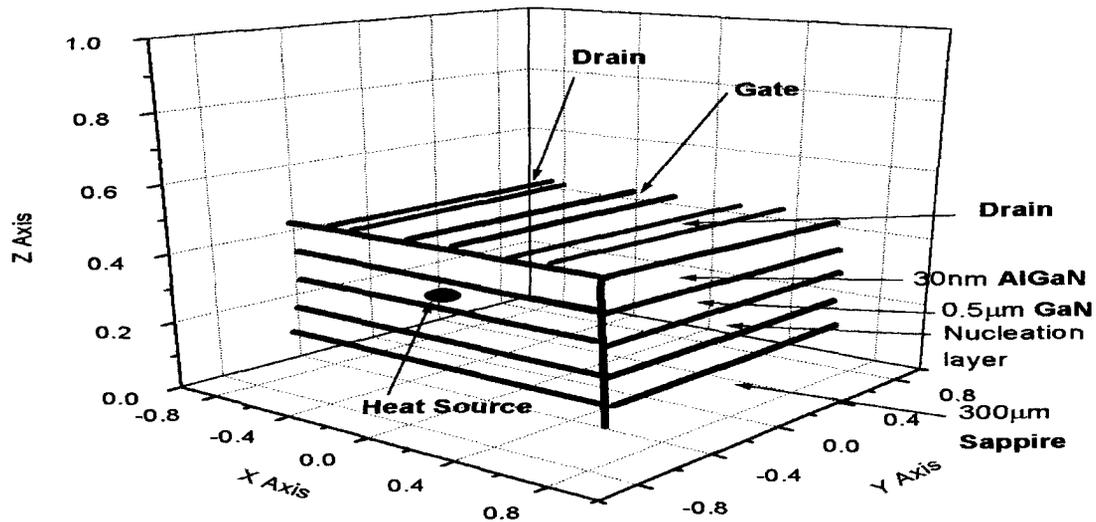


Figure 1 . The schematic simulated structure of the AlGaIn/GaN HFET. Embedded circular heat source was placed under the AlGaIn layer. The drawing is not in scale.

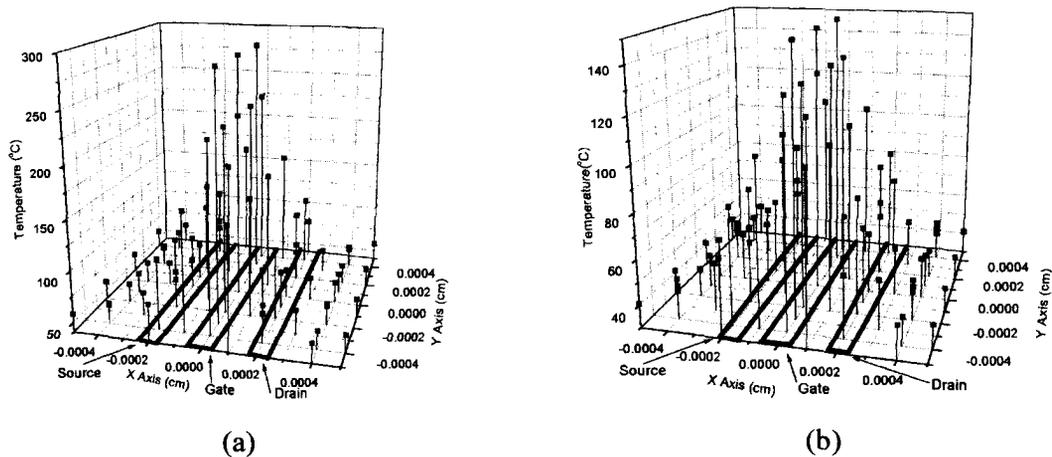


Figure 2. Temperature distribution around the gate of the AlGaIn/GaN HFET using a) the Sappire substrate (thermal conductivity of 0.28 W/cm K) and b) SiC substrate (4.9 W/cm K). The gate width and length are 200 µm and 0.8 µm, respectively. The peak temperatures are about 285 °C (a) and 145 °C (b), respectively around the gate electrode.

### Acknowledgment

Financial support for the second and the third group of authors are from the Ministry of Commerce, Industry, and Energy (# 990-02-03) in Korea.

## Hole resonant tunneling through SiC/Si-dot/SiC heterostructures

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Si-based resonant tunneling diodes (RTDs) are of great interest for applications to high-speed electronic devices and have been studied using various material systems such as Si/Si<sub>1-x</sub>Ge<sub>x</sub> [1,2], Si/CaF<sub>2</sub> [3], Si/SiO<sub>2</sub> [4]. However, the peak-to-valley current ratio is still low comparing with the GaAs-based RTDs and no room-temperature operations have been reported.

Among the many polytypes of silicon carbide (SiC), cubic 3C-SiC is a wide gap (2.2 eV) semiconductor and can be epitaxially grown on Si substrates. Since 3C-SiC/Si(100) has a wider valence band offset ( $\Delta E_V \sim 0.5$  eV) than that of Si<sub>1-x</sub>Ge<sub>x</sub>, 3C-SiC is attractive for the hole barrier in RTD structures. Previously, we have investigated the 3C-SiC/Si multilayer growth by supersonic free jet CVD and found that Si islands were formed on the SiC films at the initial growth stage [5]. Recently, we have reported the formation of SiC/Si-dot/SiC heterostructures on  $n^+$ -Si(100) and observed the current peaks and negative differential resistance due to the electron resonant tunneling from the dot structures [6]. In this study, we have grown the SiC/Si-dot/SiC heterostructures on  $p^+$ -Si(100) substrates and the current-voltage ( $I$ - $V$ ) characteristics were measured at room temperature by atomic force microscopy (AFM) with a gold-coated conductive tip.

The SiC films and Si-dots were grown by CH<sub>3</sub>SiH<sub>3</sub> and Si<sub>3</sub>H<sub>8</sub> free jets, respectively. The substrate temperature was set at 850 °C for SiC and 700 °C for the Si-dot growths. Figure 1 shows the AFM image of the sample obtained by the 1000 pulses of CH<sub>3</sub>SiH<sub>3</sub>/Si<sub>3</sub>H<sub>8</sub>/CH<sub>3</sub>SiH<sub>3</sub> jets onto  $p^+$ -Si(100). The thickness of SiC films was estimated to be  $\sim 3$  nm in this growth condition. The diameter and the height of the dots were typically  $\sim 10$  nm and  $\leq 5$  nm, respectively. Figure 2 shows the  $I$ - $V$  characteristics obtained from AFM tip on the dot in Fig. 1. The current peaks and negative differential resistance were observed at -1.7 V. Based on the Si-dot height estimated to be 4 nm from AFM line profile analysis, we calculated the hole confinement energy levels. The obtained peak may be due to the resonant tunneling between the hole confinement energy level in the quantum well and the Fermi level of the emitter as illustrated in the inset of Fig. 2.

[1] H. C. Liu, D. Landheer, M. Buchanan, and D. C. Houghton, Appl. Phys. Lett. **52**, 1809 (1988).

[2] K. Ismail, B. S. Meyerson, and P. J. Wang, Appl. Phys. Lett. **59**, 973 (1991).

[3] M. Tsutsui, M. Watanabe, and M. Asada, Jpn. J. Appl. Phys. **38**, L920 (1999).

[4] K. Yuki, Y. Hirai, K. Morimoto, K. Morita, and T. Uenoyama, J. Vac. Sci. Technol B **14**, 4068 (1996).

[5] Y. Ikoma, T. Endo, T. Tada, F. Watanabe, and T. Motooka, *Materials Science Forum* **338-342**, 265 (2000).

[6] Y. Ikoma, T. Tada, K. Uchiyama, F. Watanabe, and T. Motooka, *Solid State Phenomena* **78-79**, 157 (2001).

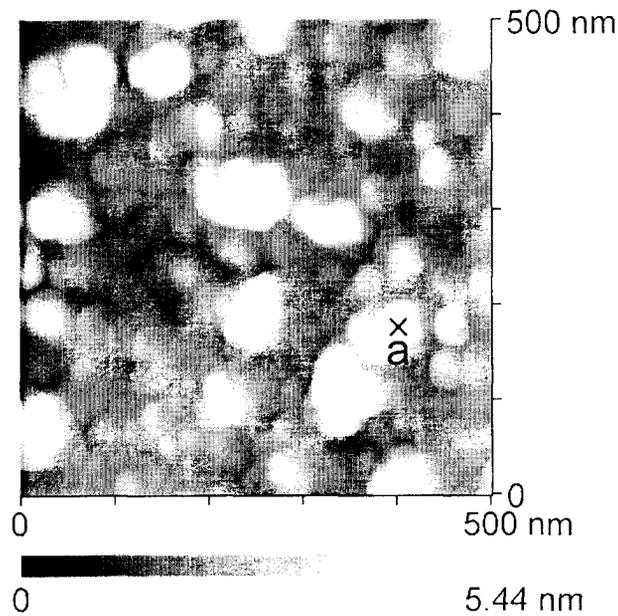


Fig. 1. AFM image of SiC/Si-dot/SiC/Si(100) surface morphology which was grown by 1000 pulses of  $\text{CH}_3\text{SiH}_3/\text{Si}_3\text{H}_8/\text{CH}_3\text{SiH}_3$  free jets.

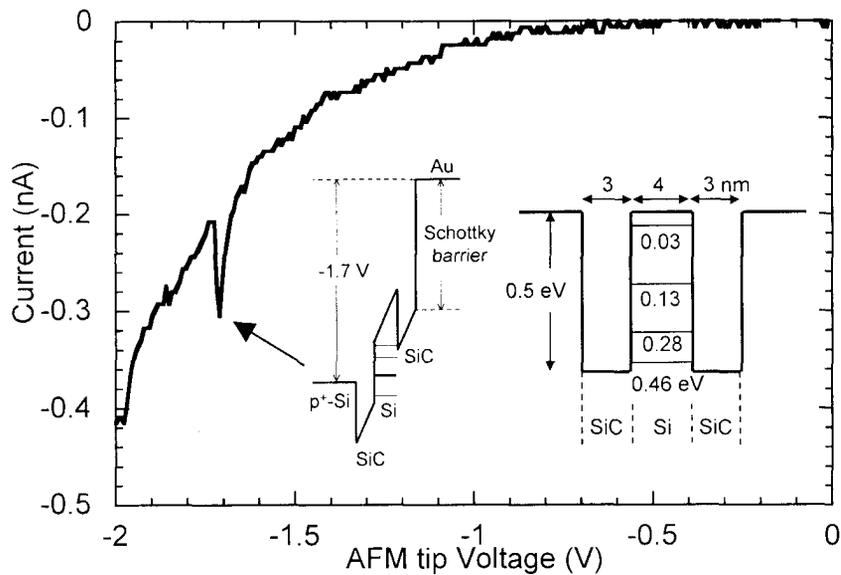


Fig. 2.  $I$ - $V$  characteristics obtained from the point a in Fig. 1. together with calculated hole confinement energy levels.

### Simulation of 5 kV Asymmetrical 4H-SiC Thyristor as Main Switches in EML Application and Study of its Junction Edge Termination

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The feasibility of using silicon power thyristor for Electric gun pulser has been established [1]. But a series array of a large number of devices is needed to achieve the required performance. The resulting size and weight of the pulser is non-optimal. The material properties of silicon carbide (SiC) indicate the potential of reducing the size and the power losses of the power devices [2]. This paper investigates the design and the performance of a 5 kV Asymmetrical 4H-SiC Thyristor as main switch in ElectroMagnetic Launching applications (EML). Based on the simulation results, an evaluation of 4H-SiC Thyristor is carried out with regard to electrothermal effect. A two-dimensional (2D) finite element simulation package ISE is used [3]. The ISE simulator first have allowed to estimate the maximum breakdown voltage for different thickness and doping level of an ideal plane parallel junction by using impact ionization coefficients given by Konstantinov [4]. Using these results (Fig. 1), a 35  $\mu\text{m}$  epitaxial layer doped at  $10^{15} \text{ cm}^{-3}$  for the blocking layer of the thyristor should give a theoretical forward blocking voltage of 5700 V. Figure 2 shows the simulated structure where all parameters are indicated. We obtain  $V_F = 6\text{V}$  for  $1800 \text{ A/cm}^2$  at 600 K.

As the periphery protection is an important issue in the design of SiC power devices, several techniques, such as MESA, Junction Termination Extension (JTE) and Epitaxial Guard Rings (EGR<sub>s</sub>) have been studied. The optimal breakdown voltage for each technique will be presented. The study of the MESA shows that the best configuration is for a vertical etch that reaches the P buffer layer. The JTE is realised by forming at the peripheral of the device an N-type region in the P-type blocking layer by ion-implantation of nitrogen. For this region which spread in 150  $\mu\text{m}$  at the peripheral, several couple of doping level and thickness of the JTE give the optimal breakdown voltage but the condition is to keep a dose of  $9.10^{12} \text{ cm}^{-2}$  of nitrogen (Fig. 3)

Another periphery protection, so called EGR<sub>s</sub>, consist to etch the N-type epitaxial layer to form guard rings. The optimal design is obtained with 5 rings, the space between the rings is 2  $\mu\text{m}$ , the ring width is 12  $\mu\text{m}$  and the etch depth is 2.1  $\mu\text{m}$  (Fig.4).

Futhermore we report on the simulation of the finite element thyristor inserted in the circuit application, shown in the figure 5, where the other component are Spice's model defined. The typical current for an Electromagnetic Launching application, is formed by the inductance L ( $L=30 \mu\text{H}$ ) and the capacitance C ( $C=865 \mu\text{F}$ ). Diodes are used as a crowbar switch. The schedule of condition imposed a thyristor able to switch a current pulse superior to 20 kA. We have then studied the minimal area of the thyristor that allows to obtain those current peak by considering the evolution of the temperature inside the structure due to the self heating (Fig. 6). The initial voltage at the capacitor is 5 kV. When the thyristor is switched-on the pulse current in the load (L and R in series) takes place. The figure 5 represents this pulse current waveform for an area structure of  $20 \text{ cm}^2$ . The current rate is  $di/dt = 160 \text{ A}/\mu\text{s}$ , the maximum switching current is 25.7 kA and the drop voltage is only 5,5 V. By decreasing the area down to  $1.5 \text{ cm}^2$ , the maximum current is only reduced to 25.5 kA and  $V_F = 35 \text{ V}$ . the self heating in the structure increase the maximum temperature up to 700 K. The realisation of this device is on the way and the design has taken into account the simulation results.

## References

- [1] E. Spahn, G. Buderer, J. Wey, V. Wegner, F. Jamet, "the use of thyristors as main switches in EML application," IEEE Trans. on Magnetics, Vol. 29, no. 1, pp. 1060-1065, Jan. 1993
- [2] B. J. Baliga, "Trends in power semiconductor devices," IEEE Trans. Electron Devices, Vol. 43, pp.1717-1731, Oct. 1996.
- [3] ISE Integrated Systems Engineering AG, Zurich/CH(1998)
- [4] A. O. Konstantinov, "Ionization rates and critical field in 4H-SiC, Appl. Phys. Lett. Vol.71, no.1, pp. 90-92.

Figure 1 : Breakdown voltage for a plane parallel junction versus thickness and doping level of the blocking layer

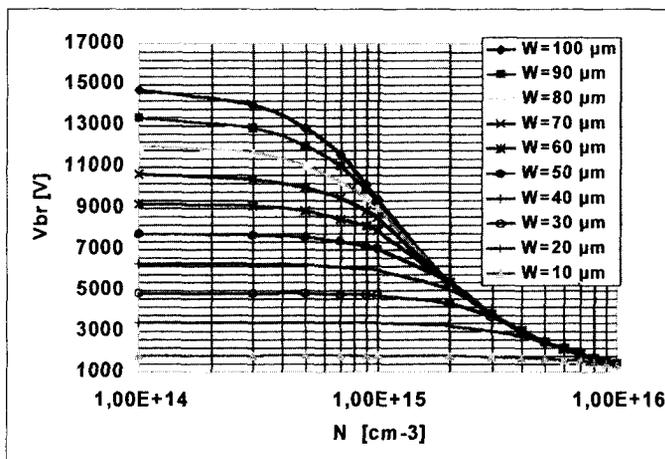


Figure 2 : Thyristor structure

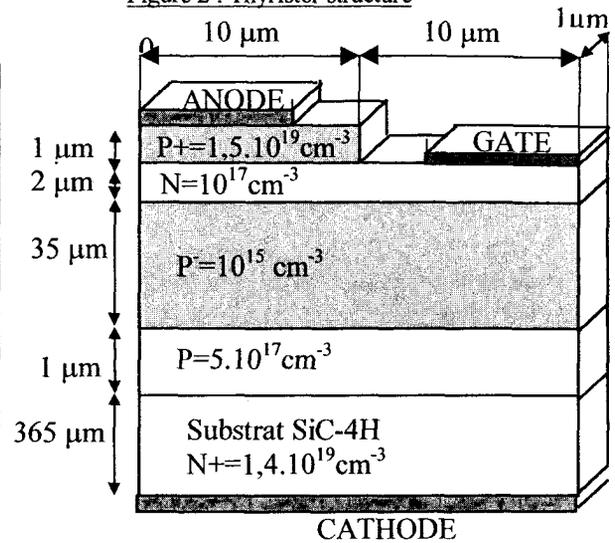


Figure 3 : optimised parameter for JTE

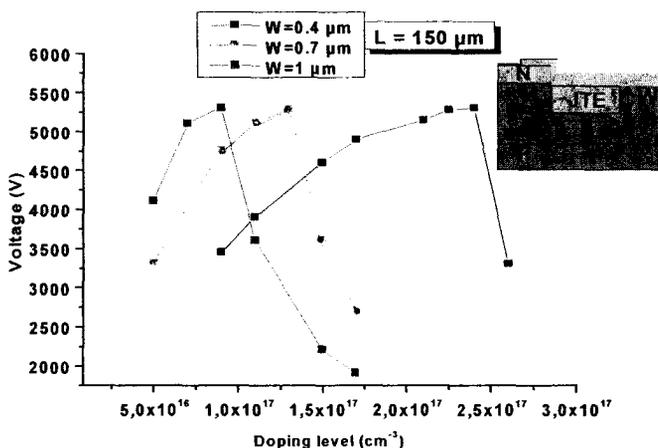


Figure 4 : voltage distribution in EGRs

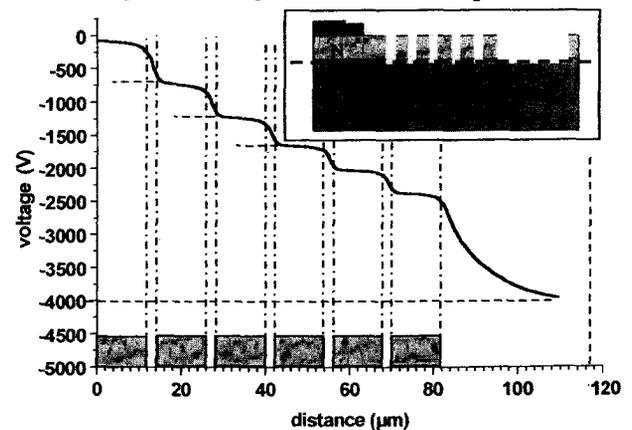


Figure 5 : application circuit and pulse current

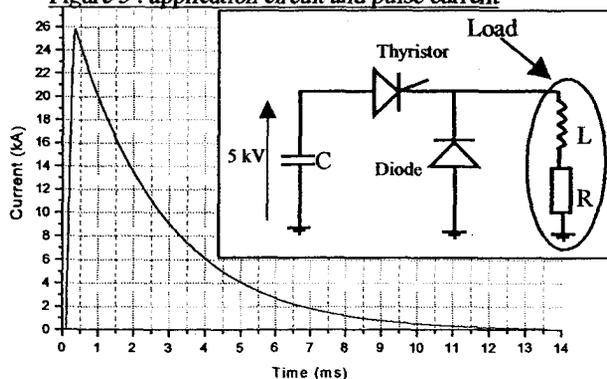
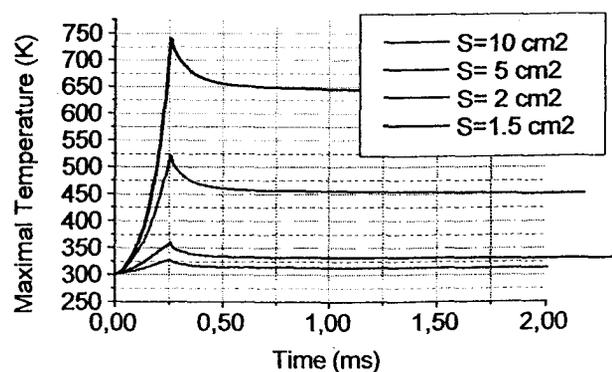


Figure 6 : Temperature versus area device



**Dynamic Performance of 2.6 kV 4H-SiC Asymmetrical GTO Thyristors**A. K. Agarwal<sup>1</sup>, P.A. Ivanov<sup>2</sup>, M.E. Levinshtein<sup>2</sup>, J.W. Palmour<sup>1</sup>, and S. L. Rummyantsev<sup>2</sup><sup>1</sup>Cree, Inc., 4600 Silicon Drive, Durham, NC 27703, USAPhone: 919-313-5539, Fax: 919-313-5696, email: [Anant\\_Agarwal@cree.com](mailto:Anant_Agarwal@cree.com)<sup>2</sup>The Ioffe Institute of Russian Acad. of Sci., Politekhnikeskaya 26, 194021 St-Petersburg, Russia

Silicon carbide shows tremendous potential for bipolar device applications such as inverters and switch-mode power supplies. Very recently, remarkable progress has been made in 4H-SiC based GTO thyristors. For example, 4H-SiC GTO thyristors with 2.6 kV forward blocking capability and up to 12 A of forward current were successfully demonstrated [1]. In this paper, we examine the turn-on and turn-off performance of these GTO thyristors.

A cross-sectional view of the thyristor structure is shown in Fig. 1. Five epilayers were grown on 380  $\mu\text{m}$  thick, 8° off-axis 4H-SiC n-type substrates with resistivity of 0.02  $\Omega\cdot\text{cm}$ . The blocking p<sup>-</sup> (base) layer was 50  $\mu\text{m}$  thick, doped to around  $7 \times 10^{14} \text{ cm}^{-3}$ . The p<sup>+</sup> buffer layer served to block the spreading of the depletion layer under forward bias, thus making the device asymmetrical. The proper injection efficiency of the p<sup>++</sup>(anode)-n(base) junction was provided by very heavy doping of the p<sup>++</sup>-layer to  $1 \times 10^{19} \text{ cm}^{-3}$ . It is worth noting that, owing to the relatively large ionization energy of Al in SiC (0.24-0.26 eV), only about 2 percent of the Al atoms are ionized at room temperature. As a result, the concentration of holes in the p<sup>+</sup>-emitter grows exponentially with temperature in the range from 300 to 450 K.

Figure 2 shows the time dependence of the current density during the turn-on process in a 2.6 kV SiC thyristor at different temperatures. The steady state current density  $j_o \approx 1200 \text{ A/cm}^2$ . It can be seen that the turn-on process is strongly temperature dependent. The total turn-on time is 1.2  $\mu\text{s}$  at 293 K and only 0.4  $\mu\text{sec}$  at 404 K. It can also be seen that at  $T > 380 \text{ K}$  the temperature dependence of the turn-on process tends to saturate. Qualitative analysis, analytical calculations, and computer simulations have been made to clarify the origin of this effect. It is shown that the temperature ionization of the Al dopant in the p<sup>+</sup>-emitter is mainly responsible for the effect. The hole concentration in the p<sup>+</sup>-emitter grows sharply with increasing temperature, making the injection coefficient of the p<sup>+</sup>-n junction larger.

We also report on the gate turn-off performance of 4H-SiC asymmetrical GTO thyristors with 2.6 kV breakover voltage, for temperatures ranging from 293 K to 500 K (Figs. 3-4). Both quasi-static and pulse regimes of the gate turn-off operation were studied. The temperature dependence of turn-off time and cathode holding current were investigated. At every temperature, there is a maximum value of cathode current  $I_{Con \text{ max}}$ , which can be turned off by the gate current. At room temperature,  $I_{Con \text{ max}}$  is equal to 3.3 A which corresponds to current density  $j_C \approx 1000 \text{ A/cm}^2$ . Turn-off current gain  $K_G = I_G / I_{Gst}$  depends on temperature, the gate pulse duration  $\Delta t_G$ , and the current density in the on-state. The  $K_G$  is maximum when  $\Delta t_G$  is large (quasi-static turn-off by the current  $I_{Gst}$ ). At  $j_C = 1000 \text{ A/cm}^2$ , the maximum value of  $K_G$  is equal to 6. With  $j_C$  decreasing,  $K_G$  increases, and at  $j_C = 300 \text{ A/cm}^2$ ,  $K_G = 12.5$ . The above value of  $K_G$  is the highest reported for SiC GTO's. The turn-off gate current  $I_G$  increases with a decrease in  $\Delta t_G$ . The following semiempirical formula describes the  $I_G / I_{Gst}$  dependence well over the entire temperature range:

$$I_G / I_{Gst} = \frac{1}{1 - \exp(-\Delta t_G / \tau^*)}, \quad (1)$$

where  $\tau^*$  is a fitting parameter which can be considered as a rough estimation of the carrier lifetime in the blocking base. The  $\tau^*$  is found to grow exponentially from 0.6 to 3.6  $\mu\text{s}$  in the temperature interval 293 – 502 K.

### References

[1] A. Agarwal, S.-H. Ryu, R. Singh, O. Kordina, and J.W. Palmour, "2600 V, 12 A, 4H-SiC, Asymmetrical Gate Turn-off (GTO) Thyristor Development", from Silicon Carbide and Related Materials - 1999 (Part 2), Materials Science Forum Vols. 338-342, C.H. Carter, Jr., R.P. Devaty, and G.S. Rohrer, eds. (Trans Tech Publications, Zurich, Switzerland, 2000) p. 1387-1390.

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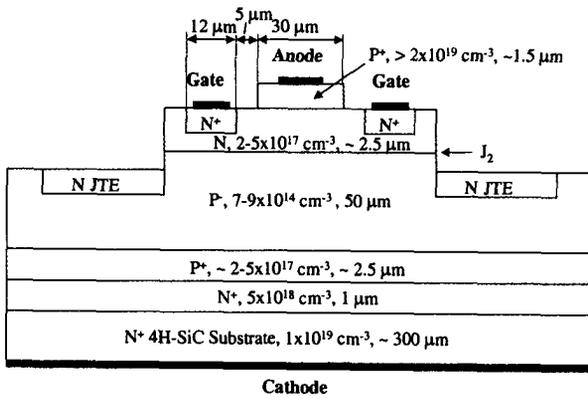


Fig. 1. Cross-sectional view of the thyristor structure under investigation.

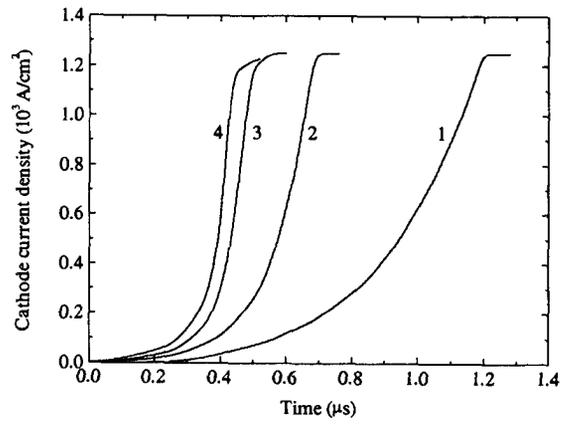


Fig. 2. Time dependence of the current density during the turn-on process at different temperatures.  $T$  (K): (1) 293, (2) 330, (3) 379, and (4) 404. Cathode voltage  $V_c = 200$  V, load resistance  $R_l = 50$  Ohm.

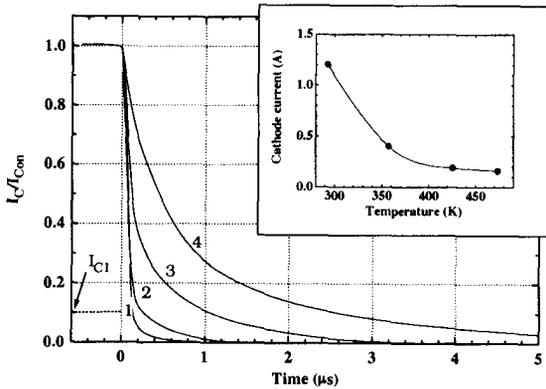


Fig. 3. The cathode current decay during the turn-off process at different temperatures.  $T$ (K): 1 – 293, 2 – 358, 3 – 426, 4 – 474. In all cases, a very long turn-off gate pulse of 100 mA is applied. For every temperature, the turn-off cathode current  $I_C$  is normalized to the cathode current  $I_{Con}(T)$ , where  $I_{Con}(T)$  is the maximum current  $I_C$  that can be turned off by a 100 mA gate pulse. Inset shows the temperature dependence of  $I_{Con}$ .

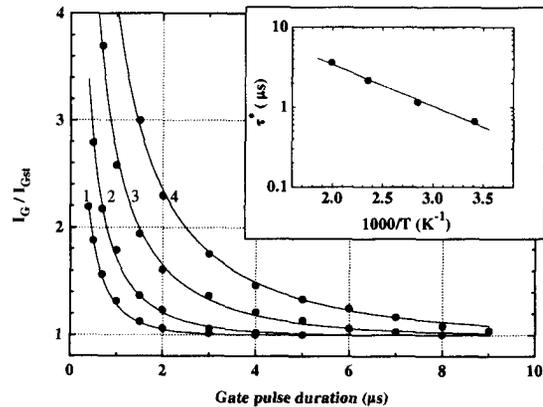


Fig. 4. The dependence of normalized turn-off gate current  $I_C/I_{Gst}$  on gate pulse duration at different temperatures. Solid lines are plotted according to Eq. (1) with  $\tau^*$  as a fitting parameter. 1 – 293 K, 2 – 351 K, 3 – 424 K, 4 – 502 K.  $R_l = 25$  Ohm. Inset shows the dependence of  $\tau^*$  versus  $1000/T$ .

## Electrical characteristics of 6H-SiC bipolar diodes realized by sublimation epitaxy on Lely substrates.

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Sublimation epitaxy SE has several advantages over chemical vapor deposition such as a higher growth rate, possibility of in-situ etching...The aim of this work is to demonstrate the feasibility of bipolar diodes with high blocking voltages realized on layers grown by SE. This method allows to obtain n-type layers with doping level as low as  $N_d - N_a \sim 5 \times 10^{15} \text{ cm}^{-3}$  on  $n^+$  6H-SiC Lely substrates [1].

Epilayers with thickness between 10 and 20  $\mu\text{m}$  have been grown, using a growth rate in the order of 15  $\mu\text{m/h}$ . PN junctions have been realized by a triple implantation of Aluminum into such epilayers to create the emitter, with energies ranging from 70 to 180 keV and a total dose of  $8.8 \times 10^{15} \text{ cm}^{-2}$ . A surrounding region, named Junction Terminal Extension (JTE), has been realized also by a 4-fold implantation of Aluminum, with energies ranging from 50 to 300 keV, with a total dose of  $1.18 \times 10^{13} \text{ cm}^{-2}$ . The aim of this region is to decrease the probability of surface breakdown, by the spreading out of the equipotential lines. The diameters of diodes are in the range 200-800  $\mu\text{m}$ . The JTE width is 250  $\mu\text{m}$ , as shown by previous numerical studies.

Rectifying properties are observed in forward bias with current density between 5-10  $\text{A cm}^{-2}$  at 2.5 V. In the reverse direction, structures has rather stable breakdowns (Figure 1) in the 800 V range. Values of the experimental breakdown voltage on diodes with the smallest diameter (200  $\mu\text{m}$ ) are in agreement with calculated values.

Temperature stability of this diode was investigated up to 1080 K (Figure 2).

Electrical characteristics of diodes realized on layers grown by SE epitaxy will be detailed in the full article.

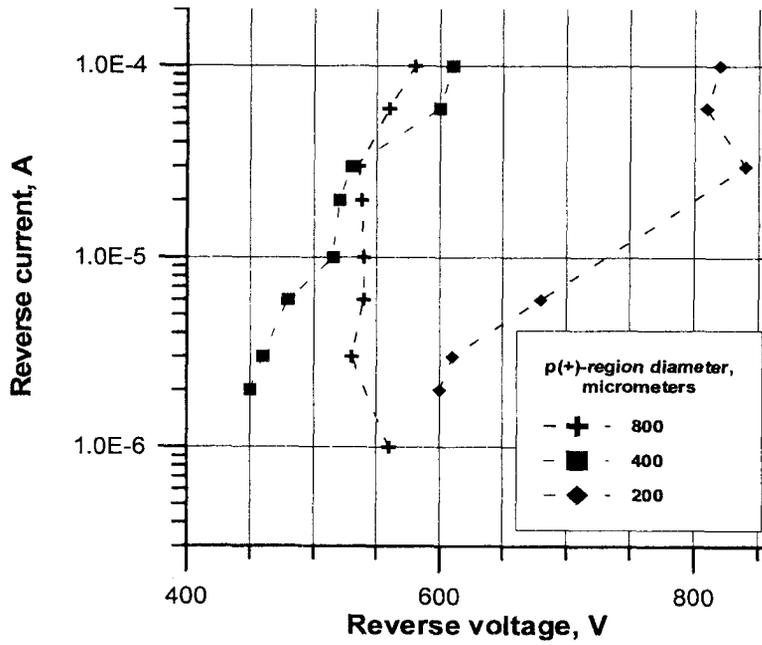


Figure 1 : Reverse current voltage characteristics of the diodes with different areas at room temperatures.

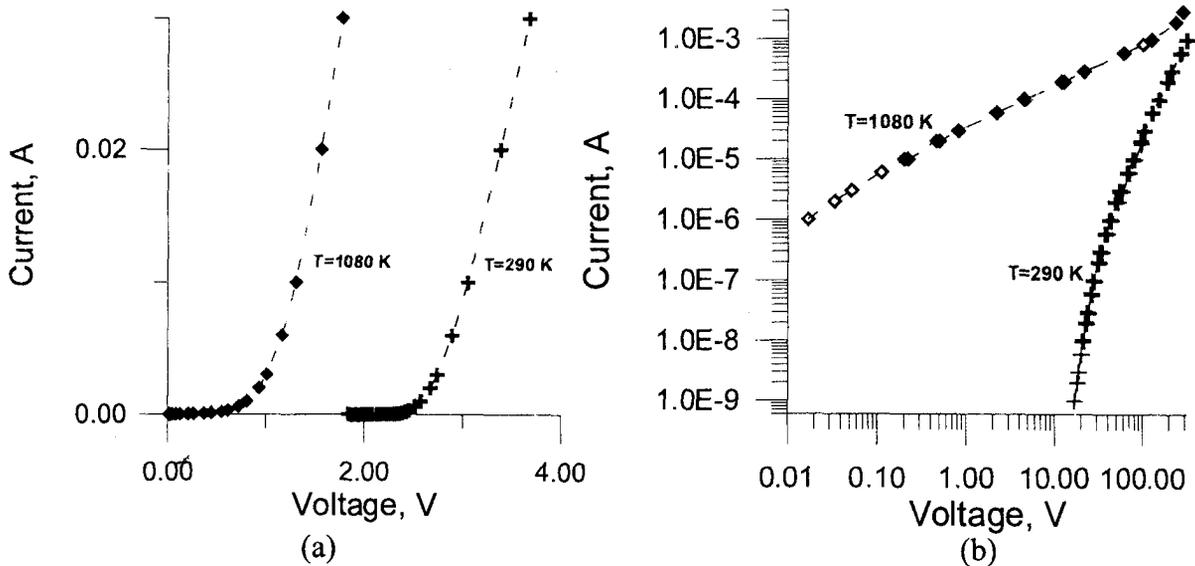


Figure 2 : Forward (a) and reverse (b) current voltage characteristics of the diodes with a diameter of 200 microns at room temperature and at 800°C.

This work was partly supported by INTAS grant N97-30834.

References:

[1] Savkina N.S., Lebedev A.A., Davydov D.V., Strel'chuk A.M., Tregubova A.S., C.Raynaud, J-P.Chante, M.L.Locatelli et al. Mat. Sci. Engin, B77, 50-54 (2000).

## On the Temperature Coefficient of 4H-SiC NPN Transistor Current Gain

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Silicon carbide (SiC) has been recognized as an attractive wide-bandgap material for high-power, high-voltage, and high temperature applications. While SiC power rectifiers are about to be commercially available, SiC power switches still require substantial development efforts. The major problems facing the MOSFET-based SiC power switches are the low inversion layer carrier mobility and the poor reliability of gate oxide under both high field and high temperature. GTOs are free of gate oxides but, being latch-on devices, are not as attractive for many power system applications such as motor control inverters. Before a novel high temperature and high power switch free of gate oxide becomes available, SiC BJTs could be a candidate for some system applications at high ambient temperatures. The disadvantages of BJT switches normally lie in two aspects. First, BJTs are current controlled switches. When designed to block high voltage and conduct high current, a substantial base current is needed. Darlingtons BJTs can reduce the complexity in implementing the base drive circuitry but with a substantially increased forward voltage drop. Second, BJTs normally have a positive temperature coefficient (PTC) for current due to carrier lifetime increase with increasing temperature, which makes paralleling power BJT difficult. Simulation work has, however, shown that SiC BJTs should have the desired negative temperature coefficient (NTC) due to acceptor Al's deep ionization energy (191 meV) [1]. The first experimental demonstration of 4H-SiC power BJT [2] observed an NTC while the subsequent reports reported both PTC [3] and NTC [4]. This paper focuses on the effects of base carrier lifetime, doping density, and acceptor energy level on the temperature dependence of NPN transistor gain. It will be shown that, depending on the carrier lifetime and base doping, 4H-SiC NPN transistors with Al-doped base could show both PTC and NTC. Besides, SiC NPN BJTs would generally have a PTC if an acceptor with  $E_A < 170\text{meV}$  were used.

The 4H-SiC NPN cell structure used in the simulation is shown in Fig.1. Its  $J_C$ - $V_{CE}$  curves at room temperature are shown in Fig.2. The acceptor energy level ( $E_A$ ) has great effects on  $\beta$  as illustrated in Fig.3. When  $E_A < 170\text{meV}$ , the device has a PTC in  $\beta$ . At  $E_A = 170\text{meV}$ , the NTC in  $\beta$  begins to appear at current densities from 30 to  $150\text{A/cm}^2$ . When  $E_A = 191\text{meV}$ , the temperature coefficient of  $\beta$  is negative up to  $500\text{A/cm}^2$  for the structure shown in Fig.1. Figs. 4 and 5 show the effect of electron lifetime in the base on  $\beta$  at different base doping concentrations. For a base doping concentration of  $1 \times 10^{17}\text{cm}^{-3}$ , the turning point of the temperature coefficient of  $\beta$  is at  $\tau_n = 0.291\mu\text{s}$ . Below  $0.291\mu\text{s}$ , the temperature coefficient of  $\beta$  is positive. Above  $0.291\mu\text{s}$ , the temperature coefficient of  $\beta$  becomes negative at around  $60\text{A/cm}^2$ . At  $\tau_n = 2.908\mu\text{s}$ , NTC is found at the current densities from 20 to  $150\text{A/cm}^2$ . For the base doping concentration of  $2.5 \times 10^{17}\text{cm}^{-3}$ , the turning point of the temperature coefficient of  $\beta$  is around  $\tau_n = 26\text{ns}$ . Below 26ns, the temperature coefficient of  $\beta$  is positive. Above 26ns,  $\beta$  has an NTC. With electron lifetimes in the base of 55ns and 257ns, an NTC is obtained at the current density up to  $300\text{A/cm}^2$  and  $800\text{A/cm}^2$ , respectively. Thus, using higher base doping concentration can relax the requirement for carrier lifetime to obtain an NTC. The effect of the base doping concentration on  $\beta$  with an electron lifetime of 100ns is depicted in Fig.6. A PTC is found when the base doping concentration is smaller than  $1.5 \times 10^{17}\text{cm}^{-3}$ .

[1] K. Adachi, C.M. Johnson, S. Ortolland, N.G. Wright and A.G. O'Neill, Materials Science Forum, Vols. 338-342 (2000), 1419-1422.  
 [2] Y. Luo, L. Fursin and J. H. Zhao, Electronics Letters, No.17, Vol.36 (2000), 1496-1497.  
 [3] Sei-Hyung Ryu, Anant K. Agarwal, Ranbir Singh, and J. W. Palmour, IEEE Electron Devices Letters, Vol.22, No.3 (2001), 124-126.  
 [4] Yi Tang, Jefferey B. Fedison, and T. Paul Chow, IEEE Electron device letters, Vol.22, No.3 (2001), 119-120.

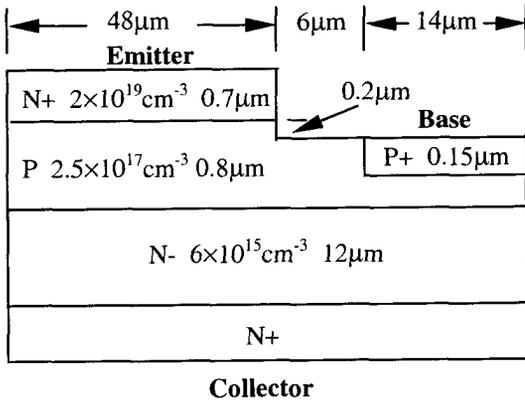


Fig.1 Cross-sectional view of 4H-SiC BJT

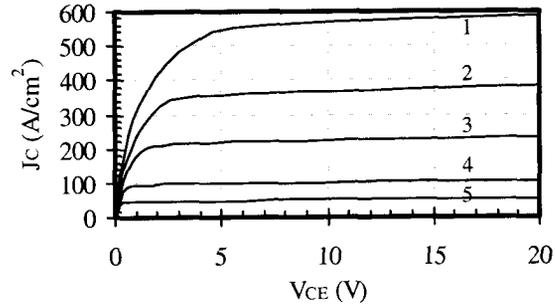


Fig.2  $J_C - V_{CE}$  characteristics of 4H-SiC BJT at 300K. In the base,  $\tau_n = 5\tau_p = 0.1\mu s$ ,  $\mu_n = 441\text{cm}^2/\text{Vs}$ .  
 1:  $J_B = 3.5\text{A}/\text{cm}^2$  2:  $J_B = 7.1\text{A}/\text{cm}^2$  3:  $J_B = 17.9\text{A}/\text{cm}^2$   
 4:  $J_B = 35.1\text{A}/\text{cm}^2$  5:  $J_B = 71.4\text{A}/\text{cm}^2$

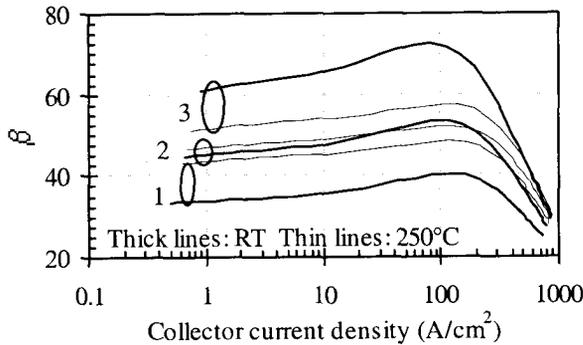


Fig.3 The effect of the acceptor energy level ( $E_A$ ) on  $\beta$ .  $\tau_n = 5\tau_p = 0.1\mu s$ ,  $\mu_n = 441\text{cm}^2/\text{Vs}$ ,  $N_B = 2.5 \times 10^{17}\text{cm}^{-3}$ .  
 1:  $E_A = 150\text{meV}$  2:  $E_A = 170\text{meV}$  3:  $E_A = 191\text{meV}$

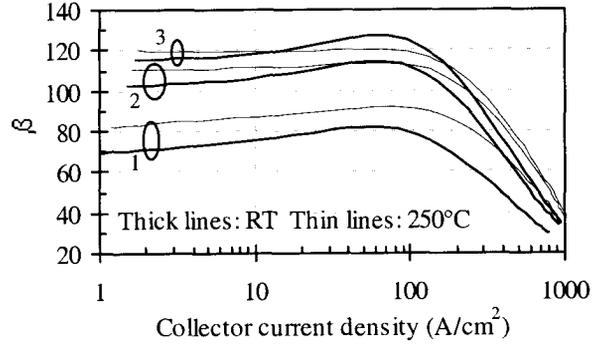


Fig.4 The effect of base carrier lifetime on  $\beta$  at a base doping concentration of  $1 \times 10^{17}\text{cm}^{-3}$ .  $\mu_n = 441\text{cm}^2/\text{Vs}$ .  $\tau_n = 5\tau_p$ . 1:  $\tau_n = 0.058\mu s$  2:  $\tau_n = 0.291\mu s$  3:  $\tau_n = 2.908\mu s$

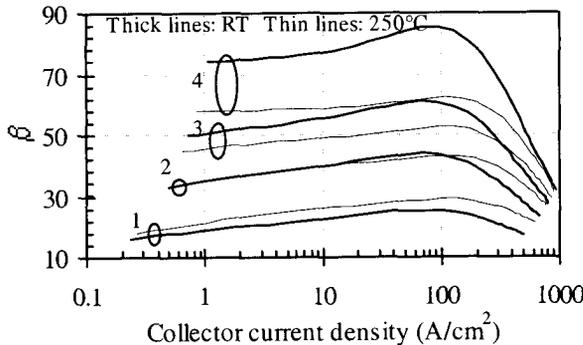


Fig.5 The effect of the carrier lifetime in base on  $\beta$  at a base doping concentration of  $2.5 \times 10^{17}\text{cm}^{-3}$ .  $\mu_n = 441\text{cm}^2/\text{Vs}$ .  $\tau_n = 5\tau_p$ . 1:  $\tau_n = 10\text{ns}$  2:  $\tau_n = 26\text{ns}$  3:  $\tau_n = 55\text{ns}$  4:  $\tau_n = 257\text{ns}$

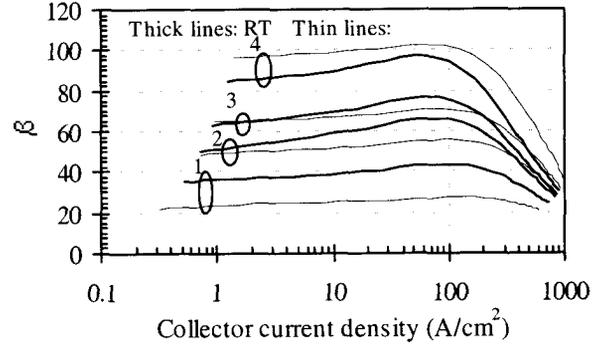


Fig.6 The effect of the base doping concentration  $N_B$  on  $\beta$ .  $\tau_n = 5\tau_p = 0.1\mu s$ ,  $\mu_n = 441\text{cm}^2/\text{Vs}$ .  
 1:  $N_B = 5.0 \times 10^{17}\text{cm}^{-3}$  2:  $N_B = 2.0 \times 10^{17}\text{cm}^{-3}$   
 3:  $N_B = 1.5 \times 10^{17}\text{cm}^{-3}$  4:  $N_B = 1.0 \times 10^{17}\text{cm}^{-3}$

## A Novel High-Voltage Normally-Off Field Gated Bipolar Transistor in 4H-SiC

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The commercial availability of 3-inch wafers of 4H-SiC and the continued effort in scaling up SiC substrates by a number of companies are fostering a SiC power electronic industry. A lot of 4H-SiC high voltage and high speed devices have been demonstrated with the majority focusing on replicating the corresponding Si power devices in the hope of achieving higher power levels. It has, however, been realized that MOS-based SiC devices may not be suitable for applications under both high electric fields and high temperatures (over 150 C) due to the reliability concern of the gate oxide. In order to take full advantage of SiC superior material properties, SiC power switches free of gate oxide or insulator need to be designed and developed.

In this paper, a novel high voltage normally-off field gated bipolar transistor (FGBT) in 4H-SiC (patent pending) is proposed. Normally-off power switches are preferred over normally-on devices, which present substantial complication in practical applications such as motor control power inverters. The DC and transient characteristics of this device are investigated by performing two-dimensional numerical simulations. ISE SiC TCAD module is used in this simulation. The 4H-SiC material parameters used in the simulation are taken from most recently published literatures in order to obtain realistic results. The cross sectional view of the proposed normally-off FGBT is shown in Fig.1. A buried N<sup>+</sup> layer formed by using MeV deep Nitrogen implantation is used to collect the electrons injected from the emitter and to define the horizontal channel. A semi-insulating layer formed by deep Vanadium implantation is used to terminate the horizontal channel controlled by an implanted N<sup>+</sup>P gate. The simulated DC characteristics are presented in Fig.2. The device is normally-off and blocks 3015V at 300K and over 3500V at 600 K. It can be turned on with gate voltages up to of 2.7V and 2.0V at 300K and 600K, respectively, with a negligible gate current. At 100A/cm<sup>2</sup>, the forward voltage-drops are 3.82V and 3.58V at 300K and 600K, respectively. Since there is presently a large variation in carrier lifetimes in 4H-SiC materials although, being an indirect band gap semiconductor, its carrier lifetimes should be long, the effects of the variation of carrier lifetimes on the performance of the device have been studied and are depicted in Fig.3. The forward voltage drop improves when electron lifetime  $\tau_n$  is increased to around 2 $\mu$ s. Although beyond 4 $\mu$ s the improvement is minimum for this particular design, longer carrier lifetimes should make it possible to design the device with a thicker base with improved blocking voltage capability. The vertical channel opening  $d$  is a key design parameter for high voltage normally-off FGBT. Its effects on blocking voltage and the forward current density at 5V are illustrated in Fig.4. The optimized value for  $d$  for a 3,000V FGBT is 2.5 $\mu$ m. The switching speed is a critical parameter for a power switch. The simulated switching waveforms for a resistive load circuit with an emitter current density of 200A/cm<sup>2</sup> and a blocking voltage of 1000V are summarized in Fig.5. With a  $dV_{GC}/dt$  of 5.4 $\times 10^6$ V/s, the turn-on time is 0.52 $\mu$ s while the turn-off time is 1.17 $\mu$ s at 300K. Experimental demonstration of the first 4H-SiC FGBT will be presented along with future work suggestions for improved device performance.

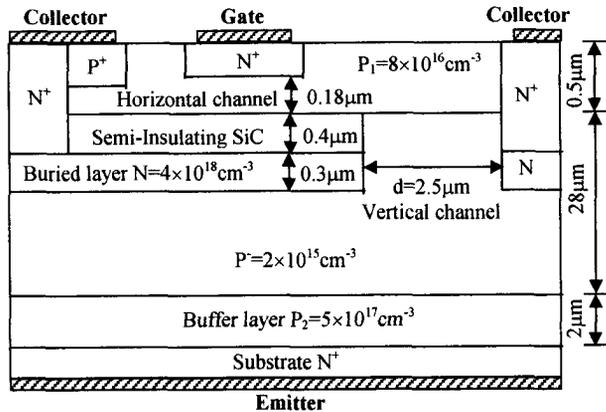


Fig.1 Cross sectional view of Normally-Off VJFET.

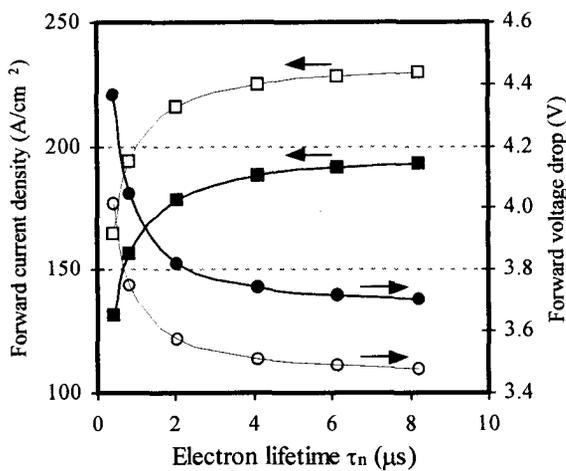
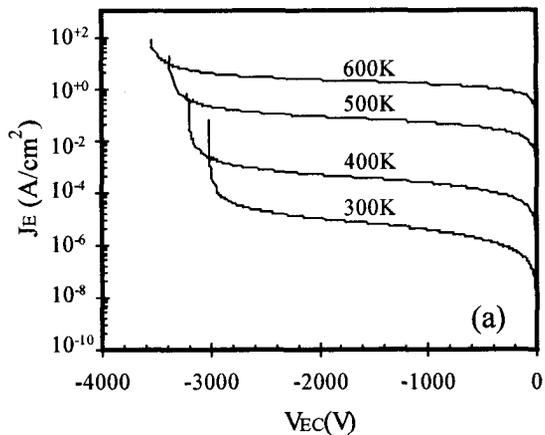


Fig.3 The effects of the variation of carrier lifetime. Forward current density is measured at  $V_{CE}=5V$ . Forward voltage drop is measured at  $J_E=100A/cm^2$ . Thick lines: 300K Thin lines: 600K

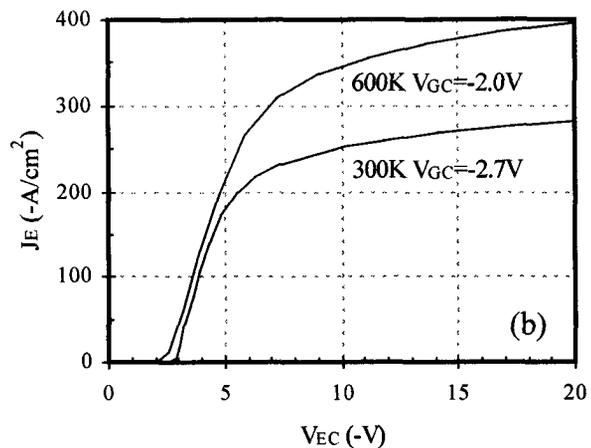


Fig.2  $J_E$ - $V_{EC}$  curves at (a) off-state and (b) on-state.

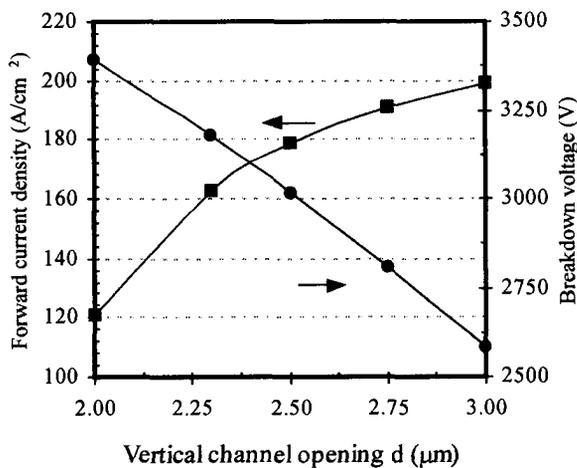


Fig.4 The effects of the vertical channel opening  $d$  on the forward current density at 5V and the breakdown voltage at 300K.

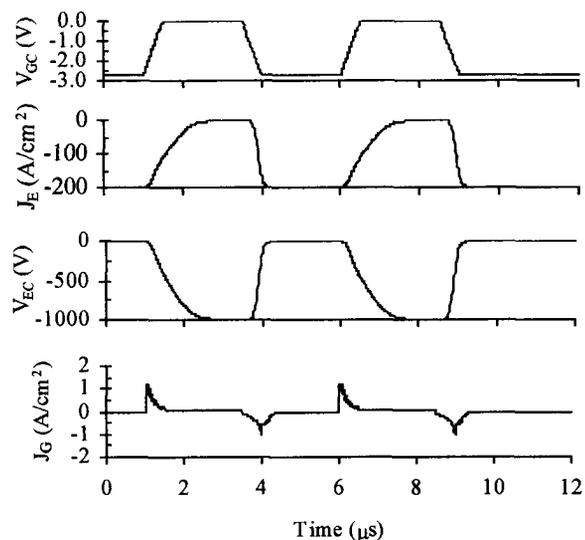


Fig.5. The switching waveforms at 300K.  $dV_{GC}/dt=5.4 \times 10^6 V/s$ .

**Hybrid MOS-Gated Bipolar Transistor Using 4H-SiC BJT**

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SiC has long been recognized as one of the candidates for high voltage, high temperature, high power applications. A novel MOS-Gated Bipolar Transistor (MGT) structure, which was demonstrated in silicon [1], was previously proposed in SiC [2]. Numerical simulations have proved that SiC MGT has several advantages over SiC IGBT, since it combines an n-channel turn-on MOSFET with an *npn* bipolar transistor, as well as a turn-off MOSFET. The schematic cross-section of the SiC MGT is shown in Fig. 1. The device is expected to have a wide Safe Operation Area (SOA) as well as a fast switching time [2]. However, current state-of-the-art 4H-SiC MOSFETs suffer from high interface trap density and low inversion layer mobility [3], making realization of a monolithic SiC MGT difficult. In this paper, we have used a silicon MOSFET driving 4H-SiC BJT to form a hybrid MGT and have characterized its performance.

The schematic of the hybrid MGT is shown in Fig. 2. The base current is provided by the turn-on MOSFET G1, which is commercial silicon MOSFET ECG 2380 with blocking voltage of 500V and on-resistance of 0.15Ω. A silicon MOSFET ECG 2984 with 50V voltage rating was used as the turn-off MOSFET G2 since high blocking capability was not required. The SiC BJT used in this structure was epi-base, epi-emitter 4H-SiC BJTs designed and fabricated by Cree Inc. [4]. The device has an on-resistance of 10.8mΩ·cm<sup>2</sup> and BV<sub>CEO</sub> of 1800V.

Fig. 3 shows the forward I-V characteristics of the hybrid MGT structure. The MOSFET current I<sub>DS</sub> forms the base current to turn on the BJT. As expected, there is a turn-on knee in the forward I-V characteristics, because the turn-on MOSFET G1, in between base and collector, prevents the SiC BJT from saturation. The forward drop at 100A/cm<sup>2</sup> (~1.4A) is about 4V. The maximum current is around 3A. The breakdown voltage of the hybrid MGT is limited by the blocking capability of the silicon MOSFET G1.

Fig. 4 shows the turn-on transients of the hybrid MGT. The rise time for the hybrid MGT is ~ 1.0μs. Fig. 5 shows the passive turn-off as well as the active turn-off of the hybrid MGT. During passive turn-off, the device is turned off by turning G1 off to stop the base current, so the turn-off recombination mechanism resembles an open-base turn-off of the bipolar junction transistor. At 100A/cm<sup>2</sup>, the turn-off time is ~ 2.0μs. The device can also be turned off faster by using the turn-off MOSFET G2 to shunt current. Fig. 6 shows the turn-on and turn-off gate signals. The two gate signals have an offset to prevent shorting. From the active turn-off of Fig. 5, the turn-off time can be reduced to less than 0.5μs.

The hybrid MGT structure is a voltage-controlled device with good current-handling capability that circumvents the current MOS problems in 4H-SiC. It is a good example of application of SiC BJTs in power switching territory.

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**References:**

- [1] T. Tanaka et al, IEEE Transactions on Electron Devices, Dec, 1986.
- [2] Y. Tang et al, Silicon Carbide and Related Materials Conf, Oct, 1999
- [3] R. Schomer et al, IEEE Electron Device Letters, vol. 20, 1999
- [4] S-H. Ryu et al, IEEE Electron Device Letters, vol. 22, 2001.

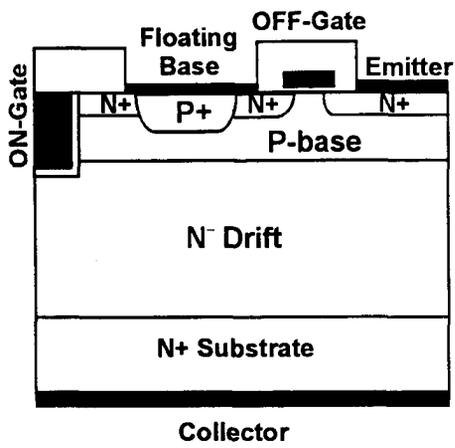


Figure. 1 Schematic cross-section of monolithic MOS-Gated Transistor

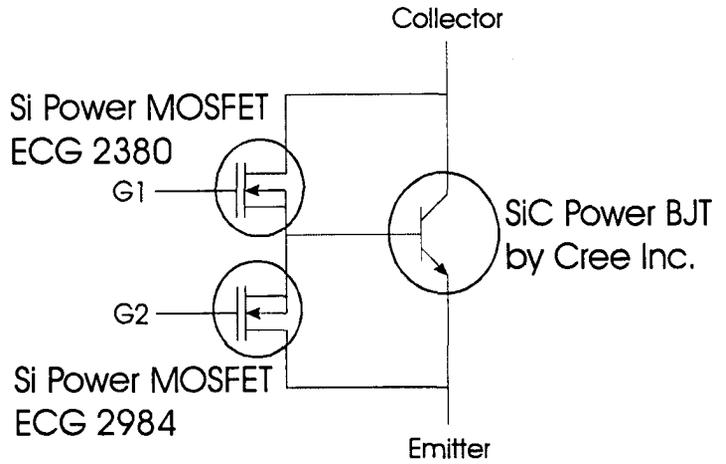


Figure. 2 Schematic of the hybrid MGT

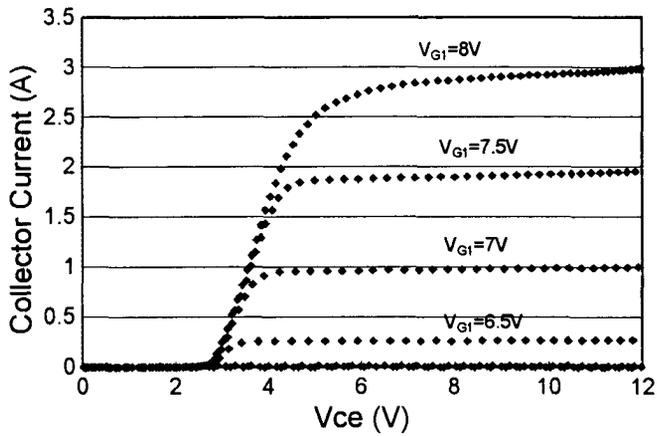


Figure. 3 Forward I-V Characteristics

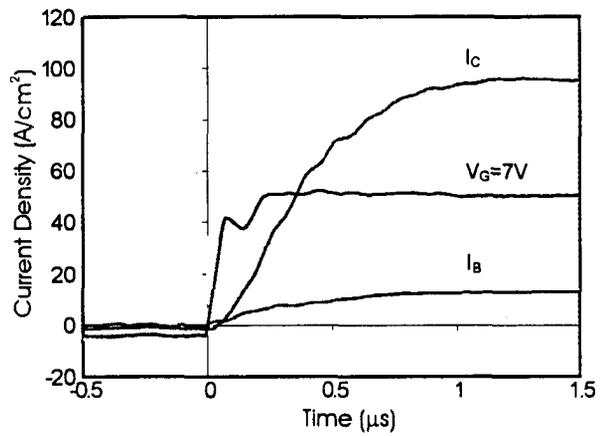


Figure. 4 Turn-on transient of the hybrid MGT

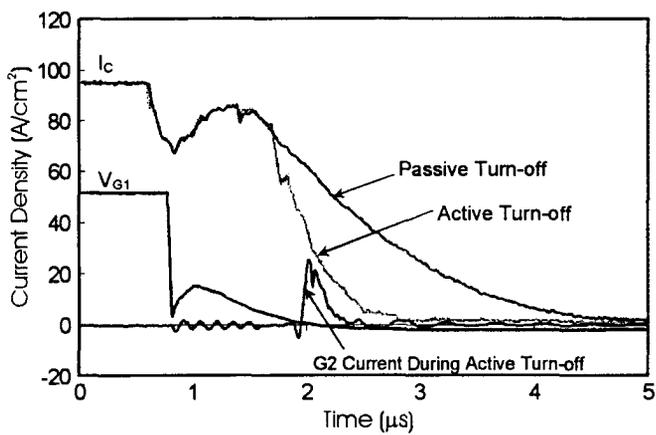


Figure. 5 Turn-off transient of the hybrid MGT

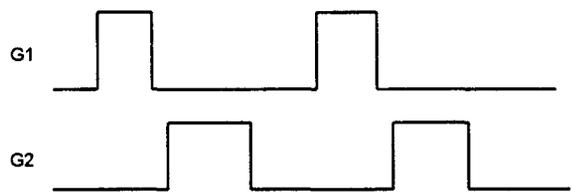
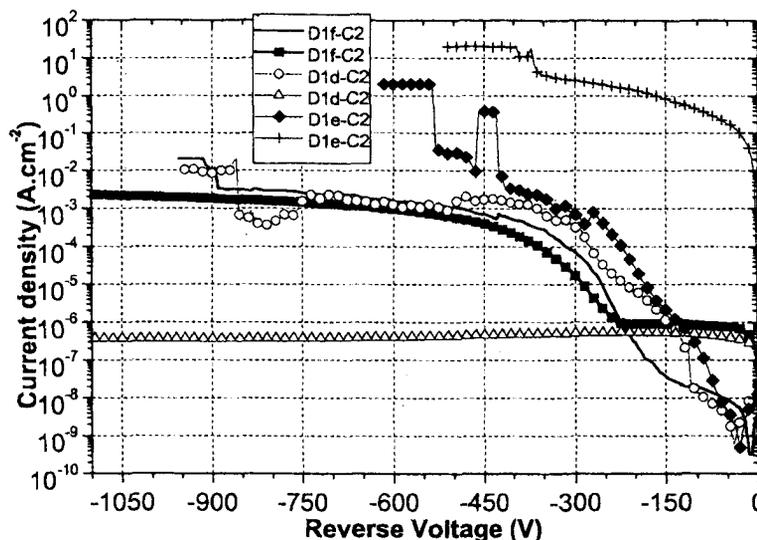


Figure. 6 Turn-off gate signals of the hybrid MGT

### STUDY OF 4H-SiC HIGH VOLTAGE BIPOLAR DIODES UNDER REVERSE BIASES USING ELECTRICAL AND OBIC CHARACTERIZATIONS

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Silicon carbide presents electrical properties suitable for many applications especially for high voltage devices. 4H-SiC p<sup>+</sup>nn<sup>+</sup> structures have been fabricated following Medici<sup>TM</sup> software simulations in order to sustain voltage as high as 6 kV. In particular, these diodes are realized by surrounding the emitter by a p-type region called JTE (Junction Termination Extension). The p<sup>+</sup> region and JTE were formed by multiple aluminum implantations at room temperature on n-type epilayer (40 μm-1×10<sup>15</sup> cm<sup>-3</sup>), followed by a thermal annealing at 1700 °C during 30 min. Current-voltage (I-V) characteristics at 300 K show good rectifying properties. Under reverse bias in air ambient, the curve presents two distinct zones (Fig. 1).



**Fig. 1: Reverse electrical characteristics measured at 300 K in the air of diodes with JTE. Several bias sweeps are presented for each diode. The order of appearance in the legend corresponds to the order of I-V measurement performed on each diode.**

In the first part of the initial characteristic, the current remains weak up to reverse bias,  $V_R = 200$  V. Beyond this voltage, the current rises quickly until  $V_R = 400$  V and saturate in the range  $[10^{-4} - 10^{-3}]$  A/cm<sup>2</sup>. When  $V_R > 500$  V, the electric arc between the anode contact and either the etched area of the sample or the moralization begin to appear. This second part of I-V curve is not reproducible. During the second measurement in the first part, we observe an increase in the current. For the second part of the characteristic, we note that for a same voltage the measured current is weaker. Those results are completed by I-V measurements performed in SF<sub>6</sub> ambient under small overpressure. In these conditions we observe the same behavior than in the air ambient. However, luminous white points in the emitter periphery accompany the electric arcs. Towards 2000 V the arcs involve the diodes breakdown with JTE. For the diodes without junction termination the maximum breakdown value reached is 1400 V. A luminous white points indicate the presence of a high electric field at this place.

This result is confirmed by comparing OBIC (Optical Beam Induced Current) measurements on diodes with JTE. No photocurrent is detected on JTE position and an OBIC signal peak emerges at the emitter edge for  $V_R \approx 300$  V (Fig. 2). OBIC measurements performed on diodes without JTE (Fig. 3). When  $V_R = 300$  V, we see a photocurrent peak at the edge of junction. Those results indicate a presence of high electric field at this place. It means that the JTE are not completely effective. The presence of high electric field to this voltage lets think that there are positive charges on the SiC surface which induce a degradation of the JTE performances. The instabilities of current noted during I-V measurements could confirm these assumptions. These measurements completed by OBIC measurement at several wavelengths and with high voltage will be analyzed in the full paper. The role of electrical activation of aluminum and surface effects will be discussed.

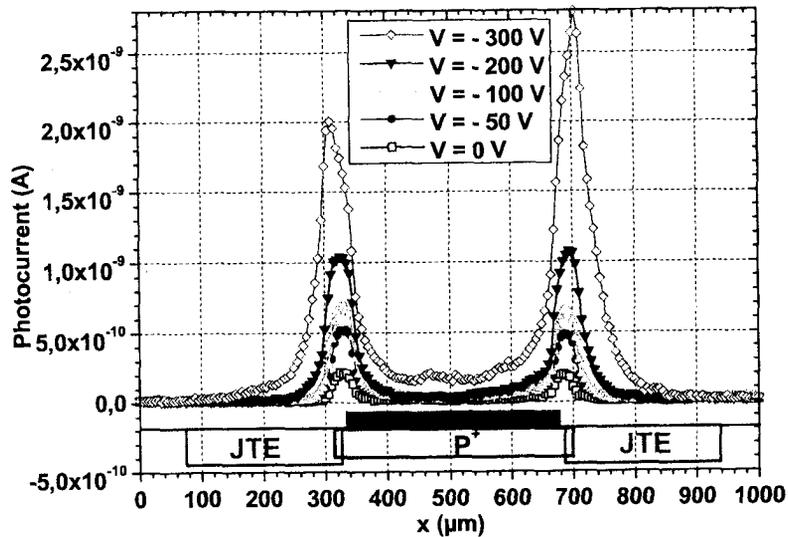


Fig. 2: OBIC measurements performed on diode with JTE at  $\lambda = 363.8$  nm with  $P_{opt} = 1$  W/cm<sup>2</sup> for different reverse voltage.

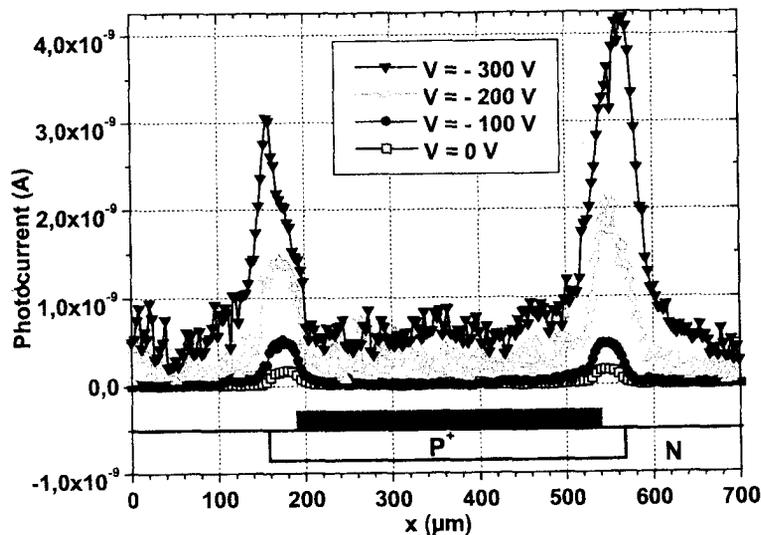


Fig. 3: OBIC measurements performed on diode without JTE at  $\lambda = 363.8$  nm with  $P_{opt} = 1$  W/cm<sup>2</sup> for different reverse voltage.

## Highly doped implanted pn junction for SiC Zener diodes fabrication

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The objective of this work was to use implantation process to form a two side highly doped pn-junction (figure 1) in order to obtain a Zener effect. In the fabrication process we used 6H-SiC substrates N type 0.043 ohm.cm ( $4e18\text{ cm}^{-3}$ ) from CREE. We performed a multiple Al implantation through a mask layer using 6 energies ranging from 330KeV to 2000KeV and two implantation temperatures (room temperature and 305°C). The total implanted dose was  $5.39e15\text{ cm}^{-2}$  and a square box profile with a plateau chemical concentration of  $4e19\text{ cm}^{-3}$  was expected. The peripheral protection was made by mesa etching and the contact was made with an annealed Ti/Ni metal layer.

Implantation and activation properties have been studied by physical (RBS, SIMS) and electrical (TLM, Van DerPauw) characterisation. MESA diodes have been characterised electrically measuring their static I-V characteristics. In figure 2 we represented the I-V curves of the diodes implanted at RT (sample S105) and 305°C (sample S104) for different contact annealing temperature. Before contact annealing, there is a significant difference in current capability between samples implanted a room temperature and at 305°C. After contact annealing at 900°C, the linear region of the I-V curve is similar for both samples but the series resistances are still lower for the 305°C implanted sample. When operation temperature is increased, the diode behaviour exhibits the standard decrease of the offset voltage and increase of the current for a given on-state voltage (figure 3). In the reverse mode, the diodes behaviour is particular due to the inherent structure the junction: N-side of the junction (substrate) is doped  $4e18\text{ cm}^{-3}$  and the implanted P-type doping (extracted from TLM) is  $3.35e18$  and  $6.3e18\text{ cm}^{-3}$  for RT and 305°C implantation, respectively. With these high doping levels, Zener mode conduction (tunnelling leakage currents) can be expected when the diode is reverse biased. In figure 4 the reverse I-V curves of a 305°C implanted diode are presented. We can infer three conduction regions in the reverse mode. Up to 8V, a first leakage current region similar to standard reverse biased pn diode dominated by generation/recombination currents is observed. From 8 to 42 V we can note a first increase of the leakage current. This leakage current is a tunnelling current as was confirmed by numerical simulation. A second change in the current slope is observed at 42V but it is not clear that a complete avalanche process is responsible for this current increase, unlike simulations are predicting. Figure 4 shows the reverse I-V curves of the diode for 4 consecutive measurements reaching a current of 0.1 A, corresponding to a current density of  $150\text{A/cm}^2$ . There is no destruction nor degradation of the device and the I-V curves are very repetitive. This seems indicate that the reverse current flow is taking place through the plane area of the junction and not on the border of the device. This has to be confirmed by OBIC measurements. This behaviour is absolutely necessary to use the diode as a protection device.

When comparing the reverse characteristics of RT and 305°C implanted diodes (figure 5) we observed that the leakage current is higher for RT implanted diodes at low voltage bias (0 to 8V). This behavior has to be checked. It could be due to a higher quantity of defect, especially in the junction region. The influence of the contact annealing on the reverse current shown that the leakage current decreases at low voltage bias after annealing at 700°C. It is possible that defects have been removed by the contact annealing process.

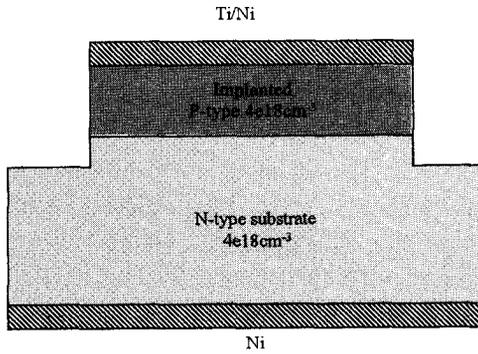


Fig. 1: Schematic cross section of the targeted implanted pn-diodes

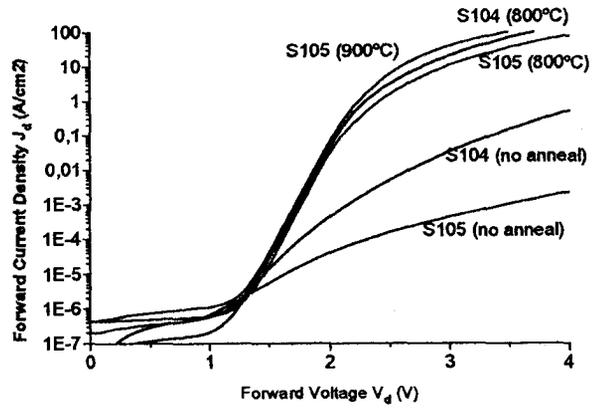


Fig. 2: Forward voltage characteristics of fabricated diodes: S104 is implanted at 305°C and S105 is implanted at room temperature.

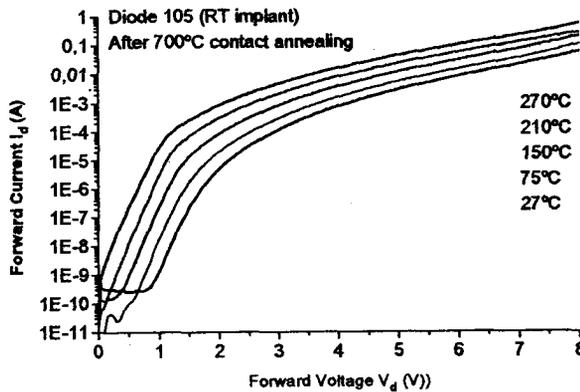


Fig. 3: Forward characteristics of a S105 diode annealed at 700°C measured at various temperatures

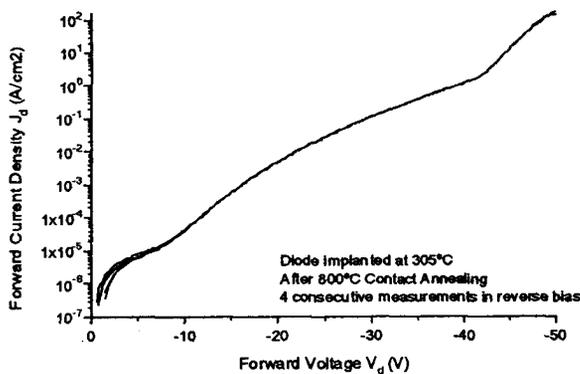


Fig 4: Reverse I-V curves of a S104 diode measured up to 100mA 4 times consecutively.

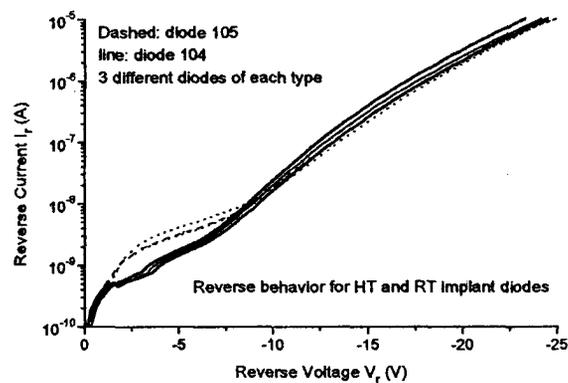


Fig 5: Reverse I-V curves (3 of each) of a S104 diode and a S105 diode

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### 4H-SiC pn diode grown by LPE method for high power applications

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Silicon carbide is a promising wide bandgap semiconductor material for high power applications requiring operation at high temperatures. Despite considerable progress in fabricating high power and high voltage SiC devices by CVD method, the problems with reducing defect density (micropipes) in SiC epitaxial layers and with increasing device lifetime (degradation of device characteristics connected with deep traps) remain critical tasks. Recently, it has been demonstrated that the micropipe defect density it is possible to reduce using the LPE process. It was found that the SiC epitaxial layers grown by LPE has the lower deep trap density in comparing with SiC epitaxial layers grown by CVD method. The objective of this research is to fabricate 4H-SiC pn diode using LPE method for high power application.

4H-SiC pn diode consisted from four epitaxial layers was grown by LPE method. First, a n<sup>+</sup>-layer was grown. It serves as the layer for closing micropipe defects that usually exist on commercial substrates. The n<sup>+</sup>-layer was deposited on (0001)Si face of the commercial 8<sup>0</sup>-off axis 4H-SiC substrates. The thickness of the n<sup>+</sup>-layer was about 10 μm. An undoped n<sub>0</sub>-layer was deposited on the n<sup>+</sup>-layer. The thickness of n<sub>0</sub>-layer was found to be 10-15 μm. N<sub>d</sub>-N<sub>a</sub> concentration in this layer was determined to be  $(9 \times 10^{15} \div 3 \times 10^{16}) \text{ cm}^{-3}$  for different samples. Al doped and Al heavily doped epitaxial layers were grown on n<sub>0</sub>-layer in that order. The thickness of Al doped layers was (1.0÷1.5) and (2.0÷2.5) micron for p<sup>+</sup>-layer and p-layer, respectively. N<sub>a</sub>-N<sub>d</sub> concentration in the p-layer was found to be  $(3 \div 6) \times 10^{18} \text{ cm}^{-3}$ . The N<sub>Al</sub> concentration in the p<sup>+</sup>-layer was determined using SIMS technique to be  $3 \times 10^{19} - 2 \times 10^{20} \text{ cm}^{-3}$ .

Low resistivity ohmic contacts to the both n- and p<sup>+</sup>-sides of the diode have been formed. An AlSi(2%)Ti(0.15%) alloy has been used as a p-type contact to the LPE 4H-SiC layer. The metal film with a thickness of 100 nm was deposited by an e-beam evaporation in vacuum of  $1 \times 10^{-6}$  torr. The AlSiTi contact was formed in a resistance furnace in an argon atmosphere at 900 °C. After annealing a reproducible contact resistivity of  $8 \times 10^{-5} \Omega \cdot \text{cm}^2$  has been measured. After the contact formation Au was deposited as a top layer. The ohmic contact to n-side was formed using Ni. A 100 nm thick film was also deposited by e-beam evaporation at the same conditions. The annealing has been performed at temperature of 950 °C and a contact resistivity of  $5 \times 10^{-5} \Omega \cdot \text{cm}^2$  has been obtained. After the ohmic properties formation an additional contact film consisted of subsequently evaporated Ti/Pt/Au layers was deposited to improve the backside metallization. The thermal stability study of the both contact types established that they were

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stable during the long time ageing at a temperature of 500 °C in nitrogen and in operating temperatures up to 450 °C in air.

The diode chip was attached to the gold-plated MoCu-base plate of the ceramic package using a high temperature eutectic Au(88%)-Si(12%) alloy. The contact pads on the diode top side were connected to the package lead by a gold wire. The electrical measurements were made up to 300 °C without degradation of the packaged diode.

The forward I-V characteristics measured at high current density up to  $1.5 \times 10^3$  A/cm<sup>2</sup> were studied at different temperature. The reverse I-V characteristics showed an abrupt breakdown at voltage about 500 V. It was found that the breakdown electrical field for the pn junction was  $\sim 1.3 \times 10^6$  V/cm. The C-V measurements were performed at different test frequencies of 10 kHz and 1 MHz. The impurity concentration Nd-Na was uniform and did not depend on test frequencies indicating on low concentration of deep traps in n<sub>0</sub>-layer. The C-V data indicate an abrupt pn junction. The value of built-in potential was determined to be about 3.0 eV that is close to theoretical value for 4H-SiC pn structure doped with nitrogen and aluminum.

Electrical characteristics of 4H-SiC pn diodes will be reported in detail.

### **Acknowledgements**

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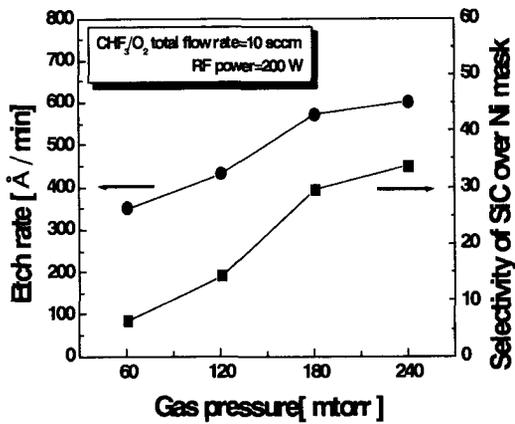
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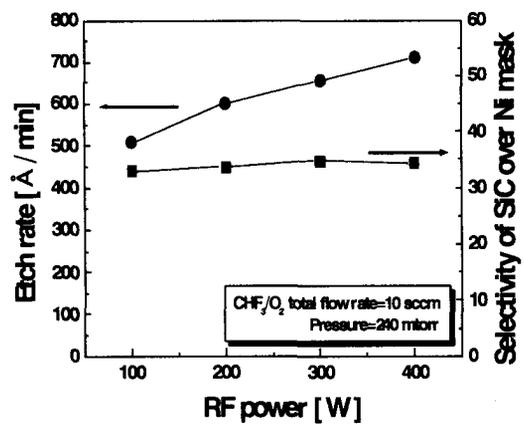
**Reactive Ion Etching Process of 4H-SiC Using the CHF<sub>3</sub>/O<sub>2</sub> mixture with a Post O<sub>2</sub> Plasma Etching Process**Soo Chang Kang and Moo Whan ShinSemiconductor Materials/Device Lab  
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There are several reports on the RIE (Reactive Ion Etching) process of SiC wafers using the CHF<sub>3</sub> as a source gas with additional H<sub>2</sub> or O<sub>2</sub> gas for the improvement of etching characteristics. It is known that the addition of H<sub>2</sub> gas in the CHF<sub>3</sub> can significantly reduce the amount of residues on the surface of etched SiC. However, the etching rate of the processing is known to be relatively low. When O<sub>2</sub> gas is employed instead of H<sub>2</sub> gas with CHF<sub>3</sub>, the etching rate can be enhanced due to a selective etching of C component in the SiC, but the surface roughness of the etched surface is known to increase due to the formation of residues. In this paper, we report on the RIE etching process of 4H-SiC wafer using the CHF<sub>3</sub>/O<sub>2</sub> mixture with a consecutive O<sub>2</sub> plasma etching process. It was found out that the etching rate is enhanced by the addition of O<sub>2</sub> gas into CHF<sub>3</sub>, while the surface roughness is significantly improved by the post O<sub>2</sub> plasma etching. SiC wafers with an n-type epitaxial layer grown on highly doped n-type 4H-SiC substrate were used for the RIE process. The etching rate for the RIE etching using the CHF<sub>3</sub>/O<sub>2</sub> mixture was found to increase from 500 Å/min to 710 Å/min when the RF power was increased from 100 W to 400 W (Fig.1(a)). The etching rate is also increased from 350 Å/min to 600 Å/min when the gas pressure is increased from 60 to 240 mtorr at the RF power of 240 W (Fig.1(b)). The surface roughness of the 4H-SiC after the RIE with the CHF<sub>3</sub>/O<sub>2</sub> mixture without the post O<sub>2</sub> plasma etching was measured to be about 5.0 Å. The roughness was found out to be decreased down to about 1.2 Å when the sample was accompanied with the O<sub>2</sub> plasma etching after the RIE with the CHF<sub>3</sub>/O<sub>2</sub> mixture (Figure 2). The SEM (Scanning Electron Microscopy) analysis showed no evidence of formation of a trench which is generally induced by the excessive flow of ions reflected from the etched surface. It was concluded that the RIE etching process using the CHF<sub>3</sub>/O<sub>2</sub> mixture with a consecutive O<sub>2</sub> plasma etching process results in promising etching characteristics for the fabrication of SiC devices.

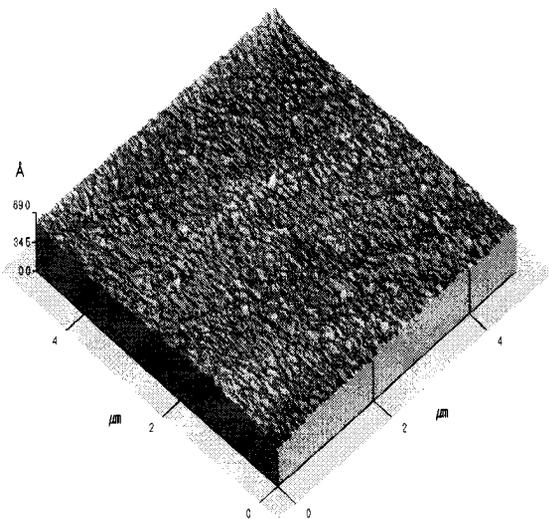


(a)

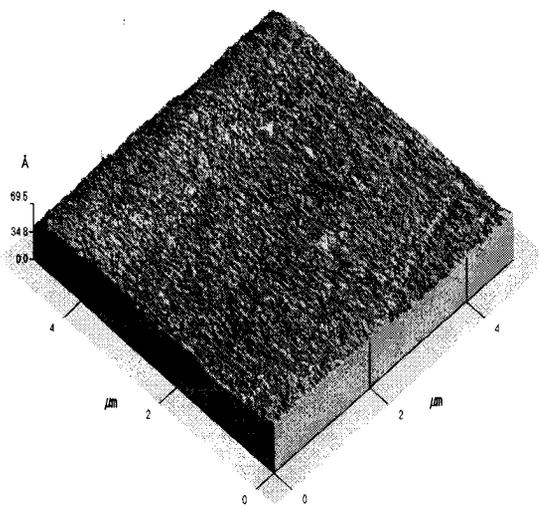


(b)

Fig. 1 The RIE etching rate of 4H-SiC using the  $\text{CHF}_3/\text{O}_2$  mixture etching as functions of a) gas pressure and b) RF power.



(a)



(b)

Fig. 2 AFM of the surfaces of 4H-SiC etched by  $\text{CHF}_3/\text{O}_2$  mixture a) without the post  $\text{O}_2$  plasma process ( RMS roughness of 5.0 Å) and b) with the post  $\text{O}_2$  plasma process ( RMS roughness of 1.2 Å).

#### ACKNOWLEDGEMENT

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