

Poster Session II

Liquid Phase Epitaxial Growth of Highly Al Doped p-type Contact Layers for SiC Devices and Resulted Ohmic Contacts

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Liquid Phase Epitaxial growth of highly Al doped p-type contact layers for SiC devices and resulted Ohmic contacts.

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High Al doping level in Silicon Carbide layers is strongly desirable for most of SiC bipolar devices. Contact resistivity of such regions becomes a limiting factor for most types of SiC based power and microwave power devices (p-i-n diodes, IMPATT-diodes, microwave limiters, BJTs *etc.*).

Commonly used chemical vapor deposition (CVD) technique is not able to provide aluminum atomic doping concentration sufficient for reproducible fabrication of ohmic contacts with specific contact resistance lower than $10^{-4} \Omega \text{ cm}^2$. Ion implantation can provide rather high Al atomic concentration, but the defects produced by implantation require post implantation high temperature anneal and can cause the additional problems for devices fabrication and operation.

In this paper we report on SiC doping with Al during liquid phase epitaxy (LPE) of thin (0.3-0.4 μm) 6H- and 4H-SiC layers for diode structures with a smooth mirror-like surface. Al doped 6H-SiC epitaxial layers were grown by LPE on the 6H-SiC (0001) 3.2° and 4H-SiC 8° off-axis substrates. We also grew p^+ -6H-SiC and p^+ -4H-SiC layers on commercial p-n epitaxial structures. Growth was performed in a vertical dipping version of LPE reactor.

We achieved significant improvement of surface morphology for thin layers doped with Al by decreasing of growth temperature. Smooth layers with Al atomic concentration over $2 \times 10^{20} \text{ sm}^{-3}$ (as measured by secondary ion mass spectroscopy) were grown. Thickness of p^+ -layers was measured using scanning electron microscopy.

Ti-Al alloy was deposited to form ohmic contacts both by sputtering and e-beam evaporation. Test structures were formed for transmission line (TLM) resistivity measurements. Contact layers were annealed in vacuum at high temperature. TLM measurements show that reproducible Ohmic contacts with contact resistivity in low $10^{-5} \Omega \times \text{cm}^2$ range were fabricated. For the best contacts, $10^{-6} \Omega \times \text{cm}^2$ level was achieved.

Highly doped p^+ -SiC layers were applied to fabricate SiC diodes with low on-state resistance. In this case p^+ -SiC LPE layers were grown on the top of commercial pn epitaxial structures. Back contacts for diodes were formed by nickel evaporation and subsequent anneal in Ar flow. Diode mesa-structures of various sizes were formed by reactive ion etching in radio frequency glow discharge SF_6 plasma. We protected the top contacts against etching by the aligned Ni masks using lift-off lithography. To improve on-state resistivity of diodes back and topside contacts were enforced with gold. Resulted

in diodes show low on-state resistivity of $\sim 8 \times 10^{-4} \Omega \times \text{cm}^2$. This value exceeds the level of contact resistivity to p-layers. The resistivity is possibly limited by the substrate and/or base n-layer resistance.

We may conclude that heavily aluminum doped p^+ - SiC layers and resulted record low resistivity Ohmic contacts to p-type SiC have been demonstrated and implemented for diodes fabrication.

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Abstract

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Homoepitaxial growth of 4H-SiC on porous substrate by chemical vapor deposition using bis-trimethylsilylmethane precursor

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Dislocations and micropipes in SiC wafers still limit the performance of SiC electronic devices such as MESFET, MOSFET and SBD. Therefore, it is prerequisite to reduce the dislocation in order to exploit high performance SiC electronic devices. Usage of porous silicon carbide (PSC) is one of the ways to reduce dislocations during epitaxial growth.

In this paper, 4H-SiC films were grown on 8° off-axis porous 4H-SiC (0001) by chemical vapor deposition using a single source material, bis-trimethylsilylmethane (BTMSM). The flow rate of the carrier gas H₂, which flows through liquid BTMSM source, and growth temperature were varied from 10 to 30 sccm and from 820 to 1390°C, respectively. The grown films were examined by atomic force microscopy (AFM), scanning electron microscopy (SEM), electron back scattering diffraction (EBSD), high resolution x-ray diffractometry (HRXRD) and transmission electron microscopy (TEM). The roughness of as-received substrate (1.2nm) was improved to 0.5 nm by hydrogen etching for 10 min at 1500°C. As the growth temperature and the flow rate of source material, BTMSM, increase, the rms roughness of the thin film was decreased, indicating that the growth follows the so-called step-controlled epitaxy model. It was found that the flow rate of source material,

BTMSM is critical growth parameter to polytype formation of thin film. At higher flow rate (>20sccm), parasitic 3C-SiC polytype was included in the grown film. The (111) Bragg spot position of 3C-SiC on PSC is displaced by $1.2 \times 10^{-3} \text{ nm}^{-1}$ along the Q_z -axis with respect to the (0004) Bragg spot position of 4H-SiC in reciprocal space, while the (111) Bragg spot position of 3C-SiC on the standard 8° off-axis 4H-SiC substrate is displaced by $3.4 \times 10^{-3} \text{ nm}^{-1}$. The result suggests that 3C-SiC on PSC is more strained than that on standard substrate. This difference might be ascribed to the porosity of the substrate. However, at low flow rate (10sccm), homoepitaxial 4H-SiC films without parasitic 3C-SiC was grown. Although the FWHM of (0004) Bragg spot of the epilayer grown below 990°C is larger than that of substrate, FWHM of thin films above 1200°C is smaller than that of substrate. Monocrystalline 4H-SiC films were grown even at the extremely low temperature of 820°C . At optimum growth condition, the density of dislocation in the epilayer was reduced compared to that of typical commercial substrate.

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SiO₂ as oxygen source for the chemical vapor transport of SiC

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Recently, the sublimation epitaxy method has attracted attention in order to grow thick homoepitaxial SiC layers at low cost. This technique is a simple transposition to lower temperatures of the modify Lely-process used for SiC boules. However, in most cases the temperature is higher than 1800°C [1,2]. Reduction of the growth temperature could help solving some problems such as thermal stress, defect generation or graphitisation of the source. However, the lowering of the temperature is critical for the growth rate because of the low sublimation rate of SiC. The addition of a chemical agent X in the growth chamber could assist the vaporization of SiC by forming SiX and CX gaseous species. In this case, the method should be called Chemical Vapor Transport (CVT).

In a first step, a thermodynamics study based on the total Gibbs free energy minimization was performed in order to evaluate the potential of oxygen as a transporting agent for SiC. The temperature ranged from 1500 K to 2200 K and isochore conditions were used. After fixing the initial Si, C and O contents, the equilibrium partial pressures were calculated at one temperature and inserted again for calculation at a different (lower or higher) temperature to simulate a thermal gradient. SiO and CO were found to be the main gaseous species forming. It is shown that SiC can be transported on a wide range of initial reactant content or temperatures without the co-formation of SiO₂, Si or C.

In a second step, the CVT of SiC was carried out in a sublimation like graphite reactor with an internal thermal gradient of 7 K/mm. The SiC seeds were 8° off oriented (0001) 4H-SiC substrates. The use of SiO₂ powder as the oxygen source is advantageous on many points : 1) it is easy to handle; 2) it can be introduced in the reactor in a precise amount; 3) the intimate mixing of both SiC and SiO₂ powders ensures an effective interaction of oxygen with the SiC source.

CVT experiments with SiO₂ addition to the source were compared to pure sublimation experiments performed with identical argon pressure and temperature. It was found that the addition of SiO₂ in the source enlarges the conditions of pressure and temperature for the SiC epitaxial growth. Indeed, epilayers could be grown at lower temperature or higher pressure than the ones required for sublimation epitaxy. It was also observed that, when SiO₂ was added, the SiC powder never showed any evidence of graphitisation after experiment. The effect of the SiC/SiO₂ molar ratio in the source has been studied in order to optimize the growth conditions and the quality of the epilayers.

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Surface Morphology of SiC Epitaxial Layers Grown by Vertical Hot Wall Type CVD

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Control of the surface morphologies of SiC epitaxial films is important for electronic device fabrication, particularly for high-frequency applications.[1] In this study, we investigate the surface morphology of epitaxial layers etched in the hydrogen annealing under the several conditions.

The vertical hot wall type CVD system was used to grow the epitaxial layers of SiC in this study.[2] The growth temperature and pressure were 1600°C and 90kPa, respectively. The flow rate of H₂ carrier gas was 2slm. The flow rates of SiH₄ and C₃H₈ were 3sccm and 2sccm, respectively. The surface morphologies of epitaxial layers were minutely evaluated by laser microscopy and atomic force microscopy (AFM). The epitaxial layers on the 6H- and 4H-SiC(0001)Si substrates with 3.5° and 8° off-angles, respectively, resulted in the formation of the macro-steps. Size of the steps was observed as 600-1300nm in width and 10-30nm in height on the 6H-SiC. The terrace width (700-2000nm) and step height (10-50nm) on 4H-SiC were larger than those on 6H-SiC.

The epitaxial films with macro-steps on 6H- and 4H-SiC were etched in the atmosphere of hydrogen. The etching experiments were performed in the CVD system described above. The substrate temperature, H₂-flow rate, and H₂ pressure were varied within 1400-1600°C, 0.5-2.0slm, and 3-90kPa, respectively. The etching rates were varied from 0.5μm/h to 30μm/h with the etching conditions. It is confirmed that the etching rate increases with increasing substrate temperature and H₂-flow rate, and is varied inversely with the pressure.

After etching in H₂ at the pressure of 90kPa, it is observed that the surface morphologies keep the same with macro-steps mentioned above. Under atmospheric pressure, it is considered that the etching reactions mainly occur on the terraces of the macro-steps, so that the width of wide terrace becomes wider as the reactions proceed. In low-pressure H₂ atmosphere, it is clarified that the step height is drastically reduced after hydrogen etching. After 30min. etching at 1500°C under the pressure of 6kPa, the average surface roughness of 6H- and 4H-SiC measured by AFM become 3nm and 5nm, respectively. There are little effects of substrate temperature and H₂-flow rate to the surface morphologies. These results suggest that the low-pressure H₂ atmosphere accelerates the etching reactions on the kink of the bunched terraces to reduce the step height and to proceed the effective flattening of the bunched surfaces.

In conclusion, the surface morphology of SiC epitaxial layers etched by hydrogen annealing has been investigated by laser microscopy and AFM. The step height of the bunched surfaces of epitaxial layers drastically reduces after hydrogen etching at low-pressure atmosphere.

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In situ RHEED analysis of the Ge induced surface reconstructions on 6H-SiC(0001)P. Weih, Th. Stauden, J. Pezoldt

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Germanium has attracted an interest in the SiC technology. Three fields of applications are in the focus of research. Firstly, Ge can be used to improve the heteroepitaxial growth of SiC on Si [1,2]. Secondly, Ge can act as a surfactant during the epitaxy of SiC [3] and more recently the formation of germanium nanocrystals as potential candidates for optoelectronic application have been studied [4]. For all this application it is important to have a detailed knowledge about the structural evolution during early stages of Ge deposition to control the surface structure and composition, but only few reports are available on Ge induced surface structure [4]. In this paper, real time in situ reflection high energy electron diffraction (RHEED) studies of the surface structure evolution during Ge deposition on differently prepared SiC(0001) surfaces will be presented.

Cree silicon face 6H-SiC (0001) 3.5° off-oriented towards $[11\bar{2}0]$ were used as substrates. The substrates were cleaned in situ in a hydrogen plasma and by heating in a Si flux to get definite reconstructions of (3×3) -Si, $(\sqrt{3}\times\sqrt{3})$ -Si and $(\sqrt{3}\times\sqrt{3})$ -C. Subsequently, these well prepared surface reconstruction were subjected to a Ge flux of 0.003 ML s^{-1} with respect to the SiC surface. The deposited Ge amount was in the range between 0.1 and 8 ML. The investigations were carried out at substrate temperatures between 250°C and 900°C .

Independent on the prepared surface reconstruction we observed the formation of a Ge wetting layer. The thickness of these layers was in the range of 1 to 3 ML in dependence of the initial surface reconstruction and substrate temperature. These wetting layers were stable against cluster formation at substrate temperatures below 480°C and Ge coverages below approximately 0.7 ML on (3×3) -Si, 1.4 ML on $(\sqrt{3}\times\sqrt{3})$ -Si and 1.7 ML $(\sqrt{3}\times\sqrt{3})$ -C reconstructed surfaces.

The following possible transition schemes were observed:

(3×3) -Si reconstructed surface: (3×3) -Si \rightarrow (3×3) -Ge \rightarrow (4×4) -Ge \rightarrow cluster formation
 $(\sqrt{3}\times\sqrt{3})$ -Si reconstructed surface: $(\sqrt{3}\times\sqrt{3})$ -Si \rightarrow (2×1) or (2×2) -Ge \rightarrow (4×4) -Ge \rightarrow cluster formation
 $(\sqrt{3}\times\sqrt{3})$ -C reconstructed surface: $(\sqrt{3}\times\sqrt{3})$ -C \rightarrow $(\sqrt{3}\times\sqrt{3})$ -Ge \rightarrow (2×1) or (2×2) -Ge \rightarrow (4×4) -Ge \rightarrow cluster formation

A detailed analysis of the RHEED time dependent RHEED intensity behaviour will be presented.

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In situ etching of 4H SiC in H₂ with addition of HCl for epitaxial CVD growth

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Introduction Good surface morphology of the epitaxial layers is a basic requirement for both the processing and the performance of the devices. To improve the surface morphology, one important factor is the substrate surface condition prior to the growth. Etching of the SiC substrate before the CVD growth in pure hydrogen or in hydrogen with addition of either a hydrocarbon or hydrogen chloride (HCl) has been used to improve the surface quality of the epilayers [1, 2]. In this paper we investigate the etching mechanism of 4H SiC in H₂ with addition of HCl and the role of HCl in the etching.

Experimental The in situ etching and the subsequent CVD growth runs were performed in a horizontal hot-wall reactor, similar to the one described in [3]. A SiC-coated graphite susceptor was used and the small substrate pieces were placed on a poly-SiC plate lying on the susceptor floor. A small amount of hydrogen chloride (< 0.03% in volume) together with the hydrogen carrier gas was introduced during the etching. Silane (SiH₄) and ethylene (C₂H₄) were used as precursors for the subsequent growth. A 4H SiC epilayer (8° off-oriented towards the <11 $\bar{2}$ 0> direction), was etched and the thickness was measured before and after etching using Fourier Transformed Infrared Spectrometry (FTIR), and the etch rate was thereby obtained. The surface morphology of the etched substrates was examined in an optical microscope with Normaski contrast. The surface roughness profiling was conducted using light interference with a WYKO instrument. KOH etch of the SiC surface was conducted at ~ 500 °C for 5 - 15 s.

Results As shown in Fig. 1, the etch rate increases rapidly with increasing temperature. The activation energy is above 110 kcal/mol at 20 mbar (open squares), and decreases to around 72 kcal/mol at 100 mbar (black squares). The high activation energy values suggest that the limiting mechanism for the etching may be related to either the carbon removal through the reaction with hydrogen or the Si evaporation process. The pressure also has an impact on the etch rate, as indicated in Fig. 2. The etch rate decreases steeply with increasing pressure below a pressure of 100 mbar. Above this pressure, the etch rate further decreases very slowly and almost levels off after 600 mbar. Without addition of HCl (closed circles in Fig. 2), the etch rate is considerably lower at low pressures, but only slightly reduced in the high pressure range.

Etching in hydrogen with addition of HCl under proper conditions has shown to significantly improve the subsequently grown epilayer morphology. As illustrated in Fig. 3a, the epilayer grown without pre-growth etch displays a large density of pit-like defects, whereas on the epilayers grown after etch (Fig. 3b) the amount of the pit-like defects has been reduced considerably, with only a few half-moon defects encountered on the surface. The KOH etching of these epilayers shows that the pit-like defects mainly originate from dislocations, whereas the half-moon defects do not display etch pits after the KOH etch.

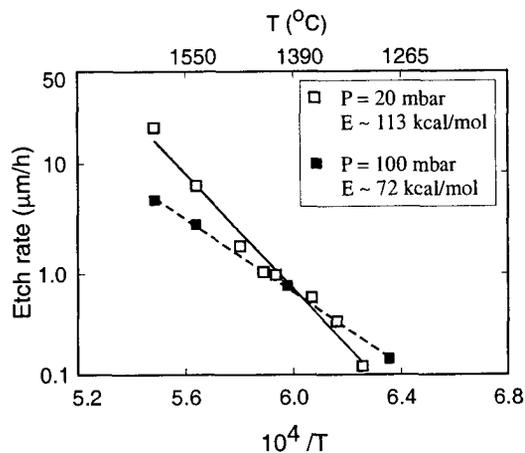


Fig. 1, Etch rate dependence on temperature at 20 mbar and 100 mbar, respectively, with 60 //min H₂ flow and 20 ml/min HCl flow.

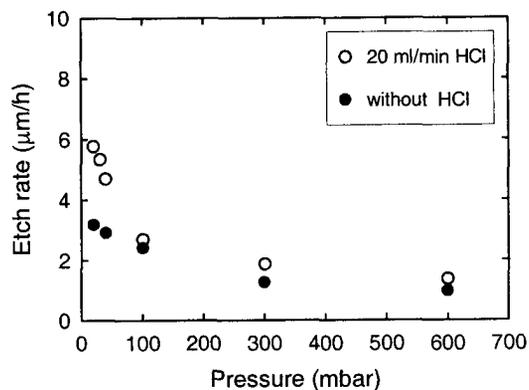
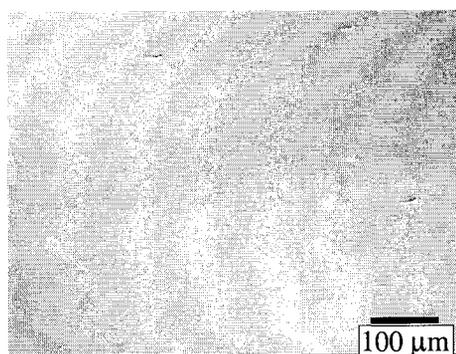
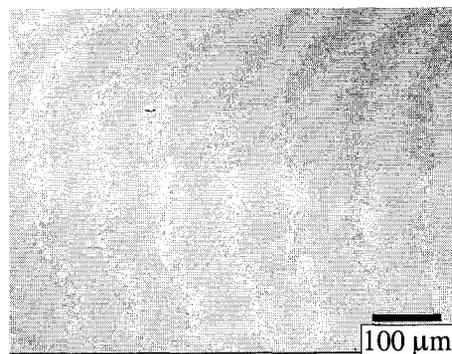


Fig. 2, Etch rate dependence on the pressure with 60 //min H₂ flow at 1500 °C.



(a)



(b)

Fig. 3, Normaski micrographs of: a) 17.5 μm epilayer grown for 3 h with no pre-growth etch; b). 9.5 μm epilayer grown for 2h after proper in situ etch in hydrogen with addition of HCl.

The surface roughness of the as-etched substrates has been measured systematically by the WYKO instrument. A too high etch temperature (> 1650 °C) is shown to give rise to rough surface, whereas a low etch pressure (around 40 mbar) results in very smooth surface.

To summarise, the pre-growth etching of SiC in hydrogen with addition of HCl has shown to effectively suppress the formation of dislocation related morphological defects after the epitaxial growth. The etch rate dependence on the etch parameters has been studied to understand the etching mechanism involving HCl.

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Fabrication of α -SiC hetero-epitaxial films by YAG-PLAD method

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I. Introduction

Silicon carbides (SiC), especially the high-temperature stable ones (such as 4H and 6H α -SiC) with hexagonal crystal structures are strongly expected to be the next-generation semiconductors, that are applicable for high power, high voltage, high temperature, and high frequency devices, since they have a wider band gap (3.0-3.2eV) than the low temperature type (β -SiC; 2.2eV), and have high melting point (m.p.>2400°C), large thermal conductivity, and large resistance for electric breakage. However, the high m.p. makes it difficult to prepare single crystals and needs complex processing for preparation of the devices, such as ion implantation and thermal annealing at high temperatures around 1600°C. Many trials were made for preparing SiC hetero-epitaxial films, however, they have failed except for β -SiC hetero-epitaxial growth by MBE techniques. Here we report the first preparation of hetero-epitaxial films of α -SiC at low temperatures around 1150°C by pulsed laser ablation-deposition (PLAD).

II. Experimental

The fabrication of α -SiC films have been studied by PLAD technique using the 4th harmonic of Nd:YAG laser (266nm). We tried the film growth using 6H α -SiC targets and seven kinds of single crystal substrates: Si(111), Si(110), Si(100), sapphire:Al₂O₃(0001), Mg(100), SrTiO₃(100), and LSAT(100). The epitaxial growth has occurred only on the Si(111) and sapphire(0001) planes.

III. Results and Discussions

Figures 1a, 1b, and 1c show the infrared absorption spectra of the films simultaneously fabricated on Si(111), Si(110), and Si(100) substrates in the following PLAD conditions: the substrate temperature =1150 °C, laser energy = 50 mJ/pulse, fluence = 5 J/cm²/pulse, pulse frequency = 10 Hz, and vacuum pressure = 1x10⁻⁷ Pa. Every spectrum shows absorption of Si-C stretching vibration mode ν (Si-C) alone, unequivocally indicating formation of SiC thin films. The absorption frequency was 786±3 cm⁻¹ for the film fabricated on Si(111). The X ray diffraction (XRD) pattern of the film is shown in Fig.2a. It is composed of SiC(0006) and SiC(00012) XRD lines expect for diffraction lines from the substrate, definitely indicating formation of c-axis oriented film of α -SiC on Si(111). On the other hand, the XRD patterns for other films prepared on Si(110) and Si(100) show XRD lines only from the substrates as shown in Figs.2b and 2c. These results along with those from the infrared spectra suggest formation of SiC polycrystalline films.

The crystallinity of the films was investigated by reflection high energy electron diffraction (RHEED). Figures 3a and 3b show RHEED images observed for the film fabricated on Si(111). Figure 3c is an image measured for film on Si(110), which did not change by rotation of the film. It is of Debye-Scherrer (ring-type) pattern, that is characteristic of polycrystalline samples. The film fabricated on Si(100) also gave essentially the same ring pattern. Thus it was confirmed that polycrystalline SiC films were formed on Si(110) and Si(100) planes, which have no C₆ symmetry (having C₂ and C₄). On the other hand, the film on Si(111) substrate shows symmetric streak patterns which is characteristic of epitaxial growth of α -SiC. Two spectra in

Figs. 3a and 3b are observed at the film-orientations that differ by 30° in each other and observed at an interval of 60° . This is evidence for the film having C_6 symmetry in the plane. The separation between streak lines is proportional to the reciprocal of the lattice constants. The ratio of the separations between the streak patterns in Fig.3a and Fig.3b was $\sim 1.76 \pm 0.05$, which agrees with the value of $3^{1/2} = 1.73$ expected for the lattice with C_6 symmetry. These results along with those from XRD strongly indicate that the epitaxial film of α -SiC having hexagonal structure is fabricated on Si(111), rather than β -SiC with cubic structure. The lattice parameters of the film were estimated to be $a = 3.09 \pm 0.04$, $c = 15.08 \pm 0.01 \text{ \AA}$ from the RHEED and XRD measurements, in good agreement with the reported values for 6H α -SiC (3.07 and 15.08 \AA). The IR absorption frequency $\nu(\text{Si-C}) = 786 \pm 3 \text{ cm}^{-1}$ observed for film prepared on Si(111) agrees with the reported value for α -SiC (789 cm^{-1}) rather than β -SiC (798 cm^{-1}), supporting the assignment to α -SiC film.

The epitaxial growth of SiC occurred only on Si(111) and $\text{Al}_2\text{O}_3(0001)$ which have the same C_6 symmetry as α -SiC, implying that symmetry matching is an important factor for the growth. The present success of low-temperature preparation of α -SiC film by PLAD may provide a new device processing for production of p and n-type semiconductors.

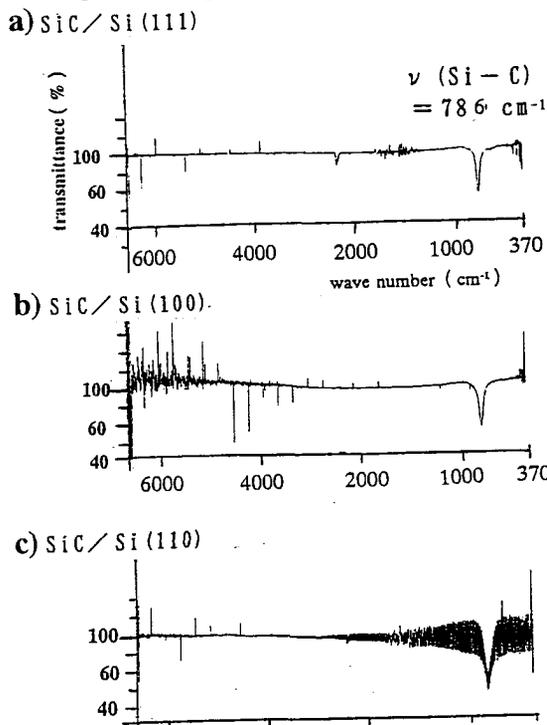


Fig.1 IR spectra observed for SiC films fabricated on Si(111), Si(100) and Si(110) substrates.

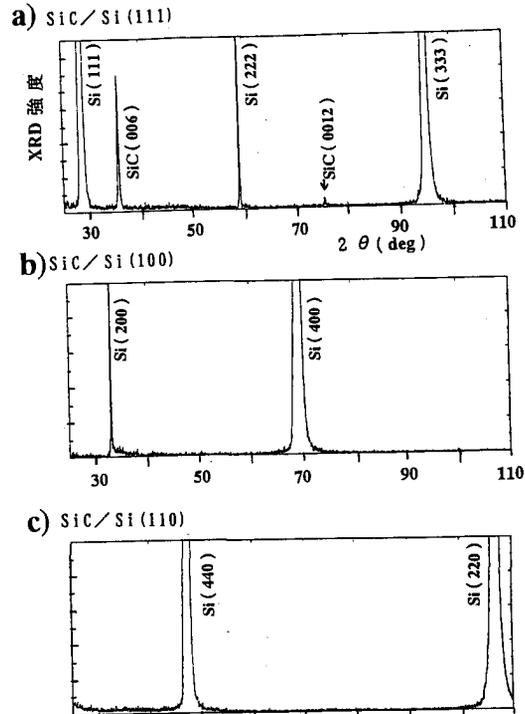


Fig.2 XRD patterns observed for SiC films on Si(111), Si(100) and Si(110) substrates.

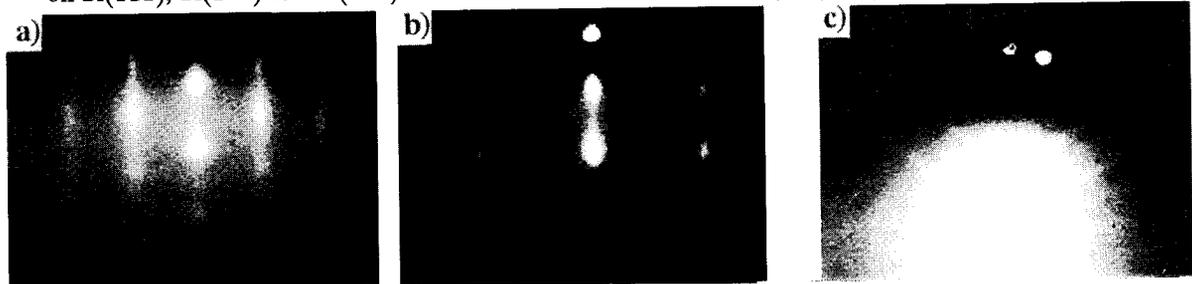


Fig.3 RHEED images observed at $\langle 10\bar{1}0 \rangle$ (a) and $\langle 21\bar{3}0 \rangle$ (b) film-orientations for the SiC film fabricated on Si(111) and image (c) for the film prepared on a Si(110) substrate.

Comparativ Study of heteroepitaxially and homoepitaxially Grown 3C-SiC Films

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Cubic silicon carbide (3C-SiC) is a promising candidate to overcome the device limit due to intrinsic silicon properties in the fields of, high power devices, high temperature devices and high radiation tolerant devices. Moreover, it may be a suitable substrate for the growth of cubic IV-nitrides. However, 3C-SiC crystals are not commercially available now. It is important to develop higher device grade 3C-SiC crystals for the realization of 3C-SiC devices.

This paper presents the results of two growth processes of 3C-SiC epilayers, heteroepitaxial growth of 3C-SiC on Si (100) substrates and homoepitaxial growth on 3C-SiC substrates. The heteroepitaxial growth was carried out by low pressure CVD method using a vertical cold wall quartz reactor with two zone RF induction heating systems. Silicon (001) on-axis wafers, 50 mm square were used as substrates. Typical heteroepitaxial growth conditions were as follows; growth temperature: $\sim 1250^{\circ}\text{C}$, growth pressure: 30 Torr, H_2 carrier gas flow rate: 8 slm, SiH_4 gas flow rate: 0.8 sccm, and C_3H_8 gas flow rate: 0.4 sccm. The growth rates were around $2 \mu\text{m/hr}$. After 50 hours growth, the silicon substrates were etched off using $\text{HF}+\text{HNO}_3$ solution to fabricate free standing 3C-SiC films of $100 \mu\text{m}$ in thickness. These 3C-SiC thick films were used as substrates for the homoepitaxial growth. The homoepitaxial growth was performed by low pressure CVD method using another vertical cold wall quartz reactor, under the conditions; the growth temperature: 1530°C , the growth pressure: 47 Torr, and H_2 , SiH_4 , C_3H_8 reaction gas flow rates: 10slm, 30 sccm, 8 sccm, respectively. The growth rate were around $10 \mu\text{m/hr}$. 1) The surface morphologies of these epilayers were observed using a Nomalski optical microscope and an AFM. The crystalinity of these epilayers were evaluated by XRD and PL spectroscopy.

The morphologies of the grown surfaces of the heteroepitaxial layers were rough, because of the formation of macro steps and protrusions caused by stacking fault. 2) as shown in Figure 1. While, the surface morphology of the back side of heteroepitaxial layers (interface with Si substrates) were very smooth as same as those of Si substrates. From this reason, we used the back side surface of the heteroepilayer as these substrates for the homoepitaxial growth, though the crystalinity was not so good compared with that of the grown surfaces. The typical values of the FWHM of XRD- ω scan rocking curve of the substrates were around 1200 arcsec.. After homoepitaxial growth of $\sim 100 \mu\text{m}$ in thickness,

the FWHM reduced to around 150 arcsec. The surface of the homoepilayers were fairly smooth as shown in Fig. 2. The AFM image of the surfaces is shown in Fig.3. Step bunchings, the height of which are 1~2 nm, can be seen in this figure, and the root mean square of the surface roughness were around 0.4 nm ($10\ \mu\text{m} \times 10\ \mu\text{m}$). Figure. 4 shows the PL spectra of the homoepitaxial layer. A free exciton peak of 3C-SiC and N dopant originated peaks can be seen. The free exciton peak was not observed for the heteroepilayers. The improvements in the crystallinity, the surface morphology and the luminescent properties suggest the possibility of the growth of 3C-SiC crystals good for the device fabrications.

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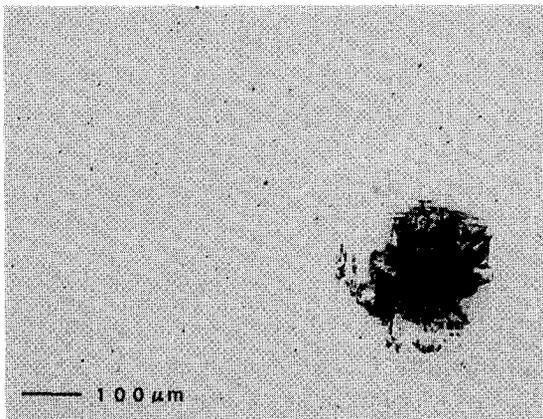


Fig. 1 Nomalski microscope image of a heteroepilayer surface.

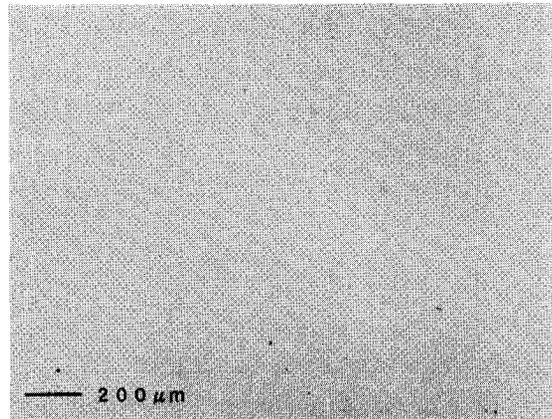


Fig. 2 Nomalski microscope image of a homoepilayer surface.

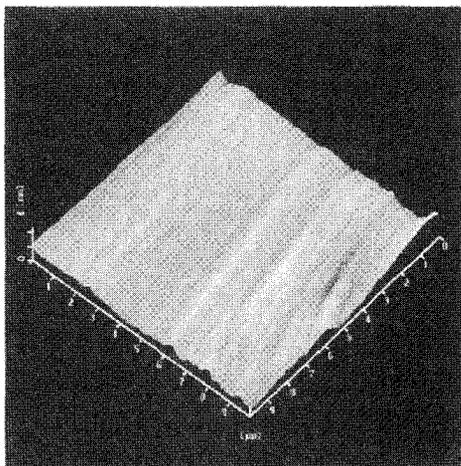


Fig.3 AFM image of a homoepilayer surface.

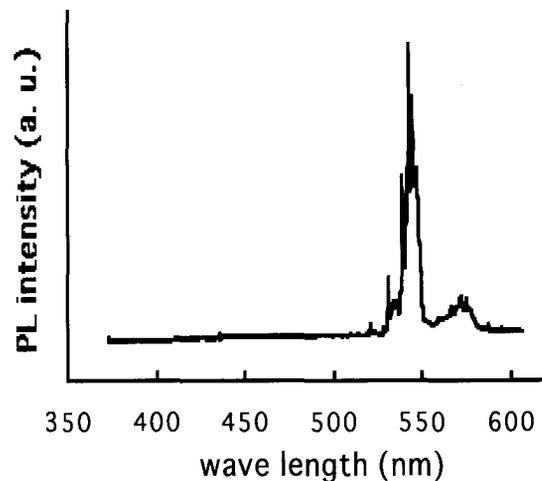


Fig. 4 Photoluminescence spectrum from a homoepilayer

In Situ* Doping of 3C-SiC Grown on (0001) Sapphire Substrates by LPCVD

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3C-SiC is a promising semiconductor material for high temperature and/or high power devices. The growth of 3C-SiC on sapphire or AlN substrates is quite interesting from the point view of semiconductor-on-insulator (SOI) structures. For most high-power applications, an insulating or semi-insulating substrate supporting the device is necessary to reduce parasitic effects and to increase the maximum power capabilities of the device. On the other hand, it is important to control impurity incorporation into epilayers for device applications. In this paper, we report the *in situ* doping of 3C-SiC grown on C-face (0001) sapphire substrates by LPCVD.

The heteroepitaxial growth of SiC on sapphire substrates has been performed with a supply of SiH₄, C₂H₄, and H₂ at a pressure of 200 Torr. The nitrogen and boron incorporation was accomplished by introducing ammonia (NH₃) and diborane (B₂H₆) precursors, respectively, into gas mixtures. The undoped and nitrogen-doped 3C-SiC epilayers were grown on the nitridized sapphires, which were formed by supplying NH₃ to the heated sapphire substrate at temperature of 1100 °C for 10 minutes. The boron-doped 3C-SiC epilayers were grown on pure sapphire substrates. Surface morphologies were characterized by Nomarski differential interference contrast optical microscopy and scanning electron microscope (SEM).

Crystallinity of SiC on (0001) sapphire substrates was characterized using x-ray diffraction (XRD). X-ray diffraction measurements of undoped and nitrogen-doped SiC samples (shown in Fig. 1) show the presence of SiC (111) and (222) peaks at $2\theta=35.6^\circ$ and 75.4° , respectively. The absence of any other reflections corroborates that the SiC film is epitaxial and cubic (3C-) form mono-crystalline as reported previously. X-ray rocking curve data confirmed the crystalline nature of as-grown 3C-SiC films.

The incorporation of nitrogen and boron into grown 3C-SiC epilayers was measured by Auger electron microscopy (AES) and secondary-ion mass spectroscopy (SIMS). Fig. 2 shows that the nitrogen concentration for the samples made at 1400 °C with a NH₃ gas flow rate of 1 SCCM increased from 2% to 15% with increasing the Si/C ratio from 0.33 to 0.5. The carbon concentration decreased from about 35% to 24%, while the silicon concentration kept the same (about 60%). This result indicates that nitrogen substitutes for carbon in the SiC lattice and the nitrogen dopant concentration incorporated into the 3C-SiC epilayers increased by increasing the Si/C ratio.

Preliminary Hall measurements were made at room temperature on undoped, nitrogen-doped and boron-doped samples using the van der Pauw technique. Undoped

and nitrogen-doped 3C-SiC epilayers were n-type conduction, and boron-doped epilayers were p-type and probably heavily compensated. Three undoped 3C-SiC samples showed n-type electrical conductivity with mobilities of approximately 2-7 cm^2/Vs and $(N_d - N_a)$ of $1.3 \times 10^{18} \sim 4.7 \times 10^{18} \text{ cm}^{-3}$. Four nitrogen-doped 3C-SiC samples yielded values of 0.021 Ωcm to 0.0014 Ωcm for resistivity, 2-5 cm^2/Vs for the electron mobilities, and $2.5 \times 10^{20} \text{ cm}^{-3}$ to $2.7 \times 10^{21} \text{ cm}^{-3}$ for the electron carrier concentration. Four boron-doped 3C-SiC samples grown with diborane gas flow rate varied from 1.25 SCCM to 5 SCCM yielded values of 580 Ωcm to 7.7 Ωcm for resistivity, $1.7 \times 10^{16} \text{ cm}^{-3}$ to $1.3 \times 10^{17} \text{ cm}^{-3}$ for hole carrier concentration, and 3.1 to 7.7 cm^2/Vs for hole mobility.

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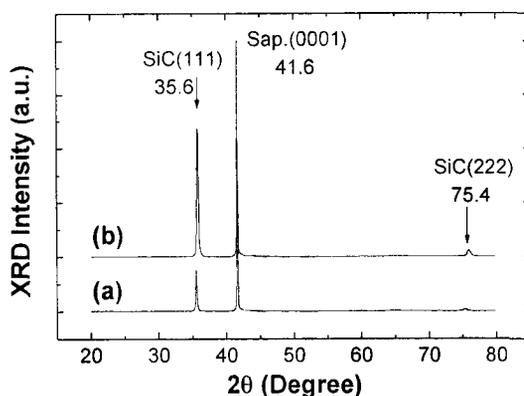


Fig. 1 X-ray diffraction patterns for (a) undoped and (b) nitrogen-doped 3C-SiC epilayers.

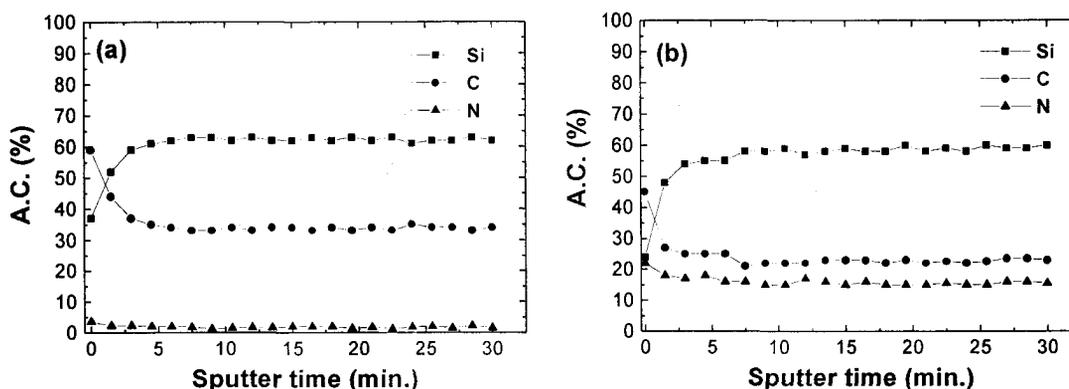


Fig. 2 Auger depth profile for N-doped 3C-SiC epilayers grown on nitridized sapphire substrates at 1400 °C with a Si/C ratio of (a) 0.33 and (b) 0.5. The ammonia gas flow rate was 1 SCCM.

SILICON CARBIDE BUFFER LAYERS FOR NITRIDE GROWTH ON Si

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Group III-nitride is one of the best candidate for UV laser-diodes and LEDs. Gallium nitride-based opto-electronic devices may possess high emission efficiency because of its electronic properties. In order to obtain high quality GaN crystalline films, the problem of finding an optimized substrate material must be solved. One possibility is to use sapphire with buffer layers because of the large lattice mismatch and thermal expansion mismatch between wurtzite GaN and sapphire. The reduction/annihilation of structural defects in GaN overlayers used as active layers is indeed a vital problem for device applications. The low lattice mismatch between SiC and GaN (~3 %) makes SiC a suitable substrate for GaN growth. However, this strategy is facing the problem of high cost of SiC wafers.

Among the different techniques which can smooth out the effect of host materials large lattice mismatch, the buffer layer technique has been widely used to assist heteroepitaxial growth. Thus one useful task is to use Si as substrate with SiC buffer layer. Large area Si wafers are indeed available with many advantages such as large area low cost, high surface quality and high conductivity. This option would also provide a route towards the integration of the group III-nitride technology into the silicon technology for which well-established processing methods exist.

However, when using this methodology, an important problem related to the lowering of residual stress existing at the SiC/Si interface must be solved since the crystalline quality of the SiC/Si interface and of the surface of the SiC buffer layer is a necessary condition to obtain GaN layers free of structural defects.

The carbonization of Si-substrate surfaces performed to grow SiC overlayers on Si generally introduces stresses at the SiC/Si interface because of host material physical properties differences: SiC and Si present indeed a disadvantage due to the large mismatches of their lattice constants and their thermal expansion coefficients respectively equal to 20 % and 8 %. Because of these mismatches and beyond layer critical thickness, extended defects, like for instance dislocations, can be favored from the formation energy point of view. However, these extended defects can not fully relax stresses introduced at the SiC/Si interface. The carbonization of clean Si surface using hydrocarbon radicals is generally performed at the early stage of the growth process. Gas source molecular beam epitaxy (GSMBE) experiments have shown that when one uses (CH₃)₂GeH₂ (DMGe) as carbon source, the morphology of the carbonized surface layer improves when compared with the one without Ge (carbon is then provided by hydrocarbon radicals from cracked -C₃H₈). The thickness of the smooth carbonized layer is ~ 40 Å with a Ge concentration showing a saturation around 0.4 %, and the purpose of using DMGe is to introduce a large size atom at the heterointerface.

In this work, our objective is to propose a strategy for the optimization of the SiC/Si structure as a subsequent substrate to grow high quality GaN layers. Several routes are investigated

within the framework of a theoretical approach which we have recently developed and which has proved itself to be very useful in many aspects of the physics of heteroepitaxy. This approach is based upon the elasticity theory of strained interfaces which are thus analyzed in terms of their elastic and structural properties. It can predict the formation of stable phases induced by epitaxial strains as well as their composition and also can allow the evaluation of buffer layers for optimized heteroepitaxial growth needs. By constraining a material to grow on a substrate structure, effective stress, which acts as a phase-stabilizing factor, is induced in the hetero-system. However, we indeed know from X-ray and electron microscopy studies that the morphology of multiphase crystals can not be understood only on the basis of classic thermodynamics of phase transformations which involve bulk chemical free energy and interface energy terms. The effect of strain elastic energy due to host materials lattice mismatch is relevant too. One of the methods we consider relies on the effect of the incorporation of group IV atoms into the 3C-SiC/Si structure. This incorporation aims at elaborating an alloy-like buffer layer which has the property of improving the matching of SiC and Si host material lattices. The parameters involved in the theory are the elastic constant c_{ij} , the lattice constant a and the density ρ associated with each host material. The importance of these parameters in investigating the physics of epitaxially strained interfaces is recognized from Hooke's law which states that the resulting strain is directly proportional to the stress magnitude, i.e. to the magnitude of the force acting on a unit area in the solid. This provides a strain-dynamics relationship implying buffer layer composition-dependent parameters. Thus by optimizing this composition, we can provide a theoretical basis for further growth investigations on the GaN/SiC/Si system based on the buffer layer technique.

In-situ etching of SiC wafers in a CVD system using oxygen as the source

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Quality of a SiC epitaxial layer depends to a great extent on the quality of substrate surface. Hydrogen etching at the growth temperature is the conventional method used for removing scratches on the commercially available substrates. However, Si droplets usually form on the surface. Formation of droplets can be inhibited by adding a small amount of C₃H₈ in the H₂ flow. However, addition of C₃H₈ reduces the etching rate considerably. HCl gas phase etching is another method used to pre-etch SiC prior to epitaxial growth, but it is preferable to avoid the use of HCl in a CVD system. We have investigated a new method to etch SiC by adding a small amount of oxygen in the hydrogen flow to overcome the above problems. Etching experiments under various temperatures and oxygen flow rates are performed. The etched surfaces are examined by optical microscope, AFM and XPS.

Etching was performed in a horizontal water-cooled cold-wall CVD reactor. High purity oxygen diluted in Argon was used as the source, in addition to hydrogen as the bulk of carrier flow. The substrates used were (0001) Si-face, 3.5°-off 6H-SiC from Cree Research, Inc. Etching was carried out for 30 minutes at 100torr and at a temperature in the range from 1500 to 1600°C with different flow rates of oxygen.

First, etch rate was measured at different temperatures and oxygen flow rates. The result shows that at a certain temperature, etch rate first increases rapidly (linear region) and then saturates with the increase of oxygen flow. When observed under the optical microscope, samples etched using a low oxygen flow (linear region) show a smooth and featureless surface, and samples etched under the saturation region show very poor morphology. The oxygen flow and the etch rate required for getting the rough surface increases with the etching temperature. Etch rate as high as 8μm/hr was obtained.

High-resolution XPS spectra from Si2p for etched samples were obtained. They can be fitted with four Gaussian peaks which are assigned to Si (99.2eV), SiC (100.4eV), SiO_x (x<2) (101.7), and SiO₂ (103eV). The fraction of each compound was calculated by determining the ratio of peak area. The result shows that SiO₂ on the surface increases while Si decreases with the increase of oxygen level in the system during etching. We believe that the saturation of etching rate and the rough surface obtained at higher oxygen concentration are the direct result of the formation of SiO₂ on the surface.

AFM on sample etched with pure hydrogen shows lots of sub-micron size white dots probably caused by Si droplets. They can be removed by dipping the sample into hot HF/HNO₃ solution for a few minutes. No white-dots can be seen on all H₂/O₂ etched samples. AFM also reveals the appearance of micro step bunching. The width and height of step increase with the increase of oxygen used during the etching. Excellent surface was obtained when epitaxial growth was carried out on this oxygen-etched surface.

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In-situ etching of SiC wafers in a CVD system using oxygen as the source
(continued)

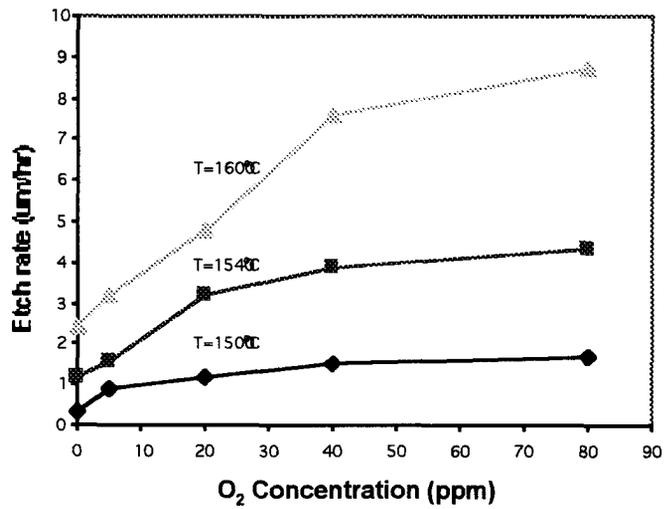


Fig. 1. Dependence of etch rate on O₂ concentration at different temperatures

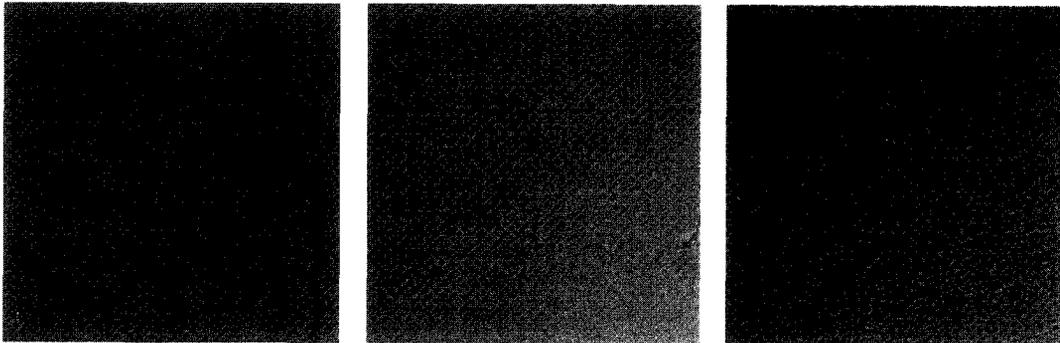


Fig. 2. Optical micrographs of SiC samples etched at 1540°C with 20ppm, 40ppm, and 80ppm of O₂, respectively

Improvement of the SiCOI structures elaborated by heteroepitaxy of 3C-SiC on SOI

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Silicon on Insulator (SOI) is a promising candidate to replace bulk Si for the hetero-epitaxial growth of 3C-SiC/Si. Large strain reduction in the 3C-SiC layer and improvement in the electrical insulation are expected [1]. However, large cavities in the buried oxide (BOX) have been observed after SiC deposition, resulting in the deterioration of the electrical properties. Increasing the deposition temperature or decreasing the silicon overlayer (SOL) thickness increased the size and density of the cavities [2, 3]. The origin of this phenomenon is not yet established, even if some initial defects in the SOI or thermal instability of the oxide were proposed.

In this work, we demonstrate improvement of the available SICOI (SiC On Insulator) structures by using new generations of UNIBOND substrates from SOITEC. Experiments have been carried out in a conventional vertical cold wall AP-CVD reactor with SiH₄ and C₃H₈ as reactants and H₂ as vector gas. Standard growth conditions were used: carbonisation at 1150°C with subsequent epitaxial growth at 1350°C. Three types of <100>-UNIBOND substrates with different SOL/BOX thickness were used : A) 205/200 nm; B) 75/50 nm; C) 85/18 nm.

After growing 3 μm thick SiC layers, all samples showed good surface morphology and crystalline quality very similar to that of comparative layers grown on bare Si substrates. No buckling of the layers was observed even for the thinnest SOI structure (sample C). From infrared reflectivity spectra and TEM observations, no deviation could be found for the SOL and BOX thickness as compared with the nominal UNIBOND values (table 1). No large cavity could be detected by optical microscopy, even at the highest magnification used (x1000). Only small cavities, with diameter ranging from 100 to 250 nm, could be found from TEM observations (figure 1). Estimated surface proportion of these holes at the SiC/SOI interface was only 0.03%, which is by far the lowest value ever reported. Balling up of the silicon around the cavities was also observed, suggesting bridges between the SiC layer and the substrate.

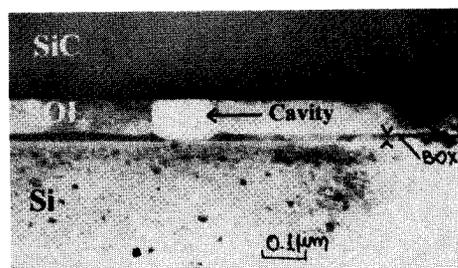


Figure 1 : TEM cross section of sample C

Table 1 : Physical parameters of the SiCOI structures

	Nominal SOI parameters	TEM data	IR data	IR Interface roughness (nm)	Cavity mean size (nm)	Density of cavities (cm ⁻²)	Dislocation density in the SiC layer (cm ⁻²)
Sample A 3C-SiC (μm) SOL/BOX (nm) SOL/BOX ratio	3.0 205/200 1.02	2.80 208/198 1.05	2.67 185/176 1.05	70	250	10 ⁶	5.10 ⁹
Sample B 3C-SiC (μm) SOL/BOX (nm) SOL/BOX ratio	3.0 75/50 1.5	2.95 68/48 1.41	2.675 67.8/47.9 1.41	57	100	2.10 ⁵	6.10 ⁹
Sample C 3C-SiC (μm) SOL/BOX (nm) SOL/BOX ratio	3.0 85/18 4.72	3.24 78/16 4.87	2.690 60.0/17.1 3.5	≈ 0	250	6.10 ⁵	10 ⁹

The cavity density calculated from the TEM observations (about 10⁵ cm⁻²) is several orders of magnitude higher than the defect density in the SOI before heteroepitaxy. So, these holes cannot be related to the defect density of the SOI samples. The mechanism of formation of the cavities should be related to the high temperatures involved in the growth. The cooling stage may also be critical as the 3 μm thick SiC change the rigidity of the structure above the BOX so that the thermal mismatch changes. As SiO₂ is quite mobile at the deposition temperature, any strain imposed to the whole SOI structure can affect preferentially the BOX. One can also think to the following reaction occurring at the Si/SiO₂ interfaces : SiO_{2(s)} + Si_(s) = 2 SiO_(g). This reaction releases gas which can explain the ball like shape of the cavities. However, figure 1 shows that the quantity of oxide consumed to form a cavity is lower than the quantity of consumed Si. We believe that silicon out-diffusion at the SiC/Si interface is also probably occurring as this phenomenon is very difficult to avoid completely at the early stage of growth.

From table 1, one can see that the thinning of the SOL and/or BOX does not affect strongly the structural properties of the SiCOI structure. However, the interface roughness, as calculated from IR spectra fitting, seems to decrease when the BOX gets thinner and/or when the SOL/BOX ratio increases. This roughness is not due to any inhomogeneity of the starting material as confirmed by TEM observations over several millimeters.

AFM, photoluminescence and electrical characterizations are under progress in order to have a deeper evaluation of the benefit given by the use of this new generation of UNIBOND samples.

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Formation mechanism of interfacial voids in the growth of SiC films on Si substrates

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SiC/Si structures have been successfully used to fabricate microelectromechanical system (MEMS) such as microsensors and microactuators working at the temperatures above 200 °C and potentials above several tens of voltages [1,2]. However, crystal defects formed at the interface of the 3C-SiC/Si structures significantly influenced the crystal quality of the over-grown 3C-SiC films. Several research groups have discussed the way to improve the SiC/Si interface and the mechanism of void formation in the growth of SiC films on Si up to recently. However, most of the mechanisms have not clearly explained how the void formation initiates in the SiC growth. Therefore, the mechanism of void formation is still open to debate.

In this work, we measured the shape of voids formed during the growth of SiC film on different orientations of Si substrates and studied the origin of the voids. SiC films were grown on both p-Si(100) and (111) wafers using a single source tetramethylsilane ($\text{Si}(\text{CH}_3)_4$, TMS) in a homemade RF-inductive chemical vapor deposition (CVD) system [3]. XRD measurements showed that the orientation of the grown SiC films followed that of the employed Si substrate. The cross-sectional SEM images (Fig. 1) shows that, in the silicon side of SiC/Si interface, reverse-triangle shaped voids were observed for the growth of SiC(100) on Si(100), whereas trapezoid shaped voids for the growth of SiC(111) on Si(111). Figure 2 shows SEM images for the initially etched Si(100) and Si(111) surfaces. The etched Si(100) uniformly produces rectangular shaped etch pits cross the wafer surface, whereas triangle shaped etch pits evenly appear from the etched Si(111) surface. This indicates that the shape of voids is mostly determined at the initial stage of the growth of SiC depending on the surface orientation of the Si substrate.

In conclusion, the mechanistic study revealed that the voids seems to be the oxygen-related defects inherently existing in bulk Si wafers. The shape of the voids was determined by that of etch pit initially formed during the hydrogen etching process, which depends on the orientation of the silicon substrate. The mechanism of the void formation in the growth of SiC orientation of the silicon substrate.

Acknowledgements

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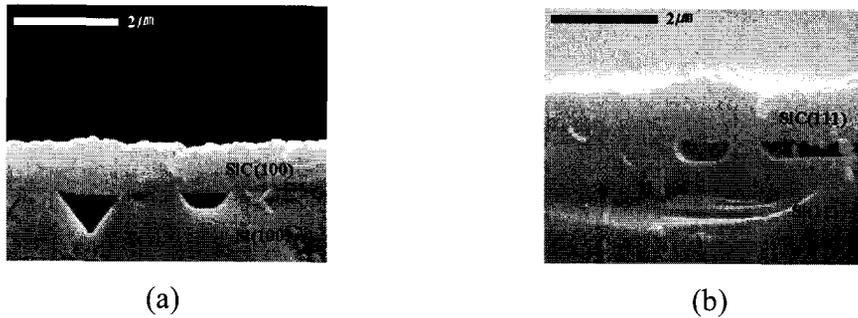


Figure 1. Cross-sectional SEM photographs for (a) SiC(100)/Si(100) and (b) SiC(111)/Si(111) structures. The growth was carried out for 60 min at 1250 °C and 50 torr with TMS/H₂ = 1.0/1000 sccm.

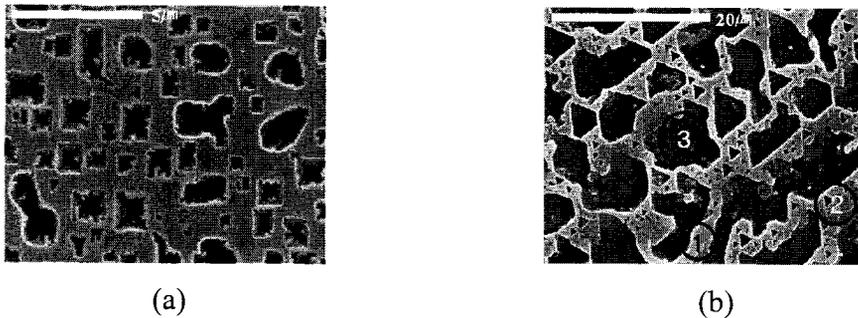


Figure 2. SEM plane views for Si surfaces after removing SiC films from SiC/Si structure. (a) Si(100) and (b) Si(111).

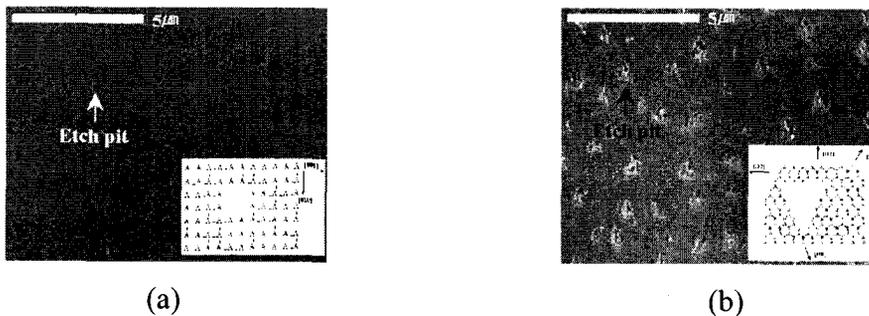


Figure 3. SEM plane views for the surfaces of (a) Si(100) and (b) Si(111) etched with 1000 sccm H₂ for 5 min at 1100 °C.

Evaluation of Carbonized Layers for 3C-SiC/Si Epitaxial Growth by Ellipsometry

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Heteroepitaxial growth of 3C-SiC on Si substrate has been a promising method for obtaining large area 3C-SiC. Success in carbonization process has been important for continuous growing process. The reproducible carbonized layers were obtain, by holding the temperature of the Si substrate at the range of hydrogen desorption temperature, prior to carbonization [1]. In this work, to reproducibly obtain the single-crystalline 3C-SiC on (100)Si, carbonization process has been paid careful attention and carbonized layers were investigated by Ellipsometry. The heating-up of the Si substrate was examined in three different ways as shown in Fig. 1 and experimental procedures were showed in detail in previous work [1]. The substrate temperature at 600 °C in Type II and Type III were held for 5 min and 15 min respectively. The reproducible carbonized layers were obtained by using Type II and Type III, while were not obtain by using Type I as showed in previous work [1]. Fig. 2 shows changes in measured Δ and Ψ values by the ellipsometer and results of RED patterns of carbonized layers by using Type II and Type III. Prior to carbonization, Si surfaces are covered with amorphous carbon films at 600 °C and the carbonized layers are crystallized by out-diffusion of Si atoms at the carbonization temperature of 1000 °C and Si surfaces are covered by single-crystalline 3C-SiC carbonized layers. When Si surfaces are covered by single-crystalline 3C-SiC carbonized layer, Graphite layers are formed on 3C-SiC carbonized layer because of sealed up out-diffusion of Si atoms. In comparison between Type II and Type III, Si surfaces are completely sealed up out-diffusion of Si with single-crystalline 3C-SiC carbonized layer by using Type III. It is impossible to evaluate the carbonized layers by simple one-layer model of Ellipsometry, so multi-layers model of Ellipsometry was adopted to the carbonized layers by using Type II and Type III. Simulation of the carbonization layers by using interface layer between each layers agreed with changes of experimental data as a function of carbonization time as shown in Fig. 3. From these results, It is possible to suggest the model of the carbonization by using Type II and Type III as shown in Fig. 4.

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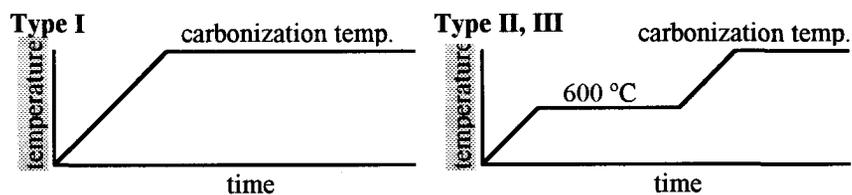


Fig. 1 Temperature program for carbonization process. Substrate temperature of Type II and Type III is held at 600°C for 5 min and 15 min respectively prior to heating up to carbonization temperature.

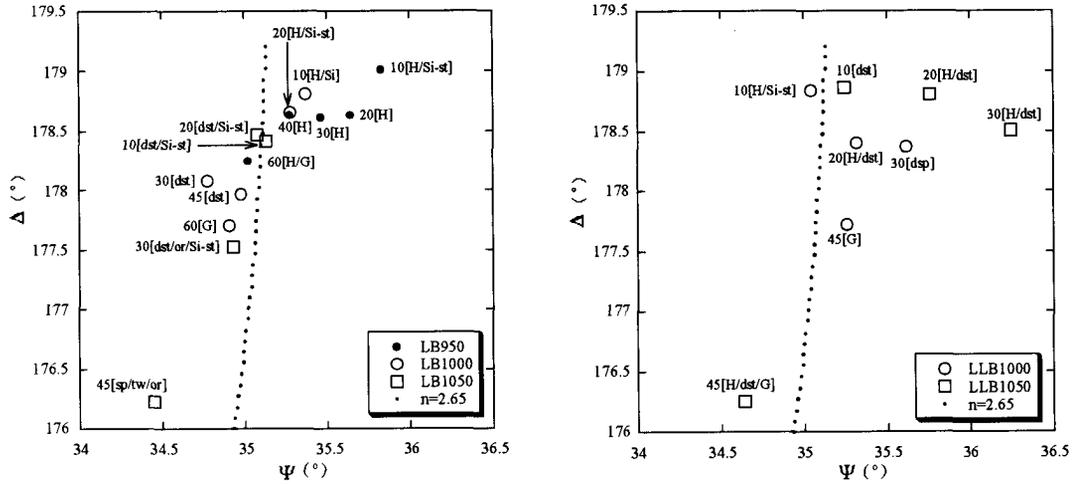


Fig. 2 Changes in measured Δ and Ψ values and results of RED patterns of the films deposited by Type II (LB) and Type III (LLB). Theoretical line (one layer model) indicates $n=2.65$, $k=0$ for 3C-SiC. One dot indicates 2 Å. Number, H, Si-st, dst, sp, or, tw and G by plots indicate carbonization time, halo, Si-streak, 3C-SiC diffused streak, 3C-SiC spot, oriented, twin and graphite ring of RED patterns.

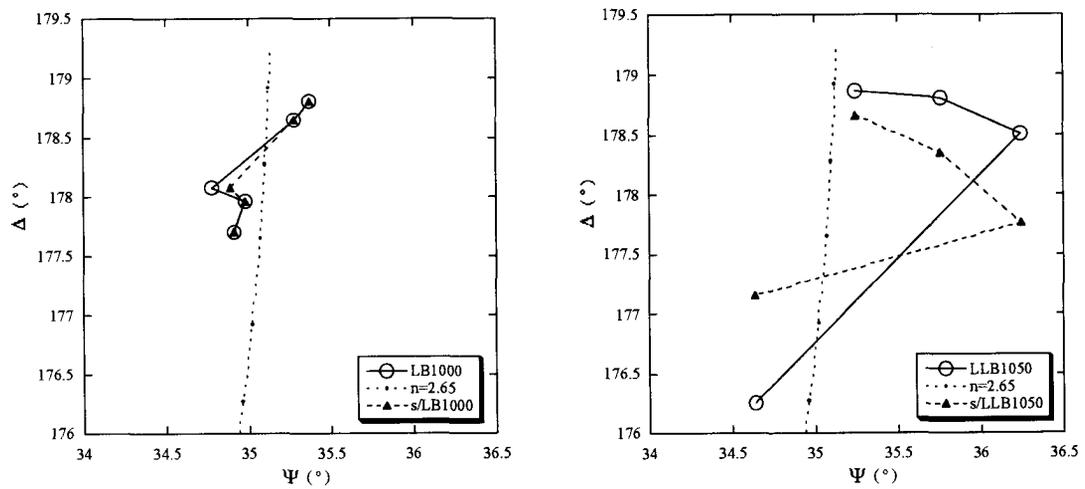


Fig. 3 Simulation of carbonized layers for Type II and Type III by multi-layers model of ellipsometry. A solid and a broken line show experimental and simulation data respectively.

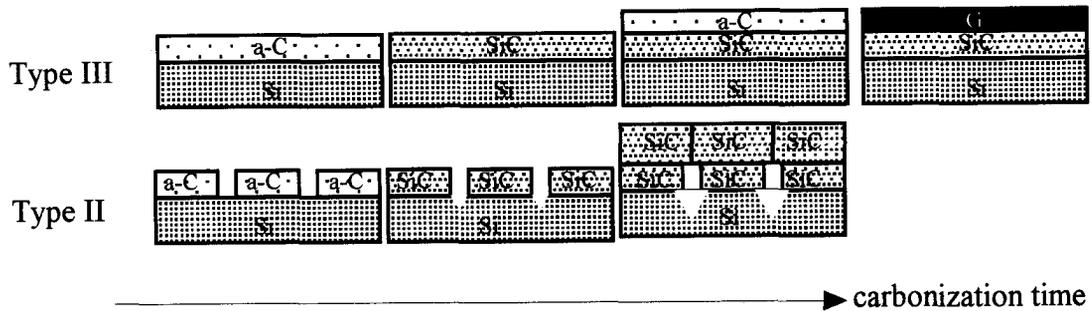


Fig. 4 Carbonization model for Type II and Type III

Carbonization process of a Si surface by subplantation of low-energy ions

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A novel carbonization process for 3C-SiC heteroepitaxial growth on Si (100) using subplantation of low-energy mass-separated carbon ion beams is proposed. SiC is an important candidate of the semiconductor materials for achieving the production of high temperature electronics, power devices, etc. In particular, the heteroepitaxial growth of 3C-SiC on Si substrates is a key technology for those electronic devices. It has been reported that a so-called carbonization process forms a SiC buffer layer which is required for the successful heteroepitaxial growth of 3C-SiC on Si. However, conventional methods such as MBE, CVD, etc. have required high temperatures ranging 700–1000 °C for achieving carbonization reaction. Those high temperatures cause serious problems of defects such as dislocations and stacking faults at the heterointerface. In this study, a carbonization process at lower temperatures has been tried using low-energy carbon ion beams for solving these problems.

Si (100) surfaces were directly irradiated by mass-separated low-energy (20–700 eV) carbon ion beams (e.g., C⁻, C₂⁻, C⁺, CH₃⁺ ions). Such energetic ion beams are implanted into a subsurface (subplanted) of the Si substrate, unlike thermal species used for MBE and CVD methods. The substrate temperatures were varied in the range 440–700 °C. RHEED measurements were performed during ion irradiation for in-situ characterization of the carbonization process. The base pressure of the deposition chamber was $\sim 10^{-8}$ Pa and the beam-on-target pressure was $1-4 \times 10^{-6}$ Pa.

Carbonization reaction was achieved at substrate temperatures of 500-700 °C with all kinds of carbon ions e.g.; C⁻, C₂⁻, C⁺, CH₃⁺ ions. There was almost no significant difference in the diffraction patterns between C⁻, C₂⁻ and C⁺ ion-beam carbonization. All the RHEED images after irradiation of these carbon ions consisted of spotty patterns indicating 3D-island growth of a 3C-SiC. On the other hand, the diffraction image after CH₃⁺ irradiation exhibited streak patterns, suggesting a smooth surface and better crystallinity relative to

irradiation by other species.

The carbonization temperatures of 500-700 °C using ion-beams are relatively low compared to conventional methods. While the process with thermal gas species with less than 1 eV is basically thermal equilibrium or nearly-equilibrium reaction, carbon ion beams as energetic species with several to hundreds of electron volts employed in this study allow non-equilibrium reactions. The difference of reaction mechanisms between these has probably affected the carbonization temperature.

GROWTH AND CHARACTERIZATION OF SiC NANOROD STRUCTURES CONTAINING Si NANOCRYSTALS

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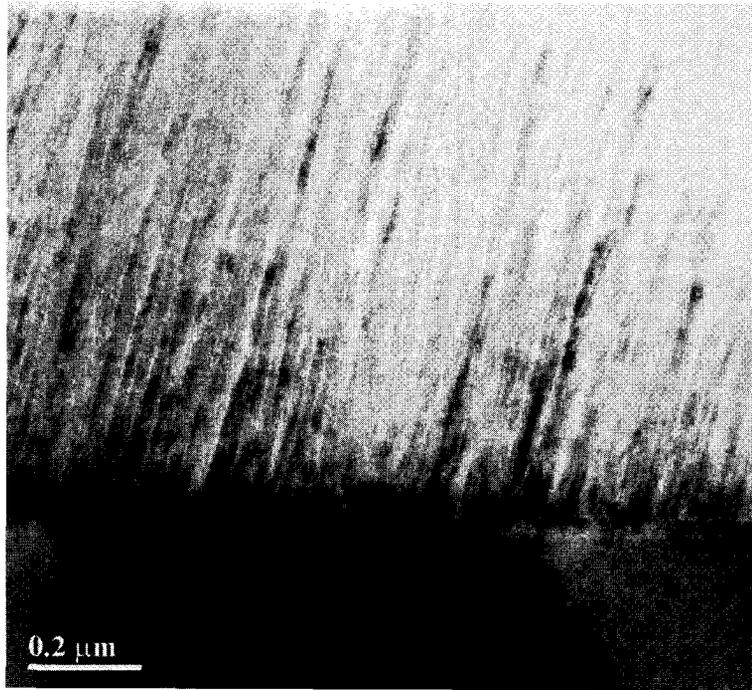
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The rapid developments taking place in the preparation and application of nanostructures is one of the most exciting areas of material science and technology. Since the discovery of carbon nanotubes, nanoscale materials have received widespread interest and nanorods of various materials have been synthesized so far. Nanorod structures, for example, have become an important material because of its excellent mechanical properties. Furthermore, devices made using nanorods can be critical for nanoelectronics. Moreover, the electron field emission properties of carbon nanotubes are of special interest for their potential application in flat panel displays. SiC nanorods were found also to be a promising material for applications in field emission technology. The electron field emission characteristics are similar to that one of carbon nanotubes. However, it is still difficult to control the rod size and orientation.

In this work we present results of the growth and the characterization of SiC nanorod structures. The nanorods were prepared on a SiC/Si(111) heterostructure under ultra high vacuum conditions at low temperatures of 1000 K using elemental silicon and carbon. Si and C were evaporated by means of electron-beam guns. The single-crystalline SiC of some nanometers thickness was grown before on Si(111) by molecular beam epitaxy.

The obtained SiC nanorod structures are homogeneous in the diameter and the length of the rods across the thickness of the structure (Figure). The diameter of the nanorods is in the range of 5-10 nm, the smallest values known so far. The rods consist of a high-density of stacking faults like a “one-dimensionally disordered” SiC polytype. This is supported by Raman scattering experiments, where the intensities of the SiC related phonon lines were very low and at different positions, depending on the structure. Furthermore, there is a strong alignment of the rods. However, the rods are tilted with respect to the [111] surface normal of the SiC layer by about 15°, which is about the [311] direction.

Between the rods, the material is amorphous and contains a high amount of Si nanocrystals, which is depending on the excess of Si in the Si/C ratio. The size of the Si nanocrystals was in the range of 1 nm. In Raman scattering experiments, the Si line was found to be broad and shifted to smaller wave numbers with respect to the Si bulk line. Moreover, a strong optical absorption in the nanorod structure occurred in dependence on the structure. Si nanocrystals with sizes smaller than 1.5 nm should demonstrate quantum confinement effects, what increases the oscillator strength significantly. The obtained structures, therefore, also allow the investigation of the optical properties of Si nanocrystals embedded in an oxygen-free, high dielectric matrix.



High-resolution TEM image of a SiC nanorod structure grown on SiC/Si(111)

RHEED: A tool for structural investigations of thin polytypic SiC layersF. Scharmann, J. Pezoldt

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One of the exceptional challenges of SiC is the possibility of the formation of heteropolytypic structures for heterojunction based advanced semiconductor devices. For the experimental realization of such devices, the development of methods for the controlled formation of different polytypes, polytypic multilayers and their interfaces is necessary. In the last decade substantial progress was achieved in this field [1,2]. The most promising technique is molecular beam epitaxy (MBE) offering exceptional possibilities for controlling and adjusting growth conditions [2], but extended post-growth characterization is necessary in order to identify the appropriate growth conditions, leading to desired surface morphology and polytype structures [3]. Nevertheless the MBE technique offers the possibility to study the structure of the growing polytype layer in situ in real time by applying reflection high energy electron diffraction (RHEED). Up to know only, relatively few papers have dealt with such investigations. Most of them utilized the analysis of the three dimensional electron diffraction pattern for polytype analysis. In the case of two dimensional diffraction, because of the difficulty in the exact determination of the streak modulations and in the interpretation of them, no data is available. In this work it will be shown that even in the case of two dimensional diffraction it is possible to distinguish between different polytypes and surface polarities.

For this reason we determined the inner potential of the silicon carbide by analysing the geometry of the horizontal Kikuchi lines for our diffraction condition. A value of 15.4 V was obtained. The value RHEED pattern simulation was performed by using the semi-kinematical approximation described in [4]. The simulation was carried out for the 3C, 4H and 6H polytypes and silicon and carbon faces and angles of incidence between 0.5 and 4°. The results obtained allows the conclusion that the polytypes can be distinguished in the case of two dimensional diffraction if the penetration depth of the electron beam is not smaller than the characteristic period of the polytype, i.e. if the specific features of the polytypes can be detected by the electron beam. To distinguish different polarities of the growing surface the penetration depth has to be smaller than seven layers. The best sensitivity to the different polarities can be obtained if the penetration depth does not exceed three double layers. From the carried out simulations of the two dimensional diffraction features it follows that the optimal angel of incidence for RHEED diffraction analysis of different polytypes and polarities is in the range of 1 to 2.5°.

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MOLECULAR ADSORPTION OF OXYGEN ON SiC SURFACES

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The initial steps of the oxidation of Si surfaces have been extensively studied and most of the oxygen molecules adsorb dissociatively on Si. However, at small oxygen exposures and low substrate temperatures a metastable molecular O₂ species has been observed [1,2,3]. Since the initial steps of oxidation of SiC are also of great interest and importance we have studied if a similar metastable molecular precursor for the dissociative adsorption of oxygen do form on SiC surfaces.

The O 1s photoemission spectrum recorded from a $\sqrt{3}\times\sqrt{3}$ R30° reconstructed 4H-SiC(0001) surface after an oxygen exposure of 0.3 L (1 Langmuir = 10⁻⁶ torr sec.) is shown in Fig. 1. The substrate was cooled to liquid nitrogen temperature during both exposure and measurements and the spectrum was collected using a photon energy of 600 eV. The spectrum is seen to contain several components and included in the figure is a peak decomposition. Four components, labeled 1 to 4, are clearly distinguished similarly as on the Si(111) surface [3]. Components 3 and 4 are interpreted to originate from molecular O₂ and components 1 and 2 from atomic oxygen. The relative intensities of these components did vary with the amount of oxygen adsorbed on the surface.

Also with the substrate at room temperature some molecular O₂ was found to adsorb while no trace of molecular O₂ was discernable after adsorption with the substrate at an elevated temperature of 800° C. This is illustrated in Fig. 2 where the O 1s spectrum recorded after 1 L exposure is shown for the three different cases, LN, RT and 800° C.

Studies were carried out on both Si- and C-terminated 4H-SiC (0001) crystals and differences between the two surfaces were observed. The time evolution of the O 1s spectrum was monitored since the state was assumed to be metastable. Our findings, showing that a molecular state precedes the dissociated (atomic) stable adsorption states on SiC surfaces, will be presented and discussed.

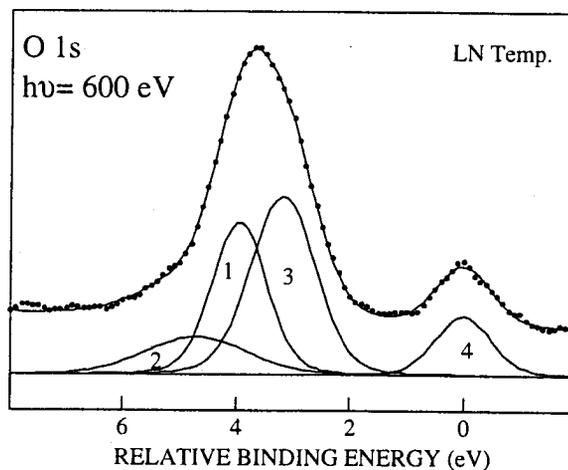


Fig.1. O 1s spectrum (dots) recorded using a photon energy of 600 eV after 0.3 L of oxygen exposure. The solid curve through the data points show the result of the curve fit and the curves underneath show the components used. See text for details.

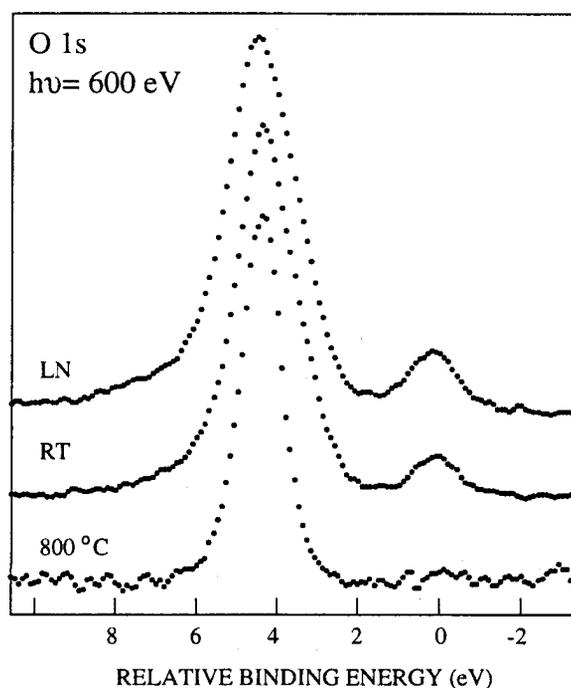


Fig.2. O 1s spectra recorded after 1 L of oxygen exposure at different substrate temperatures, LN, RT, and 800°C.

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3C-SiC pn -STRUCTURES GROWN BY SUBLIMATION EPITAXY ON 6H-SiC SUBSTRATES

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Cubic silicon carbide is of considerable interest for semiconductor electronics having, in particular, the highest charge carrier mobility of all SiC polytypes; besides, it is also known that β -SiC is sometimes found in the form of inclusions in epitaxial films of wider bandgap polytypes of α -SiC. Therefore, studies of β -SiC and identification of the effects caused by the presence of β -SiC in α -SiC are of unquestionable interest. Progress in the sublimation epitaxy in vacuum (SEV) technology enabled fabrication of n-3C-SiC/n-6H-SiC epitaxial heterostructures with good quality of the 3C-SiC epilayer [1].

The aim of the present study was to obtain 3C-SiC pn structures by SEV and study their properties. The investigated pn structures were grown by SEV on 6H-SiC (0001) Lely substrates. X-ray topography showed that the preliminarily grown n-type epilayer contains a large region of 3C-SiC, which is double-position (DP) twin. The area of the n-3C-SiC layer was about 25 mm². The pn junction was formed by SEV growth of a p⁺ (Al)-layer. X-ray topographs confirmed that a p⁺-3C region with DP twins of different sizes is formed on the n-type epilayer. An ohmic contact to the p-type region was formed by deposition of Al and Ti and annealing at 1100°C. Mesa structures of area 3x10⁻³ cm², 10⁻⁴ cm², and 8x10⁻⁵ cm² were fabricated by reactive ion-plasma etching (to a depth of about 3 μm) with an Al mask.

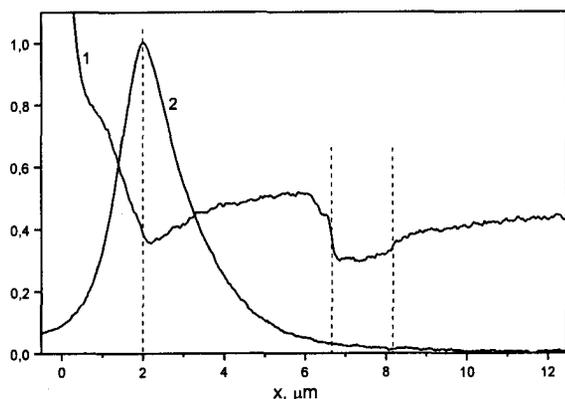


Fig.1. Secondary electrons (curve 1) and electron beam induced current (curve 2) signals for diode.

The diode cross sections were studied by the methods of electron beam induced current (EBIC) and secondary electrons (SE) in a JSM-50A scanning electron microscope. Figure 1 shows the coordinate dependencies of SE and EBIC signals obtained in scanning of the cross-sectional surface of diodes. The SE curve shows three jumps of the SE signal. The portion with the largest jump corresponds to the pn junction in 3C-SiC, which is also well manifested in the EBIC mode. The other two portions correspond to isotype n-3C SiC/n-6H SiC junctions and the n-6H SiC/substrate. Thus, in the initial stages of epitaxial growth on the 6H SiC substrate, a buffer n-6H SiC layer of thickness ~1.5 μm was formed. Then, there occurred polytype transformation and growth of an n-3C-SiC epilayer (4.5 μm thick). The pronounced jump of the secondary electron signal at the interface of the 3C-6H SiC isotype heterojunctions indicates a substantial potential jump at the interface between two semiconductors. An estimate of the hole diffusion length in the n-3C SiC layer, made on the basis of EBIC data, gave a value of ~1.5 μm. So a noticeable fraction of holes injected from

p-3C SiC can diffuse through the n-3C SiC layer to reach the interface with the buffer 6H-SiC layer.

The capacitance-voltage (C-V) characteristics of the diode were linear in the $C^{-2} - V$ coordinates, which means that the obtained pn junction was abrupt. The capacitance cutoff voltage (U_c) was 2.05 ± 0.05 V for diodes, i.e. close to E_g for 3C-SiC (2.39 eV). It was shown, that at low current densities the dependence of the current on voltage is exponential: $J = J_0 \exp(qV/nkT)$ with the ideality factor $n=2.5-2.6$ (Fig.2.a). The J-V characteristics of the diodes were fairly close to those of anisotype homojunctions based on bulk 3C-SiC [2].

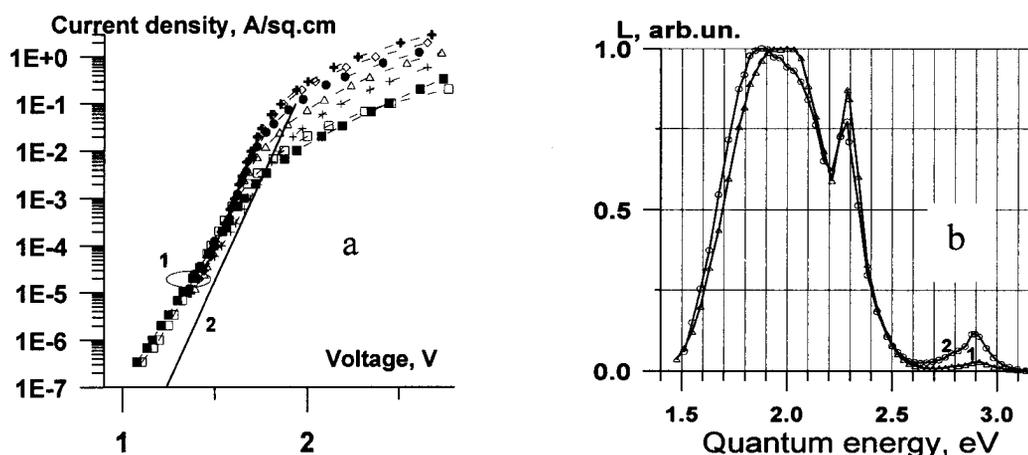


Fig.2. Experimental (curves 1; different symbols refer to different diodes) and calculated (curve 2; for 3C-SiC pn homojunction [2]) current-voltage characteristics at forward bias and room temperature (a); injection electroluminescence spectra for two diodes: of area $3 \times 10^{-3} \text{ cm}^2$ (curve 1; current 150mA) and $8 \times 10^{-5} \text{ cm}^2$ (curve 2; current 100mA) (b).

Injection electroluminescence spectra (IEL) for diodes are presented in Fig.2.b. The emission bands $h\nu_{\text{max}} \approx 1.8-2.0$ eV (red), $h\nu_{\text{max}} \approx 2.3$ eV (green) and $h\nu_{\text{max}} \approx 2.9$ eV (violet) are dominant; both the absolute and relative intensities of the emission bands at $h\nu_{\text{max}} \approx 2.9$ eV and $h\nu_{\text{max}} \approx 2.3$ eV grow with increasing current and the diode temperature. The spectral position of the EL bands at $h\nu_{\text{max}} \approx 2.9$ eV and $h\nu_{\text{max}} \approx 2.3$ eV, closeness of energies to the band gaps of 6H- and 3C-SiC, their narrow half-widths (compared, in particular, with the half-width of the so-called "defect" line (green in 6H SiC), and the characteristic change in their intensity with increasing current and stronger heating make it possible to relate these two EL bands to free exciton annihilation in 6H- and 3C-SiC. The red emission band appears to come from 3C-SiC and is believed to be due to transitions involving Al.

The characteristics of the structures under study correspond to those of homojunctions based on 3C-SiC. The emission band in the IEL spectrum of this kind of diodes, arising from recombination of free exciton in 6H SiC, is probably related to hole diffusion from p^+ 3C through the 3C SiC layer to the interface with the buffer 6H layer. The fact that this emission comes from within the base region, and not from the metallurgical boundary of the pn junction, is clearly seen on an edge cross-section of the sample under an optical microscope.

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Sensitive Detection of Defects in α and β SiC by Raman Scattering

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Raman spectra provide information on the structure of crystals. One can analyze defects from the difference of the Raman spectra for perfect and imperfect crystals. So far, we have developed a technique for sensitive detection of defects in 6H,4H [1] and 3C SiC. This technique is based on the measurement at Raman forbidden geometry and has been applied to the characterization of defects in bulk crystals and epitaxial layers of SiC. Electrical properties such as carrier concentration and mobility can also be analyzed by Raman spectroscopy [2]

In this work we have developed a method to detect low density of defects and analyze the local structure of the defects from band shape of the TO phonon bands. We also examined affect of defects on the distribution of the carrier concentration from Raman image measurements of the LO phonon plasmon coupled mode in doped SiC wafers.

In perfect crystals the wave vector selection rule and polarization selection rule hold strictly during the Raman scattering process. These selection rules break down partially when there are defects, because the periodicity and symmetry of the crystals are destroyed. The defect-induced Raman scattering signals are usually weak and buried in a strong background, which can be avoided by choosing a suitable scattering geometry. We found that the observation at the Raman forbidden scattering geometry is efficient for detecting the defect induced-Raman bands. For SiC the TO and folded TO modes are sensitive to the defects as compared with LO phonon modes. We used unfolded TO mode designated as FTO(0) at 796 cm^{-1} as a monitor band for the defects in 6H- and 4H-SiC, which is Raman forbidden at the back scattering geometry using the (0001) face [1]. The TO band in 3C-SiC is forbidden at the back scattering geometry using the (001) face.

We have measured Raman images of the (100) cross section of homoepitaxial SiC films. An epitaxial film (100 μm) was made on a heteroepitaxially grown SiC of 100 μm thick, for which the growth surface was originally the interface of the SiC and Si. Therefore, it is

anticipated that defects are concentrated in the central region of the film. In Fig.1, the intensity and half width of the forbidden TO band are plotted as a function of the distance. The intensity and the width of the TO band are large at around the central region. The TO band is broad compared with that observed using the (110) face, and is asymmetric. It has a tail on the low frequency side at the central region as shown in this figure. These results show that the defect density is high at the central region which was originally the SiC-Si interface. The asymmetry and broadening of the TO band is indicative of the presence of the stacking faults [3,4] and other defects such as antiphase boundaries and dislocations.

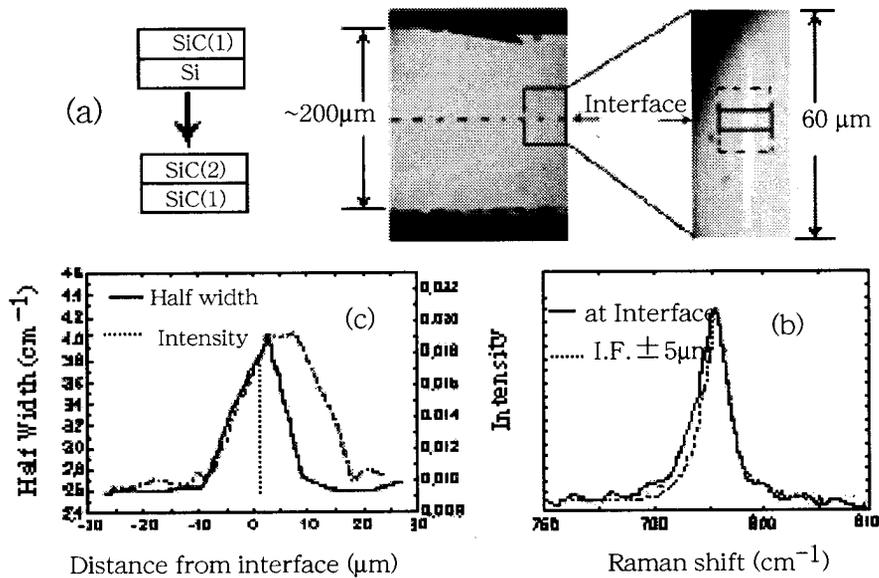


Figure 1 (a) optical microscope image of the (100) cross section of the homoepitaxial film , (b) Raman spectra of the TO band, and (c) the intensity and half width of the forbidden TO band vs distance.

The Raman images of the LO phonon plasmon coupled mode are also measured in doped 4H- and 6H-SiC wafers. The reduction of the free carrier concentration is found around some micropipes as reported before[5]. Change in the carrier concentration is also observed at defective portions which might be associated with threading dislocations , and for planar defects.

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LUMINESCENT PROPERTIES OF EPITAXIAL LAYERS OF SOLID SOLUTIONS BASED ON SiC.

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Solid solutions based on SiC make it possible to enlarge the range of application of optoelectronics devices. Specifically, LED's and injection lasers are very promising, since they can inherit, on the one hand, the unique properties of silicon carbide and, on the other, they can acquire properties which are characteristic of the second component of the solid solution.

$(\text{SiC})_{1-x}(\text{AlN})_x$ and $\text{Si}_{1-x}\text{Nb}_x\text{C}$ solid solutions have been received by sublimation in Ar + N_2 atmosphere on n-type 6H-SiC substrates. The composition of epitaxial layer (EL) has been set with source of vapor, and the type of electrical conductance – with regulation of Ar and N_2 partial pressure in the growth zone.

The spectra photo- (PL) and cathodoluminescence (CL) $(\text{SiC})_{1-x}(\text{AlN})_x$ and $\text{Si}_{1-x}\text{Nb}_x\text{C}$ solid solutions was investigated. The samples with such composition layers $(\text{SiC})_{1-x}(\text{AlN})_x$ ($x > 0,55$) are used for which the light of N_2 - laser ($h\nu = 3,68$ eV) lies in the transparency area ($E_g > 4,8$ eV) and that is why so cannot effectively excite their emission. The CL spectra were measured at liquid – nitrogen temperatures and excitation energy of 15 kV.

It is observed that at liquid – nitrogen temperature two bands with $\lambda = 520$ nm ($h\nu_{\text{max}} \sim 2,4$ eV) and $\lambda = 480$ nm ($h\nu_{\text{max}} \sim 2,6$ eV), which due to recombination on defects and donors – acceptor pairs are observed in $(\text{SiC})_{1-x}(\text{AlN})_x$ solid solutions spectra. As the AlN concentration in $(\text{SiC})_{1-x}(\text{AlN})_x$ solid solutions increases the bands shift continuously into the short – wavelength region and an ultraviolet “tail” with $\lambda = 390$ nm ($h\nu_{\text{max}} \sim 3,2$ eV) appears. The last peak indicates the solid solution formation in system SiC-AlN and a change in the structure of the band gap. The color of the emission changes from yellowish – green to pale blue.

PL intensity decreases with the x growth in $(\text{SiC})_{1-x}(\text{AlN})_x$ solid solutions, though the main bands and distances between them are practically preserved. On one hand, it is connected with increase of share of centers of nonradiative recombination, as far as at $x > 0,40$ decreases the structural perfection of $(\text{SiC})_{1-x}(\text{AlN})_x$ solid solutions and presence of defects of layers grow. On the other hand, presence Al and N_2 reduces the efficiency of DL. And, at last, the change of intensity, perhaps, is stipulated by increase of probability of interbanded transitions, as far as at $x \approx 0,75$ the reorganization of structure of solid solution to direct gap happens.

The CL spectra of $\text{Si}_{1-x}\text{Nb}_x\text{C}$ solid solutions was investigated. It is differ already at $x = 0,01 – 0,02$ and the color of the emission changes to red - purple one. One intense band with $\lambda \sim 500$ nm is observed in $\text{Si}_{1-x}\text{Nb}_x\text{C}$ solid solutions CL spectra. The ultraviolet “tail” in the spectra disappears even at small x that indicates on change of nature of radiative centers.

Influence of the crystalline quality of epitaxial layer on the inversion channel mobility in 4H-SiC MOSFETs

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Silicon Carbide (SiC) is a promising material for high power, high frequency and high temperature electronic devices. SiC has many polytypes. Among them, 4H-SiC has wider band-gap and higher bulk electron mobility than 6H-SiC. 4H-SiC MOSFETs, however, show lower inversion channel mobility than that of 6H-SiC [1]. Many researchers have studied the effect of MOS process conditions on the channel mobility of 4H-SiC MOSFETs [2-4]. However, few investigations on the influence of the crystal quality of epitaxial layers on the channel mobility have been reported. In the present study, we have fabricated MOSFETs on epitaxial layers of different growth lot, and investigated the relationship between the inversion channel mobility and crystalline qualities of epitaxial layer.

As shown in Table 1, we have used three different p-type 4H-SiC epitaxial layers grown on conventional off-angled p-type (0001) Si face substrate for fabricating MOSFETs. Epi A was purchased. Epi B and Epi C were self-made that were grown by low-pressure, hot wall type, horizontal CVD reactor with SiH₄ – C₃H₈ – H₂ – TMA system. The growth conditions were also summarized in Table 1. The crystal quality of epilayers was characterized by Hall effect measurement, AFM, x-ray diffraction and photoluminescence measurement. The MOSFETs were fabricated on these epilayers by the same process. The gate oxidation was formed at 1200°C for 140 min followed by post-oxidation annealing at the oxidation temperature for 30 min in Ar. The details of MOSFETs fabricating were described elsewhere [5].

Table 2 shows the channel mobility (μ_{FE}) and the threshold voltage (V_T) of MOSFETs. The value of the channel mobility obtained from MOSFETs on Epi A and Epi B is the same as that of previous report [6]. On the other hand, the channel mobility of Epi C is about three times higher than that of another epilayers. The fabrication process of these MOSFETs was the same as the process in this investigation. Therefore, the higher channel mobility in Epi C is probably caused by the difference in the crystal quality of epitaxial layers.

Then, we investigated the crystal

Table 1. Characteristics and growth conditions of epilayers

Sample	Epi A	Epi B	Epi C
N_a-N_d (cm ⁻³)	5×10^{15}	1×10^{16}	3×10^{15}
Thickness (μ m)	5	5	5
T_s (°C)		1600	1500
P (mbar)		250	250
H ₂ flow rate (slm)		40	40
SiH ₄ flow rate (sccm)		6.67	3.3
C ₃ H ₈ flow rate (sccm)		3.33	0.88

Table 2. Values of channel mobility and threshold voltage

Sample	Epi A	Epi B	Epi C
μ_{FE} (cm ² /Vs)	6	5.4	14.1
V_T (V)	3.9	3.8	1.9

quality of epilayers. The results are summarized in Table 3. The bulk mobility (μ_H) of Epi C was slightly lower than that of Epi A and Epi B, although the channel mobility of Epi C is higher than that of Epi A and Epi B. The surface roughness (Rms) of Epi C is slightly smaller than that of Epi A and Epi B. The FWHM of x-ray rocking curve of ω scan in three epilayers was roughly the same. As seen above, we could not find clear correlation between the channel mobility and μ_H , Rms and FWHM.

Table 3. Crystal parameters of epilayers

Sample	Epi A	Epi B	Epi C
μ_H (cm ² /Vs)	99	95	91
RMS at 16 μ m ² (nm)	1.2	0.82	0.71
FWHM of XRD (arcsec)	68.8	142.9	73.2

Photoluminescence measurements were also carried out at liquid helium temperature. The 244 nm line of Ar⁺ ion laser was used as the excitation source. Zero phonon luminescence line of the neutral aluminum acceptor and phonon spectra of the neutral nitrogen donor bound excitons were observed in both epilayer as shown in Figure 1. The broad peak due to Aluminum related donor-acceptor (D-A) pair peak was also observed around 420 nm. In this figure, the intensity of spectra was normalized by that of D-A pair peak due to comparison of the PL intensity. The intensity of near band-gap emission with Epi C is quite strong as compared with that of Epi A and Epi B as can be seen from Figure 1. This indicates that the crystalline quality of Epi C is better than Epi A and Epi B. In conclusion, it is found that the channel mobility has a correlation to crystalline quality observed at the intensity of the near band-gap emission. The channel mobility becomes higher when the intensity of near band-gap emission is strong.

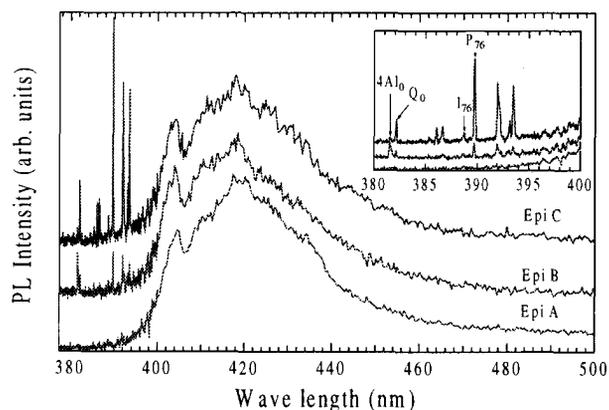


Figure 1 Photoluminescence spectra of epilayers. Near band-gap emission of epilayer is shown in the inset.

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Full band Monte Carlo simulation of electron transport in 3C-SiC

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ABSTRACT

Silicon Carbide is a very interesting semiconductor material for high temperature, high frequency and high power applications. The main reasons are its high saturation velocity, large thermal conductivity, high Schottky barriers and large breakdown voltages.

High quality 4H-SiC and 6H-SiC polytype substrates and epitaxial layers are commercially available today. 3C-SiC has been grown successfully in the form of films on Si(100). There are several theoretical studies on the charge transport in 3C-SiC.

However, we present the first full band MC simulation of the electron transport at high electric fields. The full band Monte Carlo model is based on an ab initio band structure calculation using the Local Density Approximation (LDA) to the Density Functional Theory (DFT). The following scattering processes have been considered, acoustic phonon scattering, polar and non-polar optical phonon scattering, ionized impurity scattering as well as impact ionization. Fully k-dependent scattering rates for the phonon interactions and the transition rate for the impact ionization process have been directly extracted using the wave functions and the energy dispersion of the ab initio band structure. Coupling constants for the acoustic and the non-polar optical processes have been deduced from experimental data for the mobility as a function of temperature.

In Fig. 1. the simulated mobility as a function of temperature has been compared with experimental data by Yamanaka et al. [1]. The simulations are in very good agreement with the measurements. The saturation velocity in 4H-SiC and 6H-SiC has been measured to be close to 2.0×10^7 cm/s for an electric field applied perpendicular to the c-axis. There is no experimental data available for 3C-SiC. However, our simulations indicates that the value should be close to 2.2×10^7 cm/s which is in good agreement with results from the analytical Monte Carlo model used by Mickevicius et al. [2] (see Fig. 2.) and the measured values for 4H- and 6H-SiC. The effective mass in 3C-SiC is smaller for electrons than for holes and the impact ionization coefficients for electrons are expected to be higher than for holes. In Fig. 3. we present our simulation results together with the full band MC results by Bellotti et al. [3] for holes. The electron initiated impact ionization process is found to be much stronger than for holes, from 2 to 10 times stronger depending on the strength of the electric field.

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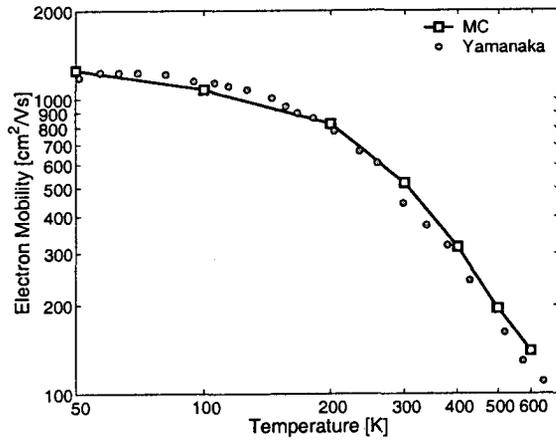


Figure 1. Electron mobility as a function of electrical field.

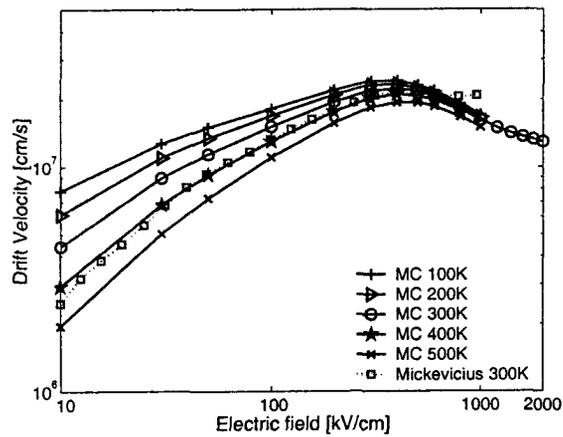


Figure 2. Drift velocity as a function of electrical field, plotted for different temperatures.

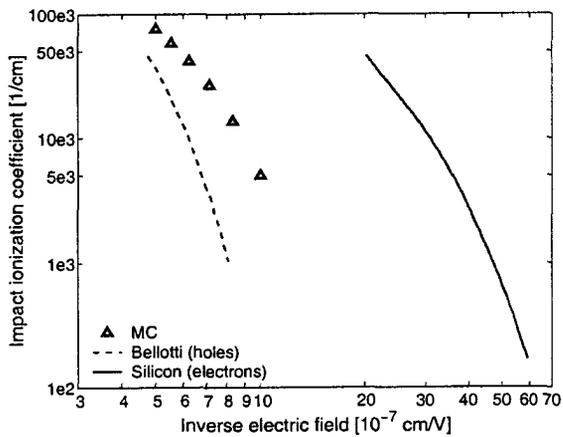


Figure 3. Electron ionization coefficient plotted for inverse electrical field.

Analysis of the surface damage caused by mechanical polishing of SiC wafers

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Dislocation free Lely platelets have been mechanically polished and used as seeds for the Physical Vapor Transport growth of 6H-SiC polytype. The type, density, and distribution of threading dislocations in the SiC overgrowth close to the interface has been analyzed by transmission electron microscopy (TEM) and interpreted in terms of the polishing-induced damage in the seed crystal.

Several characteristic features of dislocation distribution have been observed. Most of the threading dislocations present in the overgrowth are perfect edge dislocations propagating along [0001] direction with Burgers vector of $1/3\langle 11-20 \rangle$. The dislocations are arranged in form of cells typically between 0.2 – 0.5 μm in diameter with the nearly defect free central portion of the cell and high dislocation density along the cell walls. Walls are preferentially aligned along $\langle 1-100 \rangle$ directions with the average distance between neighboring dislocation of 0.05 μm . Such cell structure is consistent with a layer of a seed crystal distorted during polishing and rotated around the c-axis (and parallel to the basal plane) by approximately 1 degree. For this mechanism, the total Burgers vector for all dislocations in a single cell should be zero. An experimental evidence for this will be presented.

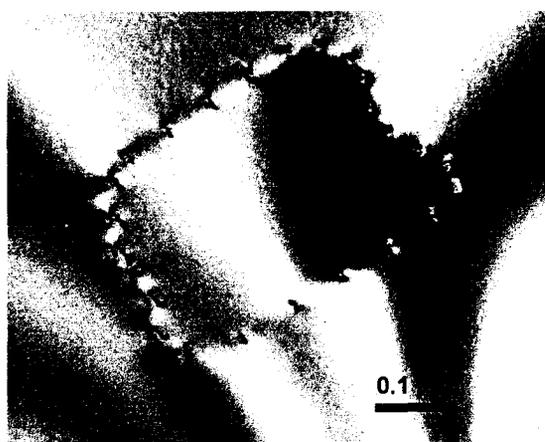


Fig. 1 Transmission electron microscopy image of a polishing-induced cell of threading edge dislocations.

The density of screw dislocations is approximately 10^5 cm^{-2} in the overgrowth and more than an order of magnitude lower than edge dislocation density. Threading screw dislocations are distributed in pairs with the average distance between nearest neighbors of about $0.3 \mu\text{m}$. The Burgers vectors of screws in a pair dislocations are equal $1c$ and have opposite sign. A model for the polishing-induced deformation responsible for such configuration will be presented.

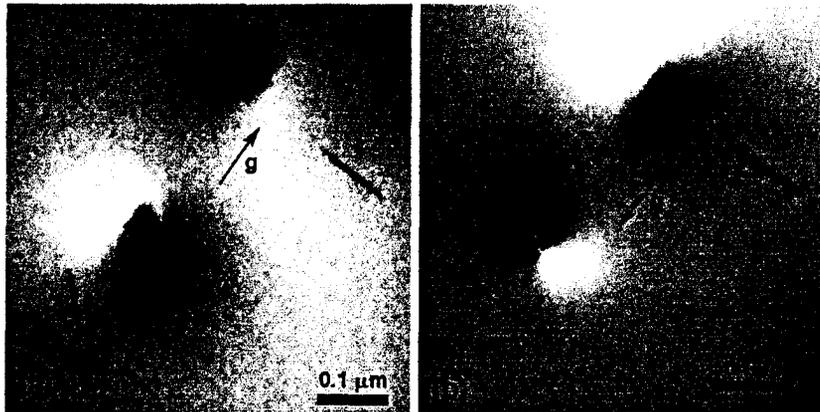


Fig. 2 Transmission electron microscopy image of a pair of threading screw dislocations

Gallium Nitride Metal-Insulator-Semiconductor Capacitors Using Low-Pressure Chemical Vapor Deposited Oxides

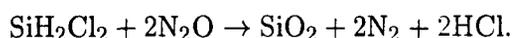
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Metal-Insulator-Semiconductor FETs (MIS-FETs) require low interface-state density interfaces in order to achieve gate-controlled devices. Also, interfaces play a key role in the DC, AC, and transient behavior of semiconductor devices, by providing locations for charge trapping and emission. Charge trapping at GaN-passivation interfaces can cause drain pinch-off, delayed turn-off transients, and reduced breakdown voltage. For the fabrication of GaN MIS-FETs, suitable dielectric materials and processes must be developed.

This study compares two low-pressure chemical vapor deposited (LPCVD) oxides on n-type GaN, namely a Low-Temperature Oxide (LTO) and a High-Temperature Oxide (HTO). On the unintentionally-doped n-type GaN samples, LTO was deposited at 450°C following the reaction:



and the HTO was deposited at 900°C according to the reaction:



In both cases the target thickness was 50 nm, and aluminum dots were formed by evaporation

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through a shadow mask. A large area capacitor was used as an effective substrate contact and was observed to be equivalent to the use of an indium ohmic contact. Using this dual-capacitor technique with a small capacitor diameter of 0.5 mm, capacitance-voltage (C-V) characteristics and conductance-frequency (G- ω) characteristics of the two samples were measured.

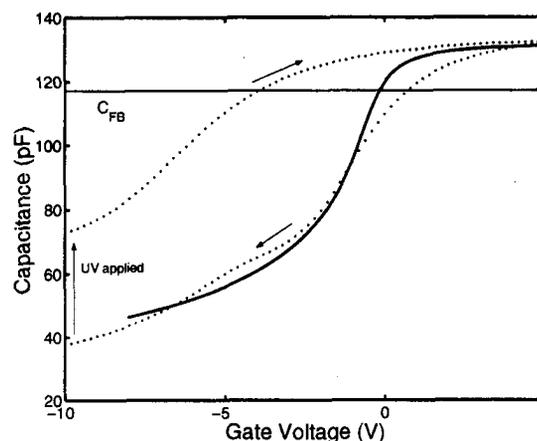


Figure 1: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for LTO sample with UV excitation at -10 Volts.

As shown in Figure 1 for the LTO capacitor, the capacitors are biased from accumulation and reach deep-depletion. With ultraviolet (UV) light incident upon the sample, the capacitance reaches a steady-state inversion capacitance. The UV light causes a negative flat-band voltage shift by emptying trapped electrons, with

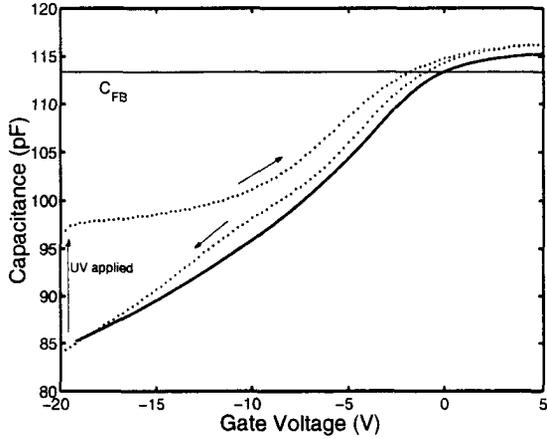


Figure 2: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for HTO sample with UV excitation at -20 Volts.

flat-band voltage is given as

$$V_{FB} = \Phi_{MS} - \frac{Q_f + Q_{it}}{C_{ox}} \quad (1)$$

From the flat-band shift of the LTO sample, Q_f and Q_{it} are calculated as 1.6×10^{12} and -2.0×10^{12} q/cm², respectively. Similarly, the HTO sample (Figure 2) exhibits lower Q_f and Q_{it} values, 6.4×10^{11} and -3.1×10^{11} q/cm², respectively. The C-V characteristic of the HTO sample shows only slight hysteresis when measured without UV light (Figure 3).

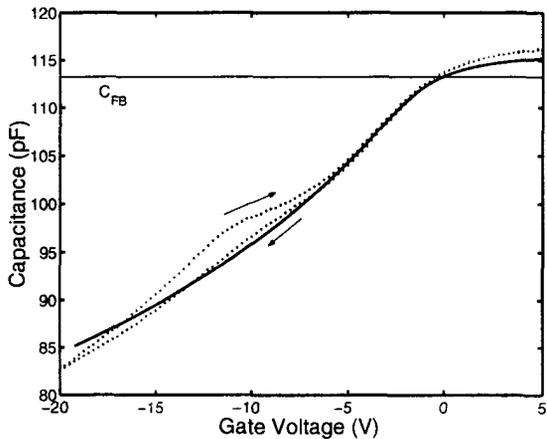


Figure 3: Measured (dotted) and ideal (solid) C-V curve at 1 MHz for HTO without UV excitation.

The G- ω technique is used to characterize

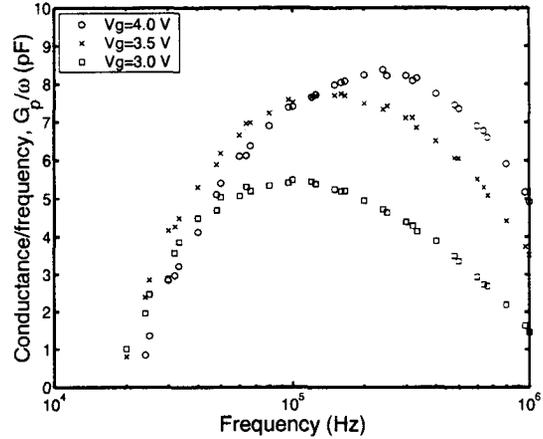


Figure 4: Conductance-frequency (G- ω) measurements on LTO sample.

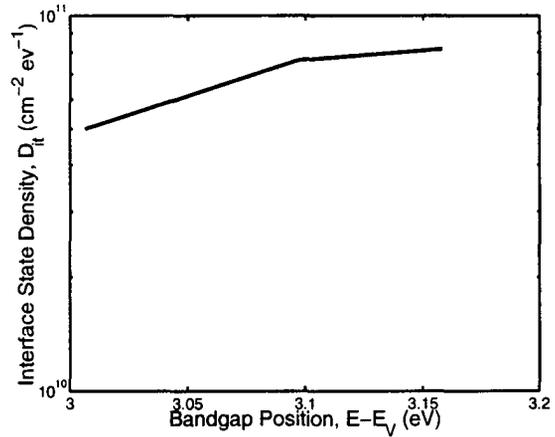


Figure 5: Interface-state density on LTO sample extracted from conductance-frequency (G- ω) measurements.

the interface-state density on the LTO sample as shown in Figure 4. The interface-state density near the conduction band is $\approx 8 \times 10^{10}$ cm⁻² eV⁻¹ as shown in Figure 5.

MOS capacitors using LTO have been fabricated on n-type GaN with an interface-state density of $\approx 8 \times 10^{10}$ cm⁻² eV⁻¹. Capacitors with the HTO dielectric show a lower flat-band voltage shift with the application of ultraviolet light and are expected to have less fixed charge and a lower interface-state density than LTO capacitors. These results indicate that LTO and HTO LPCVD oxides are viable for GaN MISFET device gate dielectrics and passivation layers.

Characteristics of mobile ions in the SiO₂ films of SiC-MOS structures

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SiC (silicon carbide) is one of the most promising semiconductor material for high-power and high-frequency devices due to its wide bandgap, high breakdown field, high electron saturation velocity, and high thermal conductivity. SiC surface can be thermally oxidized in the same way as used for Si. The existence of mobile positive ions in SiO₂ layers of MOS (metal-oxide-semiconductor) structures is one of the important sources of instabilities in MOS devices. The behavior of these ions in Si-MOS devices has been extensively studied in order to stabilize the device parameters.

Capacitance-voltage (C-V) & thermally stimulated currents (TSC) methods have been applied to characterize the mobile ions of MOS structures[1,2]. In this study, the characteristics of mobile ions in thermally grown oxide layers of 6H-SiC MOS capacitors are investigated by C-V and TSC measurements.

MOS samples used in this study are Au/SiO₂/6H-SiC structures. The wafers used were 6H-SiC epitaxial layers prepared by thermal CVD on n+ 6H-SiC (0001)Si-face substrates with 3.5° off-angle, which had undoped layers with doping concentration of about $1 \times 10^{16} \text{cm}^{-3}$. Oxide layers were obtained by thermal oxidation using dry oxygen or wet oxygen (95°C steam, O₂ bubbling) at various conditions, and post-oxidation annealing was performed at 1150~1250°C for 30 min in Ar-ambient. For the fabrication of MOS capacitors, gate electrodes were formed by sputtering of Au-dots with 200~500 μm diameters, and backside ohmic contacts also formed by sputtering of W or Ni. In order to investigate the characteristics of mobile ions in oxide layers of SiC-MOS capacitors, C-V and TSC measurements were performed.

C-V characteristics of the MOS capacitors were measured at room temperature (300K) using a 1MHz C-V plotter in the dark. Figure 1 shows the C-V characteristics of a wet oxidized sample measured at 1MHz. In this case, it seems that the inversion does not occur and the depletion layer spreads widely, probably owing to the absence of minority carriers because of the large bandgap of 6H-SiC[3]. After a C-V measurement at room

temperature, appropriate bias-temperature (B-T) stress is applied to a sample at an elevated temperature and then the sample is cooled down to room temperature with bias voltage still applied in order to measure the TSC. Then the sample is heated at a constant rate, and the short circuited current is measured. Figure 2 shows a typical TSC peak in the SiO₂ film of a wet oxidized 6H-SiC MOS capacitor. The bias voltage $V_b = 3.0V$ is applied at a temperature $T_b = 460K$ for $t_b = 1.0$ min. and the heating rate β is 0.1K/sec. It is found from Fig. 1 that a single peak is observed at $T_p = 450K$ in the measured temperature ranges, and the peak is generated by positive mobile ions. The activation energy and Q_{TSC} obtained from the TSC curves increase as the bias voltage V_b increases.

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Acknowledgment

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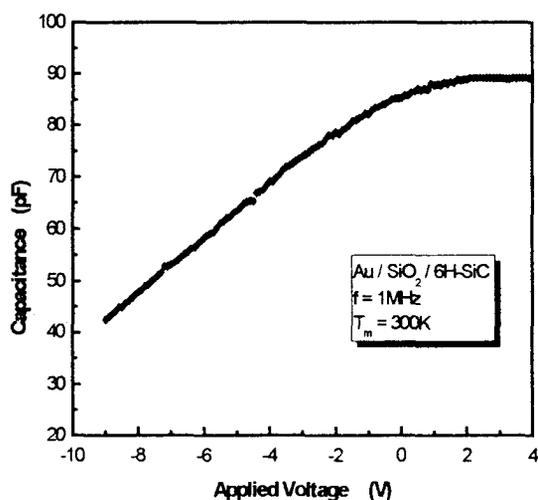


Fig. 1 C-V characteristics of a wet oxidized 6H-SiC MOS capacitor measured at 1MHz in the dark.

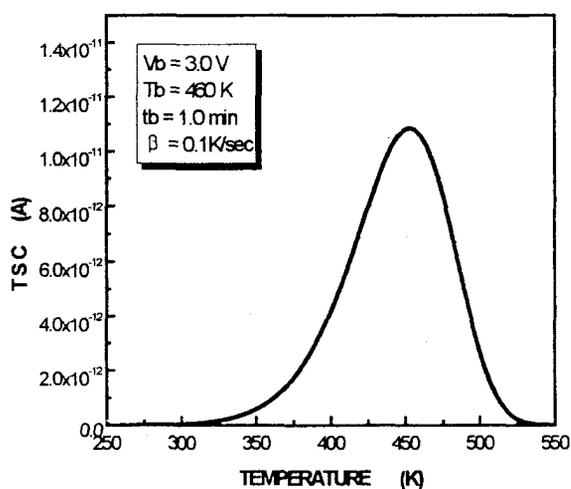


Fig. 2 A typical TSC peak in the SiO₂ film of a wet oxidized 6H-SiC MOS capacitor.

TEM (XHREM) and EDX studies of 6H-SiC porous layer as a substrate for the subsequent homoepitaxial growth

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Since the first report on electrochemical etching of bulk SiC crystal in hydrofluoric acid solution [1], large attention has been drawn to better understand physical properties of the material commonly known as a porous silicon carbide (PSC)[2,3]. In these papers the optical properties were being related with the microstructure of porous layers. Besides, hexagonal form silicon carbide, e.g. 6H-SiC polytype, is used as a substrate for growing high quality of GaN epitaxial layer and creating of semiconductor devices. This technology presents certain demands to the structural quality of bulk silicon carbide, whereas used for above purpose crystals (CREE) content micropipes and threading dislocations (10^2 cm^{-2}), which are inherited by epitaxial layer. Therefore the problem of receiving of the perfect substrates for the fabrication of the epitaxial technology based electronic devices continues to exist [4,5].

This paper focuses an attention on the microstructure analysis of the substrate/PSC/SiC epilayer cross-section by TEM (HREM). Misoriented by 3.5° , with respect to the c axis, commercial 6H-SiC crystal (CREE) was subjected to the electrochemical etching in $\text{HF} : \text{H}_2\text{O} : \text{C}_2\text{H}_5\text{OH} = 1 : 1 : 2$ solution at the illumination of the sample surface with UV light. At current density 10 mA/cm^2 and time of electrochemical etching 30 min the $34 \mu\text{m}$ thick pore layer was obtained. 6H-SiC $12\mu\text{m}$ thick epilayer was grown by the sublimation in vacuum over the PSC.

EM 4000EXII and EM 3000F electron microscopes were utilized. EDX spectra from area as small as 3 nm were recorded using SiLi detector. For preparing cross-section sample the conventional procedure (grinding, polishing, dimpling and Ar ion milling) was used. It was shown that the substrate-porous layer boundary is extremely sharp unlike the upper boundary (porous layer-epitaxial one), which was subjected to sublimation etching prior the epitaxial growth. In addition, the porous layer is inhomogeneous along the layer thickness: near the upper interface there is $\sim 1.5\mu\text{m}$ thick porous layer with enlarged pores in size (Fig.1). Near the bottom interface, at low magnification pores look like triangles. They are stacked and form the chains elongated approximately on the c- axis direction. Close to the upper boundary at intermediate magnification (100K) the pores seem as truncated triangles and in the shape they remind hexagons. At least one facet of the pore independent upon its size has the sharp interface parallel to the basal plane. Some images show clearly the amorphous structure of the internal surface of pores. High resolution image of pore crystalline-amorphous boundary show the gradual transition from crystalline region to amorphous one of the pore, certain atomic planes in this region being become diffused in character (Fig.2). Stronger contrast of (0001) lattice planes in the immediate vicinity of pores indicates on the stacking fault formation. The selected area electron diffraction pattern feature

in view of streaks in [0001] direction confirms the appearance of two-dimensional defects in the porous layer.

Comparison of EDX spectra recorded for different regions of cross-section sample shows that the amorphous internal surface of pore is significantly enriched by carbon (Fig.3). As to content of carbon in the epitaxial layer at the immediate vicinity of the porous layer, it is also higher than in SiC standard (substrate). The results received allow us to suggest that during electrochemical etching the selective extraction of silicon atoms occur. This process and high temperature growth give rise to the appearance of stacking faults and amorphous areas in the porous layer. No threading dislocations and any another defects have been observed in the epitaxial layer at all.



Fig.1. XTEM image of structure of porous layer at the vicinity of the epilayer



Fig.2. XHREM image of crystalline-amorphous part of pore

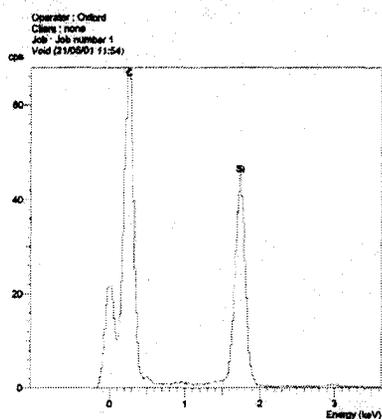


Fig.3a. EDX spectrum from the region containing the pore amorphous part

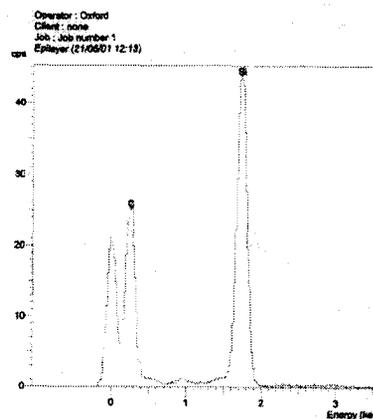


Fig.3b. EDX spectrum from the region of epilayer in the vicinity of porous layer

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Measurements on linear TLM structures with TiW/Ti/Pt contacts for corrosive and high temperature applications

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Catalytic metal insulator silicon carbide, MISiC sensors, are routinely operated up to 600°C and short periods up to 1000°C [1]. The speed of response, when changing between an oxidising and reducing ambient at temperatures $\geq 600^\circ\text{C}$ is a few milliseconds [2]. Applications like cylinder specific monitoring in exhaust gases of a car engine, synthetic exhaust diagnosis, and flue gas monitoring have been demonstrated [3, 4]. We have used both Schottky diodes and transistor devices. Gas sensitive MISiCFET devices with catalytic gate metal have been designed and processed by ACREO AB [5]. They combine the advantage of high temperature stability, since these devices have a thick insulator, with simple electronic circuitry. The MISiCFET devices have been used in several high temperature applications [1].

Ohmic contacts, as well as an insulator, that performs in an oxidising atmosphere at temperatures up to 600°C are required for the MISiCFET devices used for car applications. The ohmic contacts to the 4H SiC used for the first three batches of transistors were made of evaporated Ni, 100 nm, annealed in an argon flow for 10 min at 950°C. On top of the Ni, 200 nm TaSi_x and 400 nm Pt was sputtered as a protection to corrosion and to enable the bonding of gold wires. Linear TLM structures of this contact were tested and preliminary results were recently published [6].

Lee *et al.* has demonstrated earlier that TiW contacts on both p- and n-type 4-H SiC show good behaviour at high temperature under vacuum conditions [7]. We have performed further testing in corrosive environments. The contacts consists of 180 nm sputtered TiW, annealed at 950°C for 30 min. On top of this a 30 nm Ti layer and sequentially a 300 nm Pt layer were deposited using an e-beam evaporator. The top Pt top layer performs both as protection of the corrosive ambient and to improve gold bonding to the contacts. Linear TLM structures were processed and cut in 2x2 mm chip, which were glued on a heater. The heater is mounted on a 16-pin holder, which is put in an Al-block with a gas flow channel. A Pt-100 element is also glued on the heater for temperature control. Measurements of the resistance between the contacts were made with a Keithley 192 using four-point measurement technique.

Fresh samples had a specific contact resistance, ρ_c , of around $1 \times 10^{-5} \Omega/\text{cm}^2$. Annealing in an oxygen containing ambient is interesting because many high temperature sensor applications involve that. The specific contact resistance was measured at the annealing temperature. The

results for two linear TLM contacts annealed at 500 and 600°C, respectively, in 2 % O₂ in N₂, is shown in Fig. 1. The contacts show a stable contact resistance at 500°C and some drift at 600°C in the oxidising atmosphere. To simulate car exhaust applications the contacts were exposed to a sequence of 3 min of 0.4 % O₂ in N₂, and 1 min of 1 % H₂ injected into this background gas, i.e. 3 min of oxidising ambient and 1 min of reducing ambient. During this annealing the contacts increased their specific contact resistance considerably, see Fig. 2, and it also had a detrimental effect on the gold bonding. Further testing of the long-term stability of the contacts will be performed at different temperatures.

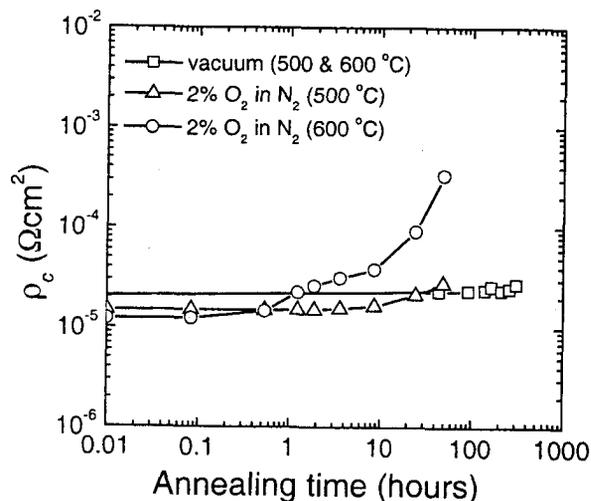


Figure 1. Contact resistance measured at the annealing temperature in 2 % O₂/N₂ at 500 and 600°C, respectively. In vacuum the temperature was 500°C for the first 140h and then 600°C for the final 168h [7].

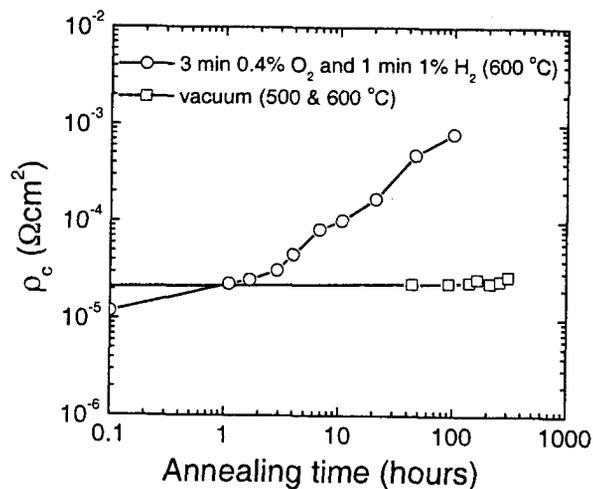


Figure 2. Contact resistance measured at 600°C in an alternating reducing and oxidising atmosphere.

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Point-contact current voltage technique for depth profiling of dopants in silicon carbide

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Introduction

Carrier concentration depth profiling is important in R&D of semiconductor devices, and many techniques have been invented. For silicon devices, spreading resistance profile (SRP) is useful since it has high spatial resolution and wide dynamic range. When SRP is applied to SiC, sensitivity of SR to doping concentration becomes low and the detectable concentration is limited to about 10^{17} cm^{-3} [1]. Since the drift layer concentration of high voltage (>1kV) devices is lower than about 10^{16} cm^{-3} , more sensitive technique is needed. For wider band gap materials, point-contact current voltage (PCIV), which is similar to SRP, is known to have higher sensitivity than SRP. SRP measures current at a low constant voltage between two-probes, on the other hand PCIV measures voltage at a constant current (Fig.1). We applied PCIV to characterize the doping profile of 4H-SiC.

Experimental

As the substrate, (0001)Si face of n-type 4H-SiC from Cree Inc. was used. The SiC wafer had a 10- μm -thick n-type epilayer with doping concentration of $1 \times 10^{16} \text{ cm}^{-3}$ and a n-type substrate with doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$. Phosphor is implanted for 2×10^{15} ions/ cm^2 with four energies up to 180kV as a ohmic contact layer, and activated at 1800°C. PCIV measurements were performed by a conventional SRP system, SSM-150 combined with SSM-350 from SSM Inc.

Results

Figure 2 shows current-voltage characteristics of point-contact for doping concentration of 10^{16} cm^{-3} and 10^{19} cm^{-3} . The sensitivity of PCIV is determined by the voltage difference between the 2 curves. Though the voltage difference becomes large with current, it is limited by maximum voltage of potentiometer. We choosed 50nA as the constant current and depth profile is obtained as shown in Fig.3. Fig.3(a) shows doping profile of n/n⁺ substrate showing flat doping in epilayer. Fig.3(b) shows doping profile of P implanted layer. PCIV result matches the TRIM calculated results.

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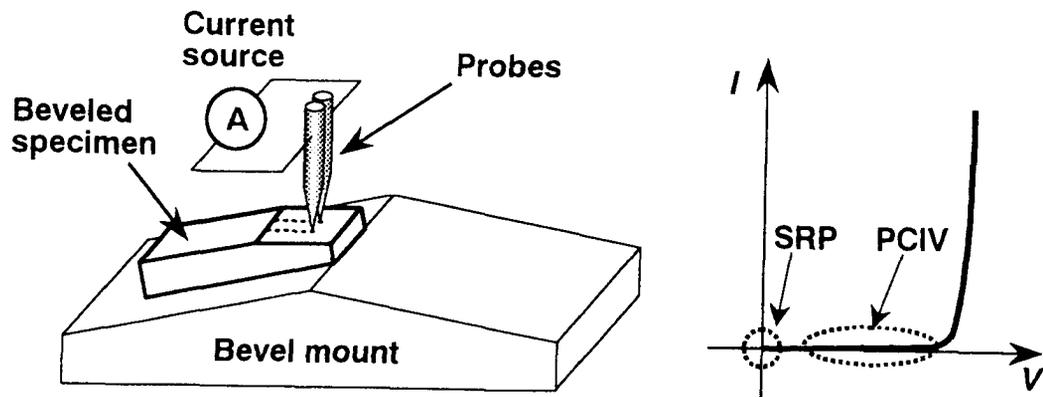


Fig.1 Schematic illustration of PCIV measurement. PCIV uses two probes as SRP, but uses a constant current source. PCIV measures higher voltage compared to SRP.

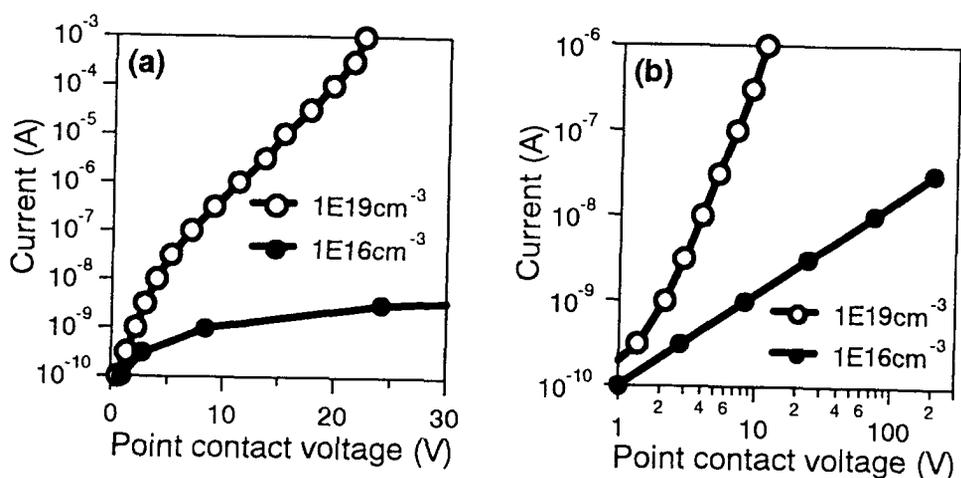


Fig. 2 Current voltage characteristics of point contact to 4H-SiC. Between 10^{-9} to 10^{-7} A, point-contact voltage changes almost linearly.

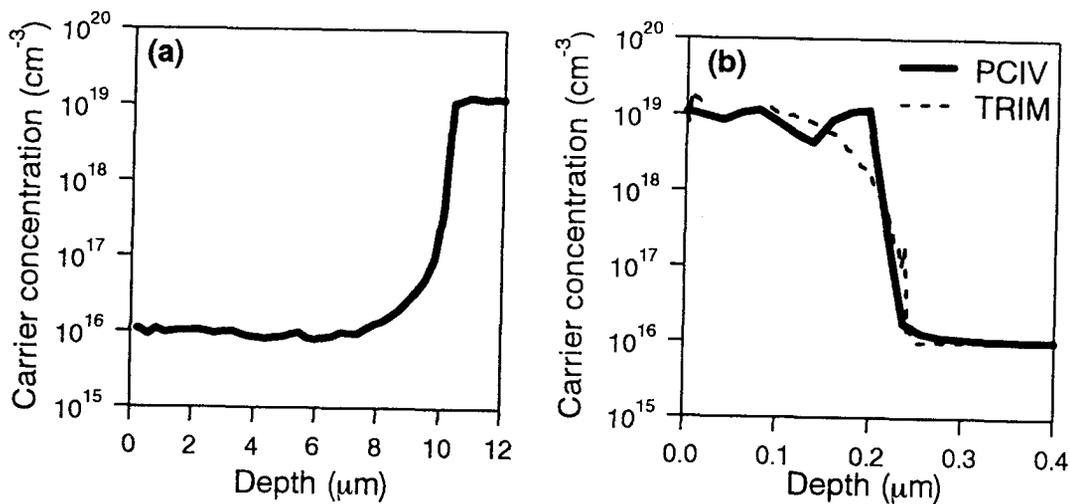


Fig. 3 Doping profile of (a) n/n^+ 4H-SiC substrate and (b) P implanted layer obtained by PCIV. In (b), simulated curve by TRIM is also shown.

Thermal conductivity and acoustic characterization of porous SiC

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ABSTRACT

Substrates were half-masked during anodization so that an epitaxial layer may be grown directly on both conventional 'STD' and porous 'PSC' substrates for comparison purposes. [1]. We will report on ultrasonic investigations of acoustic wave transport through both the porous surface regions and overgrown films on both as-received and porous surfaces. Both transmission and reflection measurements have been made. Acoustic inspection, in the frequency range of a few hundreds of MHz, is recognized as an advanced, non-destructive method for testing electronic materials for state-of-the-art microelectronic applications. Typical goals of acoustic imaging are to resolve and characterize internal bulk defects, delamination in packaged devices, and thin dielectric film metrology. Traditional Scanning Acoustic Microscopy (SAM) involves the use of peak amplitude information acquired while raster-scanning over a sample, to produce horizontal cross section images. One of important SAM features is a possibility to perform Tomographic Acoustic Micro Imaging (TAMI) where the entire image can be split into individual cross-sectional scans, analogous to physical sectioning of the sample.

We performed SAM in the TAMI mode to characterize and compare the elasto-mechanical properties of two 6H-SiC (0001)Si face off-axis wafers [2] SiC wafers prepared to be half control, half nanoporous by surface anodization utilizing an electrochemical cell, details of which are presented elsewhere [2]. Each wafer was processed to create a 3 μm or 12 μm thick porous layer on half of the substrate. With this approach the standard sample (STD) and porous sample (PSC) are on the same wafer. SAM was performed using the commercially available UHR-2000 system from Sonix, Inc. Measurements were performed at an operating frequency 260MHz in the pulse-echo mode. We also compared reflected and transmitted pulses at 75MHz frequency. The result of the TAMI scan taken on the wafer with the 12 μm thick porous layer is presented in Figure 1. The vertical line shows a border between the PSC (left) and STD (right) part of the wafer. Besides various micro-defects at the center of the wafer, the most remarkable feature is an enhanced acoustic reflection from the porous side (more white contrast). In different places on the wafer, the PSC displayed a 25-35% higher reflection

than the STD half. The scans correspond to the acoustic pulse reflected from the back surface of the substrate. In contrast, the SAM measured on the 3 μm thin PSC sample (not shown) reveals only minor variance between porous and reference halves. This difference is again towards a higher reflection from the porous side. We repeated the SAM study on the same wafers after deposition of 3-4 μm n-type SiC epitaxial layers on both full wafers. The result was very consistent with acoustic images of the pre-epi wafers. The 12 μm thick PSC region shows a higher acoustic pulse reflection compared to the STD region. Also, a minor difference was observed in a case of 3 μm porous layer.

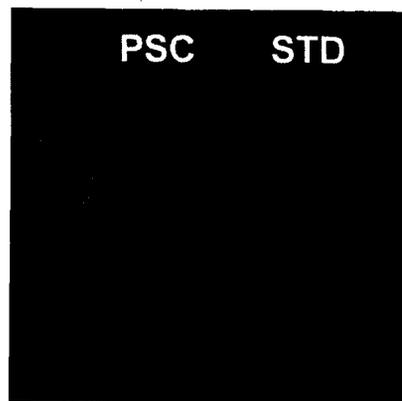


Fig. 1 TAMI scan taken on the wafer with 12 μm porous layer. Note that the porous region (PSC) has a lighter contrast indicating the material is of higher quality than the standard substrate region (STD).

Scanning thermal microscopy (S_{Th}M), which provides nondestructive, absolute measurements of the thermal conductivity (κ) with a spatial/depth resolution in the 2-3 μm range [3], was used to examine the room temperature κ of porous and non-porous SiC material. Wafers examined were processed in the same manner as described above. Thermal results were acquired by point-by-point type investigation on both halves of two samples labeled A and B. The porous film thickness was 3.5 μm (sample A) and 15 μm (sample B), respectively. For both investigated samples κ was found to be higher on the PSC region when compared to STD regions - about a 12% increase on sample A and 10% on sample B, respectively. Atomic force microscopy (AFM) investigation reveals that the influence of the surface roughness effects on κ cannot account for the observed behavior. A competition between a decrease in the phonon mean-free path and an increase of the specific heat of the porous material, with the predominant term being the specific heat, could account for these observations. The implications of these findings for device applications and design are being considered. These results are consistent with the SAM characterization, which was conducted independently. Results of these investigations will be presented along with initial thoughts on a model for the transport of phonons in PSC material.

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4H-SiC \Rightarrow 3C-SiC Polytypic Transformation during Oxidation

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Abstract

We have observed a 4H-SiC \Rightarrow 3C-SiC polytypic transformation in a highly doped n-type 4H-SiC epilayer following thermal dry oxidation. In addition to the 3.22 eV peak of 4H-SiC, cathodoluminescence spectroscopy (CLS) after oxidation revealed a spectral peak at 2.5 eV photon energy believed to correspond to 3C-SiC, that was not present in the sample prior to oxidation. To the best of our knowledge, the optical and structural results reported here are the first observation of a polytypic transformation of SiC (or any other semiconductor) as a result of thermal oxidation. CLS based on low energy electron nanoluminescence (LEEN) taken over a range of incident electron beam energies identifies the presence of localized states and their spatial distribution on a nanometer scale. With increasing excitation energy (E_B) the electron cascade and resultant generation of free electron-hole pairs occur at increasing depths, ranging from 25 nm at 1 keV to 150 nm at 4 keV for SiC's nucleon values and material densities. Electron-hole excitation rates peak at depth values (U_0) which are one-third of electron penetration depths. Fig. 1a depicts the 3.22 eV photon energy observed in the unoxidized sample, which peaks more sharply as E_B increases with further penetration into the epilayer. Emission at lower photon energies corresponds to a broad distribution of states in the band gap confined to the near-interface region. After four hours of oxidation followed by HF oxide stripping, the spectra changed dramatically as shown in Fig. 1b. A sharp 2.5 eV photon peak appears at all depths except 0-30 nm ($0.5 \text{ keV} < E_B < 1 \text{ keV}$) from the metal/SiC interface, while a broad 3.2 eV photon peak slowly decays over the first 20 nm. The 2.5 eV emission at all depths probed indicates a substantial structural change occurring over hundreds of nanometers in the oxidized 4H-SiC sample. Cross section transmission electron microscope (XTEM) image of the as received sample shown in Fig. 2a indicates a uniform lattice structure confirmed by the 3.2 eV LEEN peak to be 4H-SiC. However, the TEM image shown in Fig. 2b of the sample that was oxidized for four hours and the oxide stripped reveals structural changes. Referencing from the top surface, discrete transformation bands (DTB's) of 4H-SiC and 3C-SiC can be seen propagating into the epilayer along the (0001) basal plane, with the thickness of each DTB gradually increasing with distance from the surface. High resolution TEM of Fig. 2c offers a closer look at one of the DTB's with the corresponding enlargement in the inset. The image shows seven Si-C bilayers with a 3C-SiC lattice periodicity sandwiched between 4H-SiC. The 3C-SiC layer is bounded by 4H-SiC structure. The transition boundary from the 3C-SiC to 4H-SiC at the top and bottom may offer clues to the mechanism that initiates the transformation.

We tentatively suggest that the observed polytypic transformation may be due to slipping of Si-C bilayers along the basal plane, which may be a strain relief mechanism due to the heavy doping ($1.7 \times 10^{19} \text{ cm}^{-3}$) of the epilayer on a lightly doped substrate. Hallin *et al.*¹ used Raman spectroscopy to detect dopant-induced lattice mismatch in 4H-SiC, while Matsunami *et al.*² attributed the replication of stacking faults in a $\langle 11\bar{2}0 \rangle$ grown epilayer to difference in doping between an epilayer and a highly doped 4H-SiC substrate. Given the potential adverse effects in some applications, it becomes imperative that this observed transformation phenomenon in the crystal be critically investigated further.

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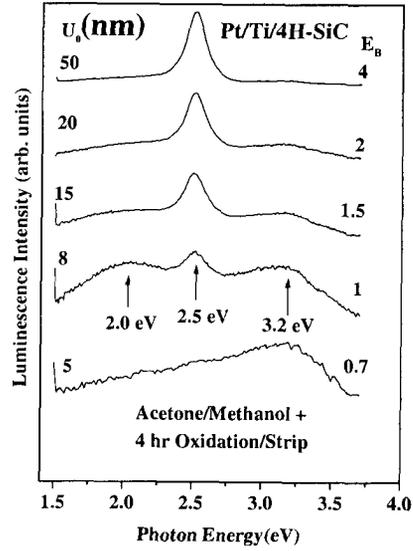
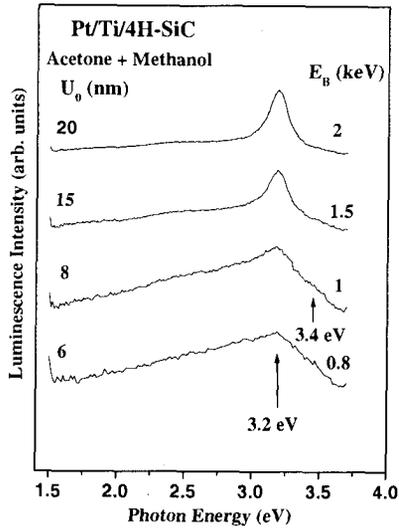


Fig. 1

(a)

(b)

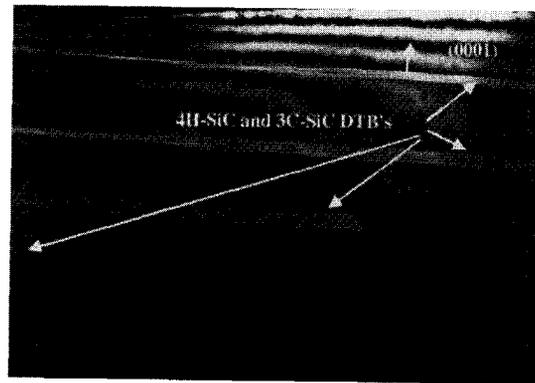
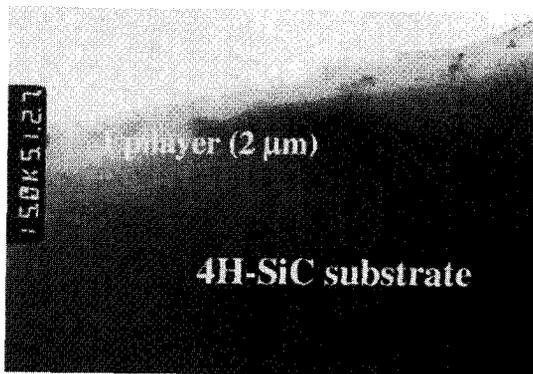


Fig. 2

(a)

(b)

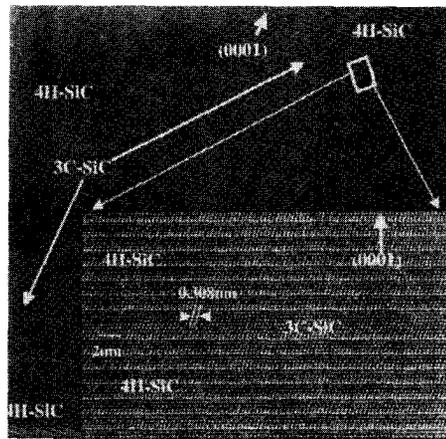


Fig. 2c

On the nature of E_1/E_2 : a DLTS study of neutron irradiated n-type 6H-SiC

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The fluency-dependent properties and the thermal annealing behaviors of neutron-irradiation-induced defects in n-type 6H-SiC have been studied using deep level transient spectroscopy (DLTS). Deep levels NE_1/NE_2 at $E_C-0.36\sim 0.44$ eV and NE_3 at $E_C-0.51$ eV are observed in DLTS measurement temperature range of 100~ 450 K. The energy levels and capture cross sections of NE_1/NE_2 and NE_3 agree well with that of the E_1/E_2 and E_i centers in electron-irradiated 6H-SiC, respectively. The present DLTS results reveal that concentrations of NE_1/NE_2 increase corresponding with decay of NE_3 in the isochronal annealing temperature range 400~ 650 K. The deep level centers NE_1/NE_2 are thought to be the same defects E_1/E_2 . The NE_3 center is attributed to the same defect E_i that has been assigned as carbon vacancy V_C in electron-irradiated experiment. The present results of isochronal thermal annealing behaviors of NE_1/NE_2 support that E_1/E_2 should be differently charged states of carbon vacancy V_C , and argue against that E_1/E_2 were due to divacancy V_C-V_{Si} .

Hall mobility and carrier diffusion investigations in free-standing 4H-SiC epilayers

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Silicon Carbide (SiC) has become the semiconductor of choice for the new generation of semiconductor devices working under extreme conditions. However, still there are only few basic investigations performed on the electrical transport properties of SiC. Recently, the free carrier diffusivity as a key parameter governing plasma behavior in bipolar devices has been studied [1]. Extracted drift diffusivity data using the Einstein relation were compared to the Hall mobility data available in the literature. It was revealed that measured minority-hole diffusion mobility values are lower than majority-carrier (hole in particular) drift mobility values as well as significant difference exists in their temperature behavior. The results suggested that Hall mobility measurements have to be performed on the same set of samples for an appropriate comparison and to assure the structural quality of the material.

In this work we present temperature dependent Hall effect measurements on *n*-type 4H-SiC epilayers grown by chemical vapor deposition (CVD). Free standing 80 μm thick epilayers with extrinsic concentration $n_0 = 10^{15}$ and 10^{16} cm^{-3} were obtained by removing the substrate by polishing to avoid the influence from the heavily doped substrates in the measurements. Ohmic contacts on the epilayers were formed by implanting contact areas with multi-energy nitrogen doses along with subsequent annealing at 1650^o C and electrically contacting them with a silver paste. Extrinsic carrier concentration, carrier mobility and resistivity were deduced from measurement data obtained from Hall effect measurements using a van der Pauw configuration. The Hall scattering factor r_H was assumed to be equal 1. Experiments were performed in the temperature range from 70 to 450 K. The ionization energy and concentration of dopants governing the conductivity type as well as the degree of compensation were determined employing a least square fit of the charge neutrality equation to the experimental carrier concentration data. The charge neutrality equation was calculated numerically applying the material parameters for 4H-SiC.

The obtained Hall mobility values are equal to the highest values reported in the literature (930 cm^2/Vs at 300 K), which assures the structural quality of the material. Nevertheless, the earlier revealed differences remain between the ambipolar diffusion and the recalculated Hall mobilities temperature dependencies. The discrepancy can be attributed to the assumption of a Hall factor $r_H = 1$ in Hall effect measurements in *p*-type 4H-SiC, where its determination is limited due to a low hole mobility. Another explanation is that the minority-hole mobility (ambipolar diffusivity) may be reduced because of electron-hole scattering. Both consequences mentioned above could not be disregarded and also may come in parallel.

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Investigation of the Relationship between Defects and Electrical Properties of 3C-SiC epilayers

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Silicon carbide (SiC) is a promising material for electronic devices used with severe specification. Nowadays, 6H and 4H type SiC wafers are supplied commercially. However, their high price and difficulty to obtain large area prevent the industrialization of SiC devices. 3C-SiC heteroepitaxial growth on Si(100) substrate is one of the attractive ways which resolve problems mentioned. Many researchers have grown 3C-SiC on Si by atmospheric pressure chemical vapor deposition method (APCVD). However, the epilayers have many protrusions on the surfaces and poor surface morphology. As a result, APCVD grown 3C-SiC epilayers could not realize Schottky barrier diodes (SBD) with high reverse breakdown voltages, which is no more than several voltages. We have studied the growth mechanism of 3C-SiC by CVD and have found that the decrease of pressure during the growth brings about the suppression of the reaction between precursor in gas phase, resulting in the decrease of secondary nucleation [1,2]. Consequently, we can obtain atomically flat surfaces without protrusions and antiphase domains by low pressure CVD (LPCVD). The SBDs fabricated using the LPCVD grown epilayers showed good electrical properties, the ideality factor of 1.11 and the reverse breakdown voltage of 240 V [3]. Recently, we have grown 3C-SiC homoepitaxial layers on 3C-SiC thick free standing layers at 1500-1600 °C, and have shown their excellent crystalline quality compared with those of heteroepitaxial layers. However, their SBD characteristics is not sufficient, compared with those on 6H and 4H epilayers. In this report, we study the influence of the defects in epilayers on the characteristics of Schottky barrier junction (SBJ).

Details of the heteroepitaxial growth and homoepitaxial growth of 3C-SiC and diodes fabrication have been described elsewhere [1,3]. 3C-SiC substrates with on-axis (100) surfaces, n type with carrier concentrations of $1 \times 10^{17} \text{ cm}^{-3}$ and the thickness of about 200 μm were supplied by HOYA corporation [4]. We have prepared 3C-SiC homoepilayers grown at different growth rates (2.5-8 $\mu\text{m}/\text{h}$). The properties of the grown layers was examined with a Nomarski differential interference contrast microscopy (NDIC) and the transmission electron microscope (TEM).

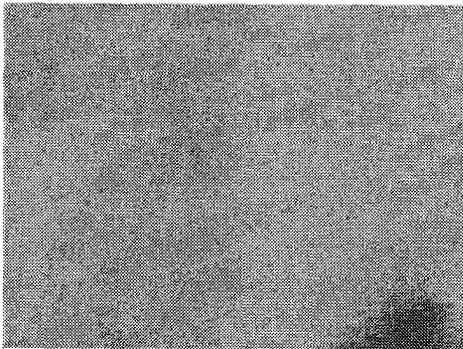
Figure 1 shows NDIC images of surfaces of homo-epilayers. The epilayers grown at the deposition rate of 2.5 $\mu\text{m}/\text{h}$ and 8 $\mu\text{m}/\text{h}$ are shown in Fig. 1(a) and (b), respectively. Macro steps of over 100 nm height and the terrace of less than 0.1 mm width were formed on the surfaces of the epilayers at high deposition rates. The density of macro steps increased with increasing the deposition rate. In order to investigate the origin of the macro steps, the TEM observation of the homoepilayers grown at high deposition rate was carried out. The TEM image near the interface between the homoepilayer and the substrate is shown in Fig. 2. Many line defects (stacking faults, twins, etc) along $\langle 111 \rangle$ directions, which do not exist in the 3C-SiC substrate, were observed in the homoepilayer. Bahng et al. have reported that

macro steps consist of twin bands in the case of 3C-SiC heteroepilayers on Si [5]. Therefore, in the case of homoepilayers, macro steps seem to relate with defects which were observed in Fig. 2. In order to make clear the relationship between the macro step and SBJ characteristics, we fabricated SBDs on many samples with the different densities of macro steps and measured their SBJ characteristics. Figure 3 shows the reverse current-voltage characteristics of homoepilayers grown at the deposition rates of 2.5 and 8 $\mu\text{m}/\text{h}$, respectively. Because we used Schottky electrodes of 0.1 mm in diameter, Schottky electrodes contain at least one macro step in the case of epilayer grown at 8 $\mu\text{m}/\text{h}$. However, the I-V characteristics of the high deposition rate sample is superior to those of low deposition sample, in which Schottky electrodes do not contain macro steps. These results indicate that the macro step do not affect on the breakdown voltage, and the characteristics of SBJ s may be determined by other micro defects.

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(a)



(b)

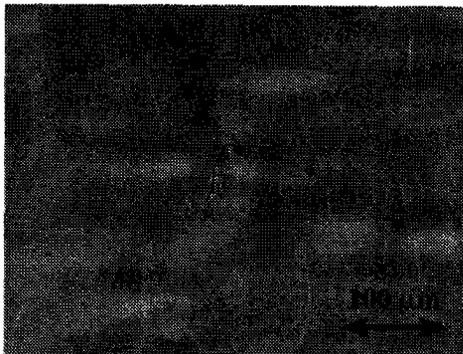


Fig. 1 NDIC image of the surface.
(a) 2.5 $\mu\text{m}/\text{h}$ (b) 8 $\mu\text{m}/\text{h}$

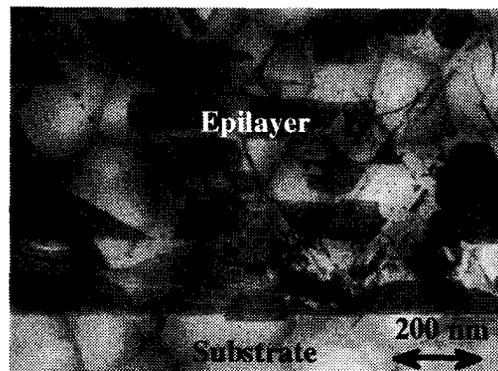


Fig. 2 TEM image of near the interface of homoepilayers and substrates.

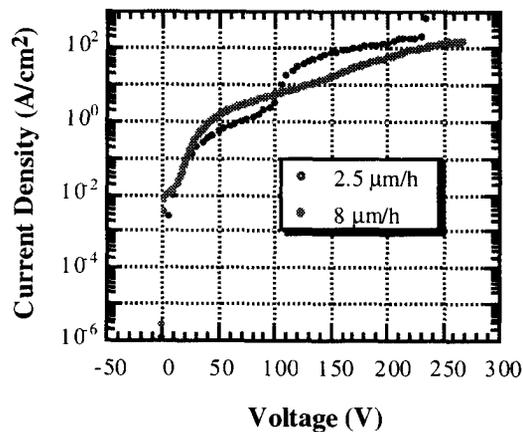


Fig. 3 The reverse I-V characteristics of SBD.

Suppression of Macrostep Formation in 4H-SiC Using a Cap Oxide Layer

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Ion implantation is the only planar, selective-area doping technology available for SiC due to the extremely low diffusion coefficients of dopants. Hence it is necessary to anneal at high temperature for the sufficient activation of dopants, so that macrosteps were easily formed on the surface of 4H-SiC device. Many researchers [1,2] have investigated several methods to suppress macrostep formation during the high temperature activation anneal using silane gas or carbon mask, since such surface ruggedness is known to deteriorating the channel mobility[3].

In order to suppress the macrostep formation we adopted a cap oxide layer thermally-grown or CVD-grown, which is expected to act a role of obstructing the mass flow between the surface of SiC single crystal and the ambient gas. Thermal oxide of 10nm and 50nm thick were grown on SiC wafers to examine the thickness effect of the cap layer. 4H-SiC wafers, supplied from Cree, U.S.A., with an off axis of 8° towards $\langle 11\bar{2}0 \rangle$ were used as starting materials. The non-implanted and Al, B implanted wafers were annealed for 30~40min at the temperature of 1500, 1600, 1700°C, respectively. The samples were loaded into SiC capped graphite crucible and then heated under argon atmosphere. The characterization of surface roughening as well as formation of macrosteps was done using atomic force microscopy (AFM).

The annealing at 1600°C for 30 min resulted in a very clear and well-aligned macrostep structure in the SiC wafers with 10nm thick thermal oxide, as shown in Fig. 1(a). The thermal oxide cap was not found after the heating cycle, which implies that 10nm oxide layer was thin enough to be removed away during the initial stage of annealing and then the surface modification has occurred. It was revealed on the other hand that thicker cap oxide could suppress macrostep formation. Fig. 1(b) shows that no macrostep was found in the sample with a thermal oxide of 50nm thick after the same thermal history of annealing. The thermal oxide layer which was etched out chemically for AFM investigation still remained, even though it was partly damaged and partly evaporated, at the surface of SiC single crystal after the annealing. It means therefore that macrosteps could not be formed at the surface of the off-axis grown SiC single crystal as long as the cap oxide remains during whole the period of high temperature annealing and thus obstructs the mass flow between SiC surface and gas atmosphere. The small pits on the SiC surface in Fig.1(b), which seems to have been created

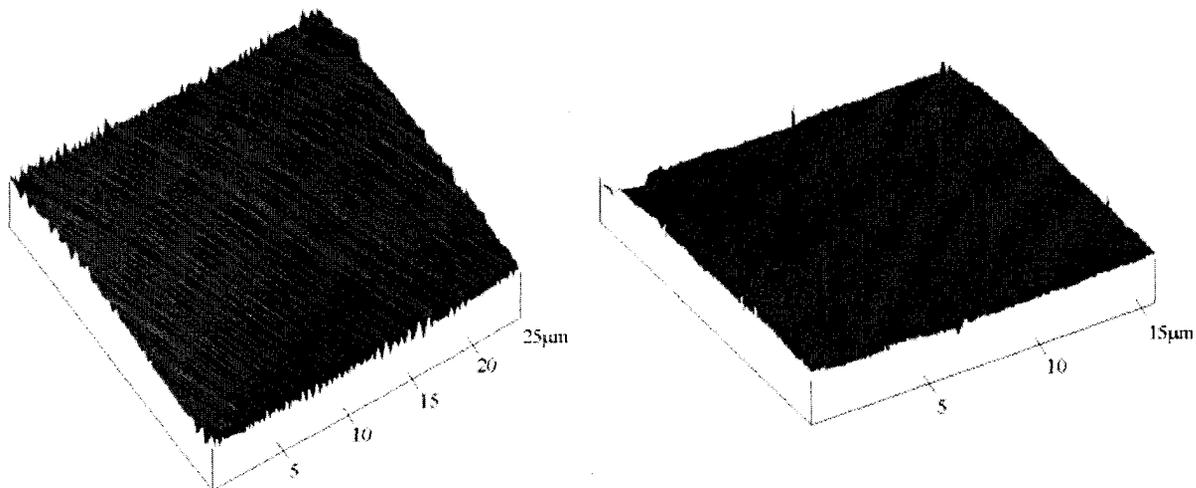


Fig. 1. Atomic force micrographs of high temperature annealed SiC surface. The samples were annealed at 1600°C for 30min with thermal oxide layers (a) 10nm thick and (b) 50nm thick, respectively. A micrograph (a) shows clear macrostep formation, otherwise (b) shows only small height steps.

during the growing of thermal oxide, are under investigation.

The stability of the cap oxide and the surface modification of SiC surface will be presented with respect to the annealing temperature and atmosphere. The characterization of high temperature annealed SiC surface with a thick (~1µm) CVD-grown oxide layer was also investigated and will be presented. The oxide formed and lithographed easily by semiconductor processing can be a good cap layer for suppressing macrostep formation during the high temperature annealing of silicon carbide.

Acknowledgement

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Influences of Implantation Temperature and Dose Rate on Secondary Defect Formation in 4H-SiC

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B⁺ and Al⁺ are used for p-type ion implantation and both ions have advantages and disadvantages, each other. For example, Al⁺ implanted layer is easy for electrical activation and shows little redistribution of dopant by diffusion during annealing but Al⁺ implanted pn junction has larger leakage current than B⁺ implanted one [1]. The difference of reverse properties between B⁺ and Al⁺ implanted pn junctions may be related to the secondary defects formed during annealing. We studied the difference of secondary defect formation between B⁺ and Al⁺ implanted layers by Transmission Electron Microscope (TEM) and showed that at the same volume concentration of implanted ion, density of secondary defect in Al⁺ implanted layer is higher than that in B⁺ implanted layer. On the contrary, mean defect size in B⁺ implanted layer is larger than that in Al⁺ implanted layer [2]. These secondary defects are extrinsic dislocation loops composed of agglomerated interstitials formed by implantation [3]. The volume of the interstitials stored in dislocation loops roughly coincides the amount of implanted ions and this correlation doesn't depend on ion species [2]. This result means that B⁺ and Al⁺ implanted layers have different agglomeration of interstitials, which cause the differences of defect size and density between them. The activation energies of secondary defect formation were estimated for both B⁺ and Al⁺ implanted layers but they are not so different [4]. These activation energies are the self-diffusion activation energy of Si in SiC. From these results, we speculate the difference of secondary defects formation between ion species does not depend on the diffusion of interstitials in implanted layer but is owing to its initial nucleation, which means the secondary defect formation is strongly dependent on as implanted state. In this paper, we show the influences of dose rate and implantation temperature on secondary defect formation in Al⁺ implanted 4H-SiC to clear this speculation.

N-type 4H-SiC wafers with a 10 μ m thick n-type epilayer, obtained from Cree Research Inc., were used for implantations. The donor concentration of epilayers is about $5 \times 10^{15} \text{ cm}^{-3}$. Single energy Al⁺ implantations at 750keV were performed, using microwave multiply charged ion source and radio frequency quadrupole (RFQ) accelerator. This implantation system permits us high dose rate ion injection of 100 μ A. While low dose rate implantation at 8 μ A was also performed as a reference. Implantation temperatures were room temperature (RT) and 1000°C for both dose rate conditions. Post implantation annealings were performed in Ar ambience at 1700°C for 5min using lamp heated furnace.

Figure 1 shows the cross-sectional TEM images obtained from Al⁺ implanted and post-annealed

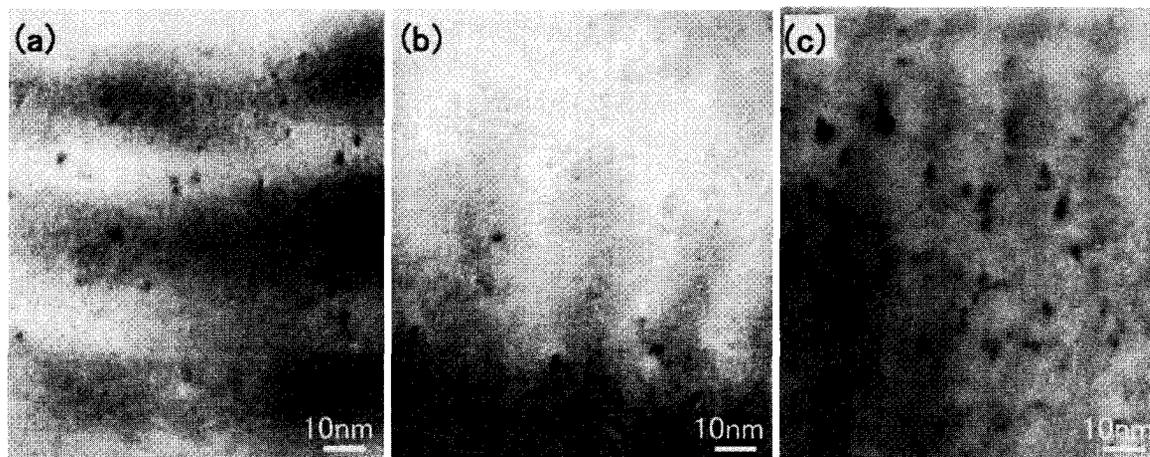


Fig. 1 Cross-sectional TEM images of Al⁺ implanted 4H-SiC. Post-annealing was performed at 1700°C. Dose rates and implantation temperatures are (a) 8 μA at RT, (b) 8 μA at 1000°C and (c) 100 μA at RT.

epilayers. Dose rates and implantation temperatures are (a) 8 μA at RT, (b) 8 μA at 1000°C and (c) 100 μA at RT, respectively. Observations are along <1120> zone axis. In these TEM images, secondary defects are shown as black dots. At the dose rate of 8 μA, secondary defects are reduced when implantation temperature is raised from RT to 1000°C. The mean defect size is also grows from 2.9nm to 4.1nm. On the contrary, defect density increases when dose rate is raised from 8 μA to 100 μA at RT. These results mean that during high temperature implantation, in-situ recombination of interstitials and vacancies is enhanced and supersaturation of them is reduced, which leads to the suppression of nucleation for secondary defect formation. As the result, the density of secondary defects decreases but the mean size of them grows. While, more interstitials and vacancies are survived at the high dose rate implantation than that of low dose rate condition and the increased supersaturation of interstitials causes the enhancement of nucleation of secondary defect formation. In the case of 100 μA at 1000°C, TEM image is similar to Fig. 1 (c). The increase of interstitials by high dose rate implantation is too high to effectively recombine at 1000°C during implantation. As the result, a lot of interstitials are remained after implantation, which leads to high density of secondary defect formation. High temperature implantation is effective only for low dose rate implantation to reduce the secondary defect formation and initial nucleation is also a key for secondary defect control.

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Aluminum and boron diffusion into a-face SiC substrates

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Diffusion as a method of doping SiC has been used for a long time¹. However, only recently it has been demonstrated that this method might be an alternative approach to ion implantation for the formation of selectively doped regions². Diffusion became possible due new technology of graphite mask formation which enables this mask to sustain the high temperatures required for the diffusion process. Since, during selective doping through a mask lateral diffusion occurs as well, diffusion mechanisms and the kinetics of diffusion along the direction perpendicular to *c*-axis (*a*-face) must be studied in detail. Furthermore, because of silicon carbide crystal anisotropy, it is reasonable to expect a difference in impurity diffusion along different crystal orientations.

In this paper, we present a study of boron and aluminum diffusion into 4H-SiC substrates, cut from the same boule, both perpendicular and parallel to *c*-axis.

Single crystal wafers of n-4H-SiC from Bandgap Technologies, Inc. were used, having orientations of (0001), (000 $\bar{1}$) and (1 $\bar{1}$ 00), and background carrier concentration of $4.1 \times 10^{18} \text{ cm}^{-3}$. Boron and aluminum diffusion were carried out simultaneously in argon ambient using an induction heating vertical quartz chamber with water-cooled walls. The temperature and time of diffusion varied from 1900 to 2000°C and from 5 to 15 min, respectively. A graphite crucible with a mixture of silicon carbide powder, elemental boron and aluminum carbide powder (source of the doping atoms) was used. The uniform temperature distribution with minimal gradients and equilibrium SiC vapor pressure were created inside the crucible to avoid undesirable evaporation and/or epitaxial growth during diffusion.

In order to accurately measure the depth profiles of the diffused impurities, secondary ion mass spectroscopy (SIMS) was performed. SIMS data of Fig.1 show that after diffusion at 1900°C for 10 min, both boron and aluminum atoms diffuse about two times faster along the direction

perpendicular to c -axis than parallel to it, while the impurity diffusion along the $\langle 0001 \rangle$ direction is practically the same as that along the $\langle 000\bar{1} \rangle$ direction.

Note, that the aluminum profile in the a-face substrate has a very shallow surface region with higher atomic concentration, while Si- and C-terminated substrates have lower Al concentration in the surface region. Possible reasons for this phenomenon are discussed in the presentation.

Acknowledgments

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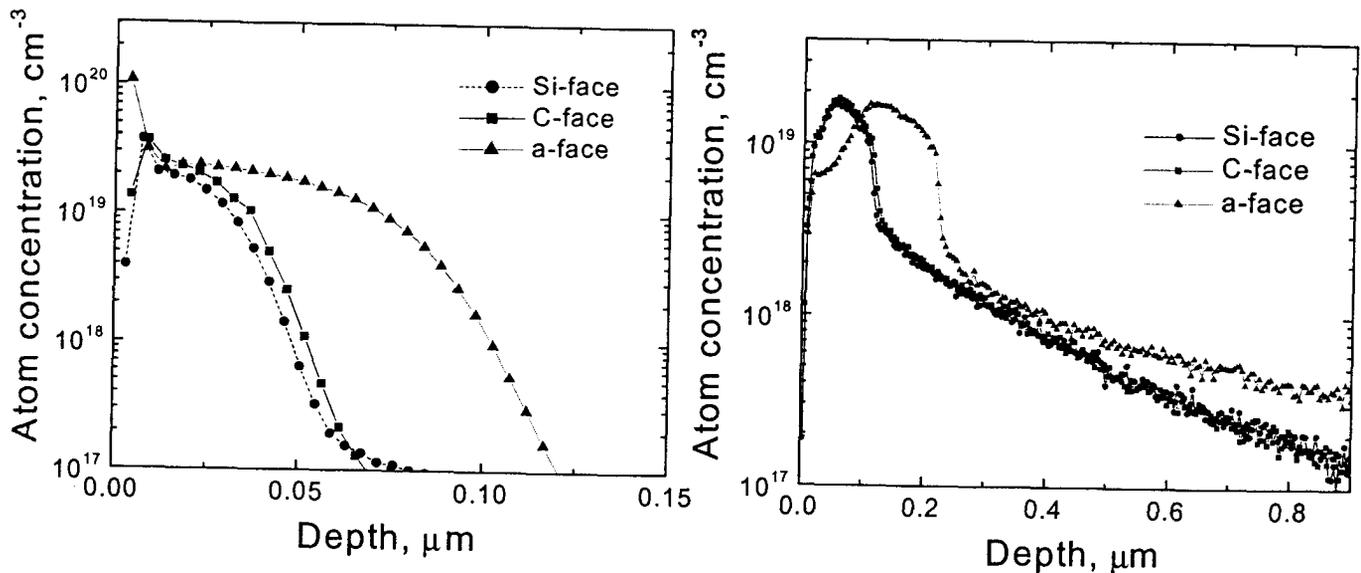


Fig.1. SIMS measurements of Al (left) and ¹¹B (right) vs. depth in 4H-SiC substrates after diffusion at 1900°C for 10 min

Laser Crystallization Mechanism of Amorphous SiC Thin Films on Glass

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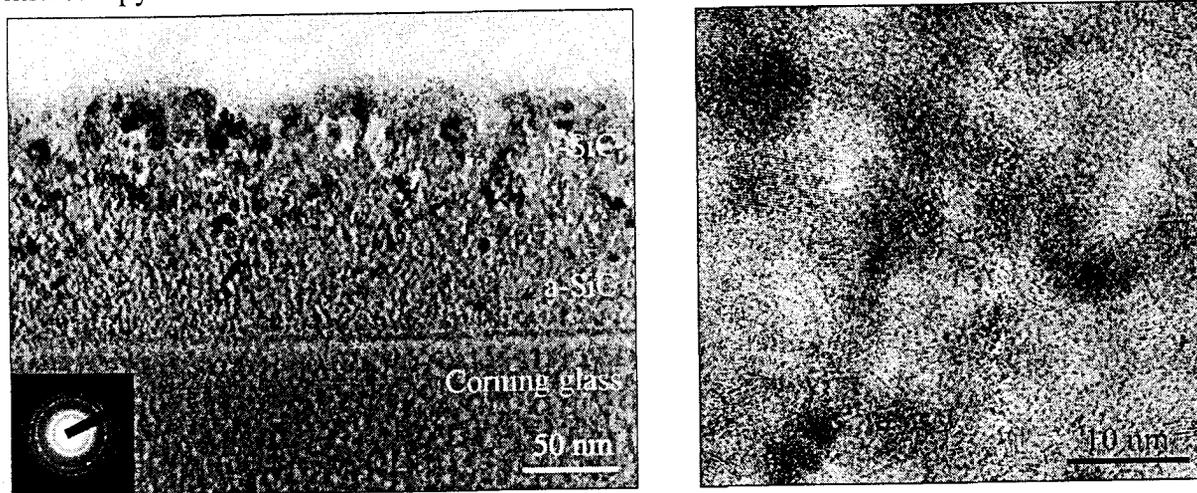
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Silicon carbide is an ideal material for high-power, high-frequency and high-temperature electronic devices. For these applications nanocrystalline, polycrystalline, or single-crystalline SiC films are required. Usually, crystalline SiC films are produced by CVD either at high substrate temperature or followed by a high temperature annealing step in which amorphous SiC is crystallized. These processing technologies have the disadvantage that large area and low cost materials such as glass cannot be used as substrates. However, high temperature annealing can be avoided by pulsed laser irradiation of amorphous material.

Amorphous, hydrogen free, SiC films with 100-400 nm thickness were produced on glass (Corning 7059) by pulsed laser deposition from a stoichiometric, polycrystalline SiC target. The ablation was carried out using a pulsed KrF excimer laser (248 nm, 25 ns) at a repetition rate of 10 pulses per second, a pulse energy of 250 mJ, a laser fluence of approximately 2 J/cm² on the target surface with about 400°C substrate temperature. The amorphous character of the deposited films was confirmed by Raman measurements and transmission electron microscopy. The Si to C atomic ratio determined by EDX and RBS analysis is close to 1:1.



a) b)
Figure 1: a) Cross sectional TEM image of laser crystallized SiC layer on a glass substrate (inset: selected area diffraction (SAED) pattern from the layer); b) corresponding high-resolution TEM image

The laser crystallization was carried out by single shots of the KrF laser in air at ambient pressure. A fluence in the range of 0.1 to 1 J/cm² was applied on a 5x2 mm² area of the amorphous film. A fluence above 250 mJ/cm² leads to crystalline SiC.

The crystalline character of the laser crystallized films above the crystallization threshold of 250 mJ/cm² was investigated by optical microscopy, Raman measurements, RBS

investigations, and transmission electron microscopy. Figure 1 shows cross sectional TEM images, Fig. 1b) a HRTEM image of a laser crystallized SiC layer. From the TEM images we conclude that the SiC crystallites have diameters of 10 to 30 nm. The corresponding selected area diffraction (SAED) pattern taken from the layer shows rings of polycrystalline material, the spacings of which fit to cubic silicon carbide. Additionally, from high resolution images a distance between atomic planes of 0.25 nm was found which corresponds to (111) planes distance (0.252 nm) in cubic SiC. Fluences well above the melting threshold lead to a segregation of the material.

The crystallization process was studied by time resolved reflection and transmission (TRRT) measurements during laser irradiation. A 10 mW cw He-Ne laser (633 nm) was used to probe the sample reflectivity and transmissivity. The He-Ne laser beam power was measured with a fast photodiode (2 ns time resolution) and registered by an oscilloscope. Since the transmissivity and reflectivity of liquid SiC is expected to differ remarkably from that of solid SiC, this method appears suitable to detect the liquid phase on the sample surface.

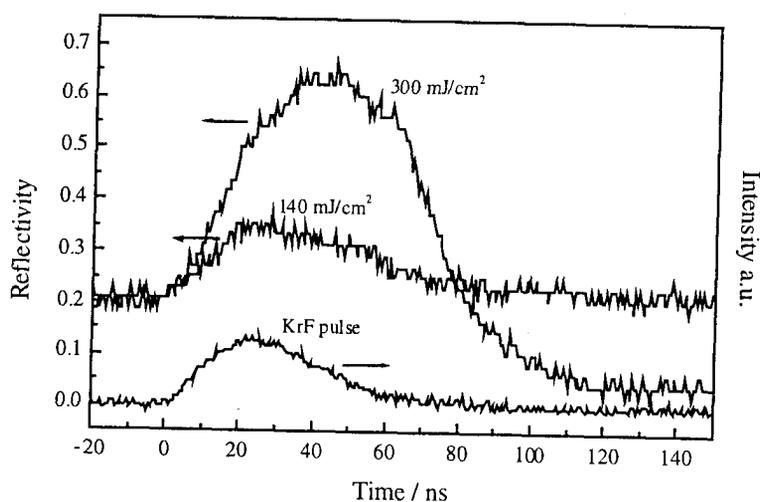


Figure 2: TRR curves and the crystallization pulse

Figure 2 shows the reflectivity results of TRR measurements during excimer laser irradiation with 140 mJ/cm^2 and 300 mJ/cm^2 . In the low fluence irradiation curve the reflectivity increases weakly which is interpreted as a film heating. After the irradiation the reflectivity recovers to the previous value, so that no permanent modification of the film was detected. For the high fluence irradiation the reflectivity increases to 0.6. The high reflectivity value remains for approximately 50 ns, which is longer than the irradiation pulse of 30 ns. After 120 ns the reflectivity reaches a permanent value lower than before corresponding to a permanent modification of the film. The laser pulse leads to a crystallization of the amorphous material. According to the TRR measurements the crystallites result from a metastable SiC melt existing for approximately 50 ns. These findings are unexpected because they are in contradiction to the equilibrium phase diagram of SiC in which no liquid phase occurs at ambient pressure.

The rather high reflectivity value of 0.6 during laser irradiation indicates a metallic character of the melt comparable to l-Si and l-Ge. To confirm the existence of a metastable SiC melt time resolved transmission and conductivity measurements are discussed.

Experimental and Computer Simulation Studies of Defects and Ion-Solid Interactions in Silicon Carbide

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The results of experimental and computer simulation studies on defects and ion-solid interactions in silicon carbide (SiC) will be presented. The interaction of energetic ions with SiC results in the creation of interstitial, vacancies, antisite defects, and defect clusters that interact to produce long-range structural disorder. Ab initio calculations and molecular dynamic (MD) simulations are used to determine defect formation energetics, defect production as a function of cascade energy, and the effects of cascade overlap. Ion-beam-induced disordering in single crystals of 6H-SiC has been investigated experimentally for wide range of ions (H^+ to Au^{2+}). The accumulation and recovery of disorder on the Si and C sublattices is determined, respectively, by Rutherford backscattering spectrometry (RBS/C) and $^{12}C(d,p)^{13}C$ nuclear reaction analysis (NRA/C) in channeling geometry.

Density functional theory has been used to study the formation and properties of native defects in 3C-SiC. It is found that the most stable configurations for interstitials are C-C and C-Si split interstitials along the $\langle 100 \rangle$ and $\langle 110 \rangle$ directions. Multi-axial channeling measurements indicate that Si and C interstitials are well aligned along the $\langle 0001 \rangle$ axis in 6H-SiC, consistent with DFT results. Along other axes, the rate of C disordering is higher than for Si disorder, which is consistent with MD simulations that show lower displacement energies for C relative to Si. The results of MD simulations for the net displacements and antisite defects produced by a Si primary knock-on atom (PKA) are shown in Fig. 1 as function of PKA energy. The number of net displacements is defined as the sum of the total number of interstitials (or vacancies) and antisite defects. The number of C Frenkel pairs is nearly 3 times the number of Si Frenkel pairs. Similar behavior is observed for C PKAs. Antisite defects are produced by nearest-neighbor replacements during the collisional phase and some random interstitial-vacancy recombination during the subsequent relaxation phase.

MD simulations have also shown that large disordered domains, including amorphous clusters, are created in the cascades produced by Au PKAs; whereas, Si PKAs generate only small interstitial clusters, with most defects being isolated single interstitials and vacancies distributed over a large region. These predictions are in agreement with the interpretation of experimental results, as shown in Fig. 2, where the relative disorder on the Si sublattice in SiC at the damage peak is shown as a function of dose in displacements per atom (dpa) for 2 MeV Au^{2+} and 550 keV Si^+ ions at low temperatures. These

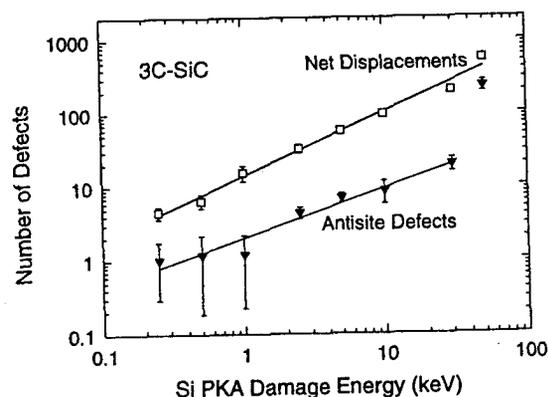


Fig. 1. Net displacements and antisite defects as a function of Si PKA energy.

results suggest that the higher disordering rate for Au^{2+} is associated with a higher probability for direct-impact amorphization or cluster formation during the cascade process.

MD simulations with 10 keV Si PKAs have been employed to simulate cascade overlap, damage accumulation and amorphization processes in 3C-SiC. A total of 140 cascades were overlapped in an MD simulation cell containing 40,000 atoms. At low dose, damage is dominated by single interstitials and small clusters consisting of interstitials and antisite defects, and their concentration increases with increasing dose. The coalescence of small and large clusters at higher dose is an important mechanism leading to amorphization in SiC, and the homogenous nucleation of small clusters at low dose is consistent with the homogenous amorphization process that is observed experimentally under similar irradiation conditions. Under these conditions, the driving force for irradiation-induced amorphization is the accumulation of both interstitials and antisite defects. The relative disorder as a function of dose shows a sigmoid behavior, as shown in Fig. 3, which is in good agreement with experimental measurements (Fig. 2). High-resolution TEM image simulations of defect accumulation processes in the MD simulation cell have been conducted to reveal the microstructural changes due to cascade overlap processes, as shown in Fig. 4, and the results are in good agreement with experimental HRTEM images.

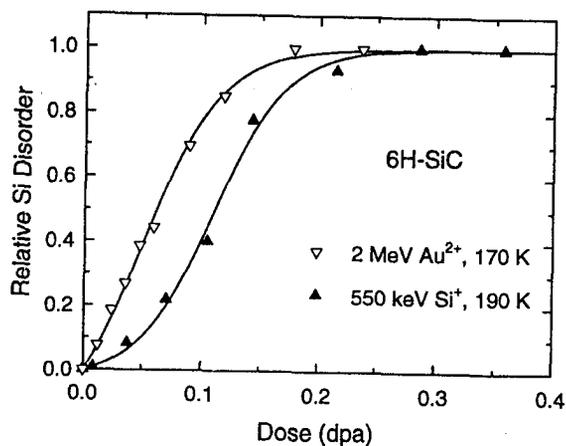


Fig. 2. Relative disorder as a function of dose in 6H-SiC irradiated by 2.0 MeV Au^{2+} at 170 K and 550 keV Si^+ at 190 K.

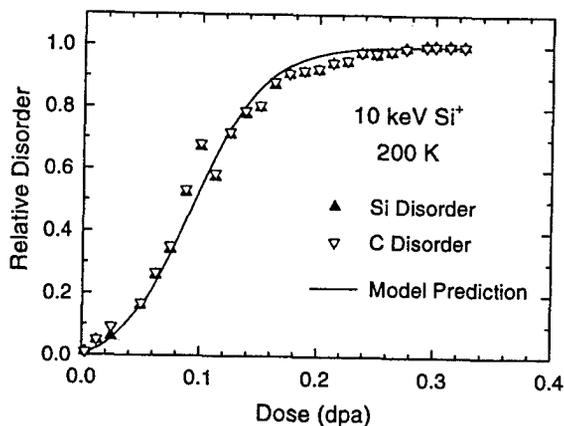


Fig. 3. Relative disorder in SiC based on MD simulations employing 140 cascades.

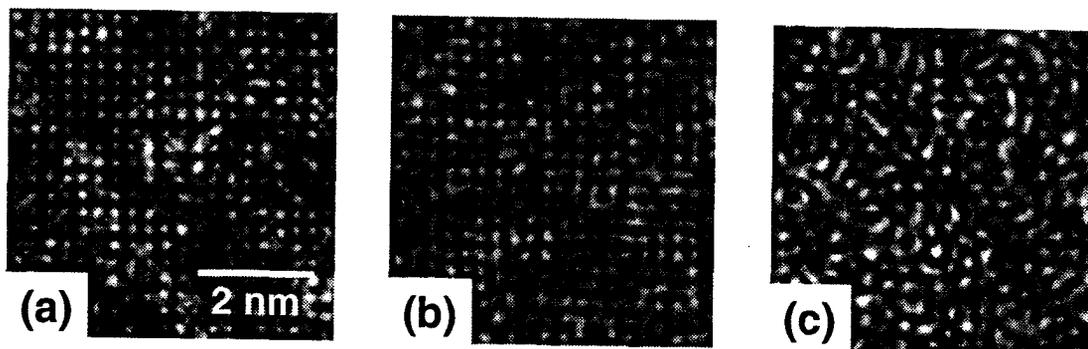


Fig. 4. HRTEM image simulations of MD damage states from accumulated cascade overlap: (a) 0.06 dpa, (b) 0.13 dpa, and (c) 0.28 dpa

ENHANCED DOPANT DIFFUSION EFFECTS IN 4H-SILICON CARBIDE

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ABSTRACT

Although doping of SiC by diffusion techniques is impractical (due to prohibitively slow diffusion rates of most common dopants), diffusion of implanted dopants at high anneal temperatures is more significant than is often considered to be the case. In simple single species implants, substantial implant profile broadening and implant tail lengthening have been observed - the latter linked to Transient Enhanced Diffusion (TED) - during high temperature annealing. Such effects are enhanced by the relatively high concentrations of lattice defects that occur in implanted SiC (due to the crystal lattice structure), and the high implant doses required (due to low activation levels). However although most realistic device structures contain more than one single implant species (e.g. complex n-p-n structures of bipolar devices), there is little published work on the effects of implant damage and dopant diffusion in such complex structures. In this paper, we present an experimental study of enhanced dopant diffusion in nitrogen/boron implanted n-p-n structures and propose a simple model which can be used to predict the extent of dopant diffusion (or migration) observed in such cases.

In order to investigate these effects, a detailed experimental study of nitrogen/boron interaction effects was performed. An implantation matrix of nested (one within the other) implants with varying nitrogen and boron implant profiles was fabricated and annealed over a range of temperatures between 1300C and 1700C. One resultant set of SIMS data obtained for implanted nitrogen into an implanted boron p-well region as a function of the anneal time at 1600C is shown in Figure 1. The boron implant fabrication schedule used was:- 20keV $1 \times 10^{13} \text{cm}^{-2}$, 50keV $2 \times 10^{13} \text{cm}^{-2}$, 100keV $3 \times 10^{13} \text{cm}^{-2}$, 160keV $3 \times 10^{13} \text{cm}^{-2}$. The wafers were then cleaned and re-patterned for nitrogen implant at the following energies and doses:- 20keV $8 \times 10^{14} \text{cm}^{-2}$, 40keV $8 \times 10^{14} \text{cm}^{-2}$ and 60keV $2 \times 10^{15} \text{cm}^{-2}$. All implants were performed at room temperature. Under these conditions, boron and nitrogen diffusion in excess of that seen in equivalent single species implantation was observed. Figure 2 highlights the unexpectedly strong nitrogen diffusion found in the SIMS data of Figure 1, previously presumed to be due to the effect of implant damage from the earlier boron implant. Although quantifying the degree of nitrogen diffusion post-experiment is straightforward (by using a modified 'effective diffusion constant'), predicting the extent of such enhanced diffusion prior to device processing is difficult as it depends on the exact nature of the whole implant and anneal sequence. Complex calculations which model the interaction of the substrate crystal lattice with the incoming ion species and the effect of subsequent annealing can be performed by molecular dynamics techniques but are computationally expensive and impractical for all

but a limited number of special cases. There is thus a need for simple tractable models which enable predictive calculation of these enhanced diffusion (redistribution or migration) effects of both n- and p-type dopants in SiC in complex multi-species implant structures.

In this paper a simple and elegant physical model for these enhanced diffusion phenomena as observed in Silicon Carbide is proposed. The model allows possible mechanisms for dopant movement (or migration) within Silicon Carbide to be examined - based on the initial state of an ion implanted substrate. It will be shown that an accurate prediction of complex implanted multi-species profiles can be obtained by simple models detailing the interaction between ion species as a function of temperature. The proposed model accurately predicts the resultant implanted ion redistribution profiles following high temperature annealing. Additionally, isolated box implant profiles follow an expected modification profile consistent with implant depletion widths. Previously published findings and the extensive new experimental data presented here correlate and agree well with the predictions of our new model. Additionally, our new model predicts the temperature behavior of a wide range of published experimental results and also accounts for the time dependant behavior of the ion redistribution during the annealing process. To date, no other TED model or analytical process as published in the literature explains the high temperature annealed ion redistribution in SiC as well as the model proposed in this paper.

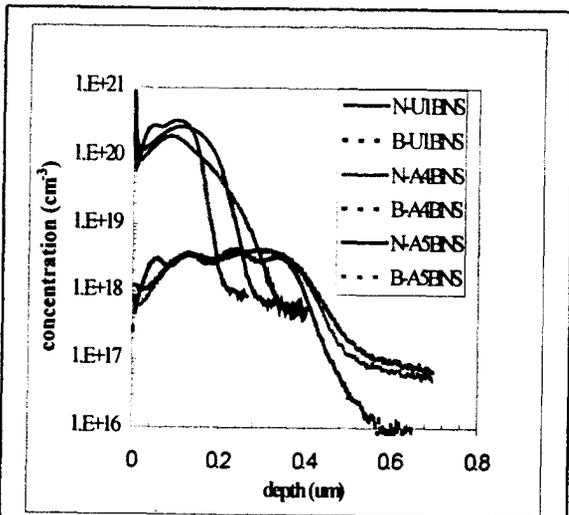


Figure 1: SIMS data showing nitrogen and boron profiles after anneal at 1600C for 10mins (sample A4BNS) and 20 mins (sample A5BNS) respectively. For comparison an unannealed sample (U1BNS) is also shown.

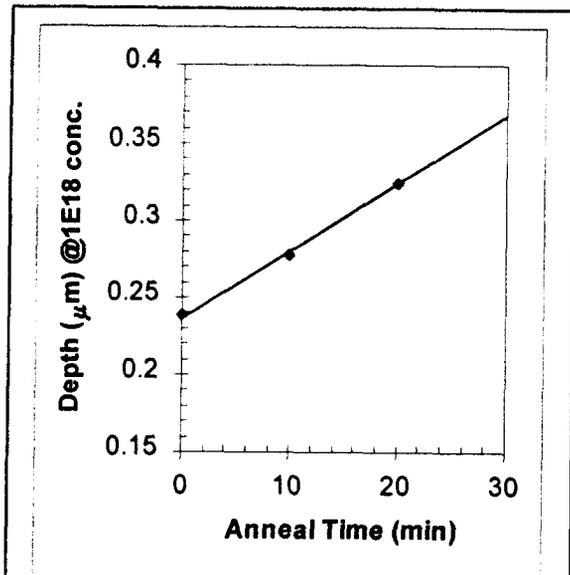


Figure 2: Nitrogen implant depth vs anneal time at 1600C (note: line is guide to the eye only)

Ion implantation – tool for fabrication of advanced 4H-SiC devices.

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SiC is one of the most promising semiconductors for manufacturing electronic devices with stable operation in extreme environments. One major for device fabrication is the high resistivity of the p-material since the acceptor concentration is limited by the solubility in SiC. Nonequilibrium method - of ion implantation doping (ID) of SiC allows to introduce acceptors with concentrations exceeding their solubility limit in SiC. However, the task of the acceptor activation is not yet solved causing the formation of high resistive p-layers [1,2]. It has been shown that ID of SiC with Al followed by high temperature annealing allowed to produce p⁺n junctions where ID p⁺-layers did not introduce additional resistance in the device structures [3]. Recently, beneficial influence of short thermal annealing on structural perfection of Al ID 4H-SiC epitaxial layers grown by chemical vapor deposition (CVD) was revealed, for instance by a rise of the hole diffusion length values [4]. In this work the advantages of high dose Al ID in 4H-SiC CVD epitaxial layers followed by short high temperature annealing for high voltage diodes as well as in the detectors of UV radiation and α -particles were investigated.

4H-SiC CVD epitaxial layers with thickness 25 μm and the concentration $N_d - N_a = 4 \times 10^{15} \text{ cm}^{-3}$ were grown on commercial 4H-SiC wafers. Al ions with energy 150 keV and dose $5 \times 10^{16} \text{ cm}^{-2}$ were implanted in CVD layers followed by short thermal annealing for 15 s at 1700 °C in Ar ambient. Regular Cr ohmic contacts to n- as well Al regular and semitransparent contacts to p⁺- SiC were produced by thermal vacuum evaporation. P⁺n mesa structures with different areas were formed by reactive ion plasma etching.

The structural perfection in lateral and axial directions of the CVD layers before and after Al ID p⁺n junction formations were investigated by scanning electron microscopy (SEM) using electron beam induced current (EBIC) imaging, by secondary ion mass spectrometry (SIMS) and SIMS imaging in Al ions, by x-ray photoelectron spectroscopy (XPS) and real color cathodoluminescence (CCL) mode in SEM. Diffusion lengths of the holes (L_p) were determined by SEM using standard treatment of EBIC signals. Electrical properties of the CVD layers and devices were revealed from capacitance-voltage as well as from forward and reverse current-voltage characteristics measured under different conditions. The produced structures were irradiated with 4.5-5.5 MeV α -particles and the pre-amplified signal was registered at 20 °C. The spectral photosensitivity characteristics of Al ID 4H-SiC p⁺nn⁺ structures were studied in the range of incident energies 2.8–6 eV under short-circuit condition for the photocurrent.

4H-SiC p⁺nn⁺ diodes with p⁺n junction position of 0.6 μm and the area of $1 \times 10^{-3} \text{ cm}^2$ exhibited forward current density of $3 \times 10^3 \text{ A cm}^{-2}$ at 12 V voltage drop and differential resistance of $3 \times 10^{-3} \Omega \text{ cm}^{-2}$. The small differential resistance value was stimulated by a low resistivity of Al ID p⁺-layers and ohmic contacts as well as partial modulation of the n-base region by injected holes due to the increase in L_p value. This effect is probably due to the

improvement of the structural quality CVD epitaxial layers after Al ID p^+n junction formation causing the absence of recombination centers of holes in Al AD p^+ layers and in CVD layers close to p^+n junction position [5]. Breakdown voltage of 1.7 kV limited by CVD structural imperfection were reached for these diodes, that had stable operation up to 500 °C.

Shallow Al ID p^+n junction position and small leakage currents, less than 10^{-8} A, were advantageous for the work of α -particle detectors. It has been revealed that these detectors exhibited the extremely low background levels due to the absence of the "dead window" like Schottky barriers. The amplitude permission values were 10% determined in spectrometric regimes.

Also UV photodetectors based on Al ID 4H-SiC p^+n junctions combine the advantages of photosensitive Schottky barrier structures and structures grown by epitaxy. The collection efficiency of nonequilibrium charge carriers nearly 100% was observed for this detectors [6]. The spectral sensitivity range of the photodiodes corresponded to 2.8-6 eV, peaking at 4.9 eV. This range is near to the spectrum of relative effectiveness of various wavelengths in bactericidal UV radiation, which indicates novel application areas for a SiC detector.

Thus, it has been shown that Al high dose implantation with short high temperature thermal annealing ensured the creation of narrow low resistive p^+ layers which can be used as effective hole injected regions in SiC devices. Improvement of SiC structural quality near Al ID p^+n junctions increased the L_p value that provided partial modulation of the n-base that reduced the resistance in device structures.

Influence of the Al ID with subsequent annealing on the quality of 4H-SiC CVD epitaxial layers will be discussed. Electrical and optical characteristics of high voltage diodes, spectral data and quantum efficiency of the photodetectors in temperature range 78-360 K. the collection efficiencies and counting characteristics of detectors of α -particles based on Al ID 4H-SiC p^+n junctions will be presented.

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A comparative study of high temperature Aluminum post-implantation annealing in 6H and 4H-SiC, non-uniformity temperature effects

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Ion implantation, an indispensable technique to locally dope silicon carbide (SiC) still presents many problems in particular for p-type zone creation. High ionization energy of dopants imposes to raise the implanted dose above the amorphisation threshold for room temperature implantations. Structure recrystallization and electrical activation of dopants, i.e. their incorporation in active SiC atomic sites, require high temperature annealing, about 1700°C in special configuration, with an overpressure of silicon and carbide.

Aluminum (Al) implantations were carried out at room temperature on the whole surface (5x5mm²) of n-type 6H and 4H-SiC epilayers (doping level ~10¹⁶ cm⁻³), cut out from CREE commercial wafers. A total dose of 1.75x10¹⁵ cm⁻² was implanted in disoriented samples to avoid channeling effects in SiC crystal axes. Post-implantation anneals were realized in a dedicated SiC induction heating furnace [1] at the center of the susceptor. High heating ramp was utilized, 40°C/s, before to reach a constant temperature plateau in the 1600-1800°C interval during 5 min to 1 hour.

Rutherford Backscattering Spectrometry in the Channeling mode (RBS/C) measurements realized after ion implantation and before annealing illustrate spectral superposition for the 6H and 4H-SiC samples (Fig. 1). A 0,31µm amorphous layer up to the surface is found, the implant dose being superior to the threshold of an amorphous layer formation [2]. To convert energy to depth in RBS/C spectra a constant density value (3,21 g/cm⁻³) was taken. The amorphous layer is found larger if we consider that the density of amorphous SiC is lower than of crystalline SiC. After annealing a better recrystallization is observed for 6H-SiC samples. After 1700°C annealing during 30 min the backscattering yield is 5,8% for the 6H-SiC sample and 6.3% for 4H-SiC sample, that proves nevertheless good crystallinity after annealing in the both cases.

As verified by Secondary Ion Mass Spectroscopy (SIMS) analyses on as-implanted and annealed samples, no dopant loosing occurs after high temperature annealing. The roughness of the sample surfaces after annealing increases with the temperature and the annealing time, this process becomes excessive for temperatures and times superior to 1700°C and 30 min.

Electrical activation of dopants on implanted and annealed samples was investigated by sheet resistance (R_{sh}) measurements with a four point probe technique. R_{sh} decreases when the annealing temperature or the annealing time increases. In Fig. 2 R_{sh} variations with the annealing temperature are represented, for a 30 min annealing time.

The linearity of the R_{sh} variations proves a non saturation of electrical dopant activation, nevertheless regression lines intersect temperature axe at 1819°C and 1801°C for the 6H-SiC and 4H-SiC respectively, which illustrates that these annealing conditions lead to nearly complete Al dopant activation.

For a deepen approach of the electrical behavior of Al-implanted layers, Van der Pauw (VdP) geometries and Transmission Line Method (TLM) structures were realized on SiC wafers (1.375" diameter) by a photolithographic process. Bipolar diodes were also created to study the rectifying properties of the p⁺-n junction realized by Al implantation. The same ion implantation parameters were utilized, and a 1700°C during 30 min thermal annealing was carried out on these wafers.

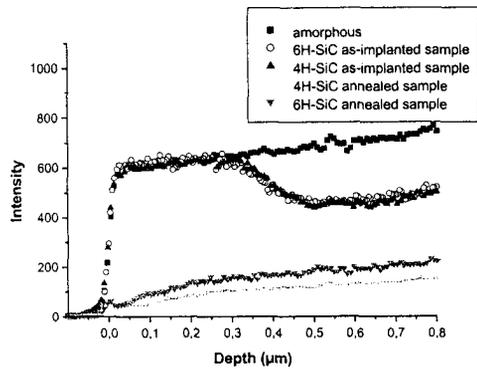


Fig. 1. RBS/C spectra on Al as-implanted and annealed 6H and 4H-SiC samples.

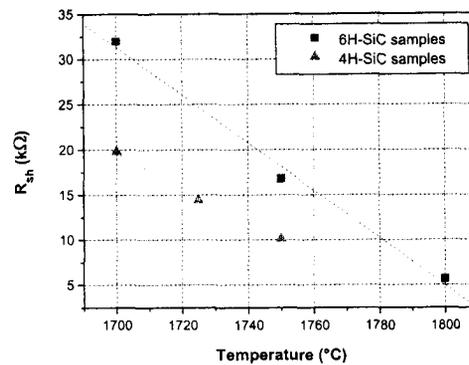


Fig. 2. Sheet resistance variations with annealing temperature for 30min annealing duration.

Sheet resistance measurements made on VdP and TLM structures of 4H-SiC samples (Fig.3) show a linear dependence with the distance between the respective structure and the center of the wafer. Sheet resistance found by TLM measurements must be corrected by a geometrical factor. A linear variation is determined also for the carrier concentration by Hall effect measurements at room temperature, the mobility values preserving a relatively constant value ($18 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$). High values of hall concentration involve a good electrical Al dopant activation.

A good agreement is found between the sheet resistance measured on the VdP structure placed at the wafer center and the values obtained by four point probe technique on $5 \times 5 \text{ mm}^2$ whole surface implanted samples, annealed in the susceptor center ($19,5 \text{ k}\Omega$ Fig. 2 and 3). The linear variations of R_{sh} on VdP wafer structures compared with the results presented in Fig. 2 involve an almost linear temperature variation at the surface of the susceptor, due to the induction heating system, the temperature of the susceptor increases from the center to its periphery. A difference of 31°C is found between the center and the wafer periphery. This is in agreement with thermodynamic simulations of the susceptor induction heating process.

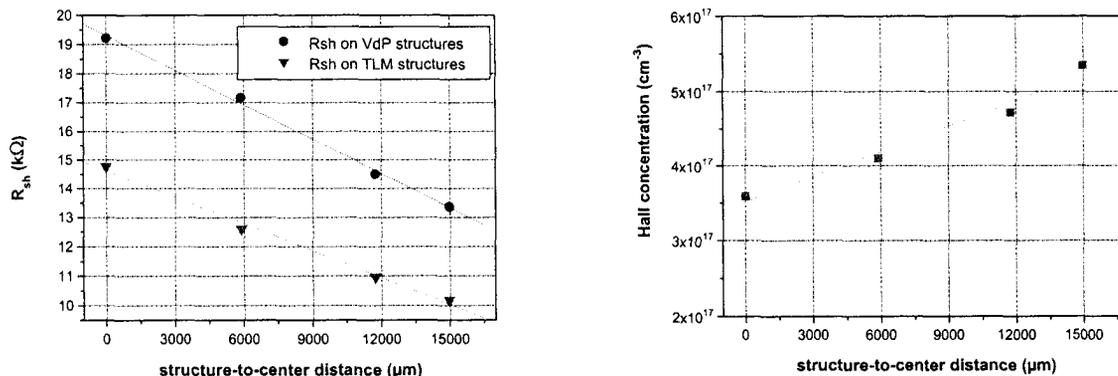


Fig3. Sheet resistance and hall concentration variation on a 4H-SiC wafer annealed at 1700°C during 30min.

I-V measurements on bipolar diodes show a good behavior in forward and reverse polarization. Current density of 60 A cm^{-2} is found at a forward bias of 5 V and $10^{-7} \text{ A cm}^{-2}$ under 100 V reverse bias.

All these results will be detailed in the final paper and more comparisons between 6H and 4H-SiC will be developed.

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Improvements of electrical properties for n-type-implanted 4H-SiC substrates using high-temperature rapid thermal annealing process

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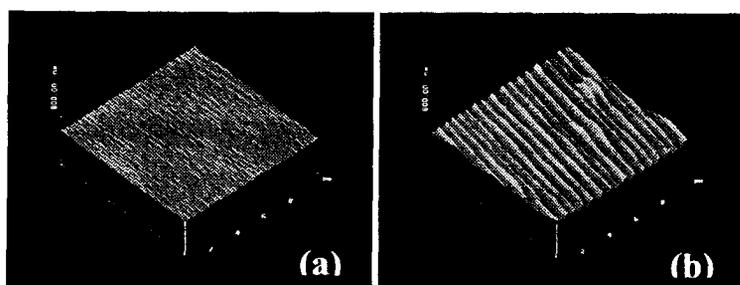
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Post implantation annealing is indispensable process for electrical activation of dopants implanted into SiC. To obtain the higher electrical activation of dopants, the post implantation annealing is generally carried out at higher temperature above 1500°C using conventional furnace annealing or a chemical vapor deposition reactor. However, selective preferential evaporation of Si atoms from the SiC surface during annealing causes local formations of C-rich phases and serious surface morphology roughening as the SiC substrates are placed on a heating holder or in a crucible for a long time. It is predicted that these degrade the performances of device fabricated on rough surface. We considered that short time annealing at high temperature is the most suitable method for the suppression of the surface morphology roughening as well as the high electrical activation of dopants. In this study, the post implantation annealing process using high-temperature rapid thermal annealing (HT-RTA) has been investigated to reduce the surface morphology roughening and to realize higher electrical activation of n-type dopants in 4H-SiC.

4H-SiC(0001) substrates with an 8°-off-angle and p-type epitaxial layer purchased from Cree Research Inc. were used. The effective carrier density ($N_A - N_D$) in the epitaxial layer was $5 \times 10^{15} \text{ cm}^{-3}$. Multiple ion implantations at 500°C were carried out through the oxide film in order to form a box-shaped profile with a thickness of 0.3 μm . The multi-energy ion implantations were performed in six steps (40 ~ 250 keV) for phosphorus (P) and nine steps (40 ~ 400 keV) for arsenic (As). The total implanted doses of 7×10^{15} and $2 \times 10^{16} \text{ cm}^{-2}$ were used. The post implantation annealing at 1700°C was conducted using the HT-RTA with the maximum raising rate of 1700°C/min in Ar atmosphere. The post annealing time (t_a) was varied between 0.5 and 30 min. To perform the measurements of sheet resistance (R_s) and Hall effect, Ni electrodes with a van der Pauw configuration were formed by electron beam evaporation and were annealed at 1000°C for 5 min. The surface morphologies of the implanted layers were observed using atomic force microscopy (AFM).

The AFM images of the surface morphology observed from P-implanted 4H-SiC (SiC:P) annealed at 1700°C for 1 min and for 30 min are shown in Figs. 1 (a) and (b), respectively. These images clearly show that the size and height of the groove structures on the SiC:P surface annealed for 1 min are less than those for 30 min. Average roughness (R_a) calculated from the AFM images of a $10 \times 10 \mu\text{m}^2$ observation area are 2.4 nm for 1 min and 13.3 nm for 30 min, respectively. Figure 2 shows the dependences of R_s , measured from SiC:P and As-implanted 4H-SiC (SiC:As), on t_a . The results show that HT-RTA reduces the R_s for both SiC:P and SiC:As. The R_s of 62 Ω/sq . for SiC:P annealed for 1 min and 160 Ω/sq . for SiC:As annealed for 2 min are obtained. According to Hall effect measurements at room temperature, an electrical activation ratio higher than 80 % is indicated in the SiC:P annealed at 1700°C for 1min. Finally, the minimum R_s of 38 Ω/sq . is achieved in SiC:P implanted with a dose of $2 \times 10^{16} \text{ cm}^{-2}$ and subsequently annealed at 1700 °C for 30 s. This R_s value is very small as a resistance of an n-type source region for SiC power devices. Consequently, it is demonstrated that the HT-RTA process is very useful for preventing the surface morphology roughening and lowering the R_s .

This work was performed under the management of FED as a part of the METI NSS program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.



Figs. 1. AFM images of surface morphology observed from P-implanted 4H-SiC annealed at 1700°C for (a) 1 min and (b) 30 min. z-axis length of image corresponds to 300 nm/div.

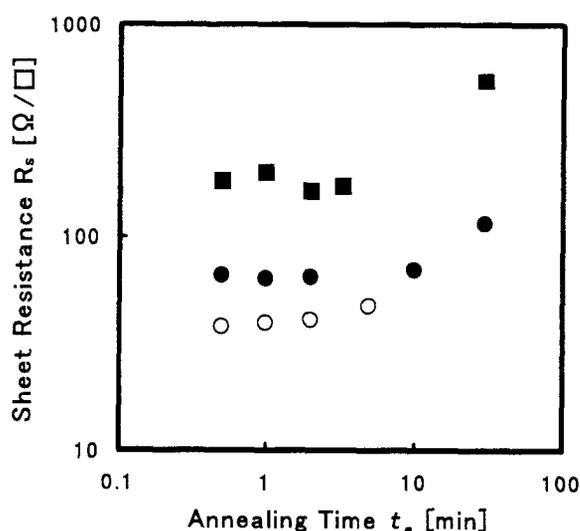


Fig. 2. Dependences of the sheet resistance R_s of P- and As-implanted 4H-SiC on the post implantation annealing time t_a . The closed circles and squares represent the R_s for P- and As-implanted 4H-SiC with a dose of $7 \times 10^{15} \text{ cm}^{-2}$, respectively. The open circles represent the R_s for P-implanted 4H-SiC with a dose of $2 \times 10^{16} \text{ cm}^{-2}$.

Masking process for high-energy and high-temperature ion implantation

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The ion implantation is promising process for manufacturing the silicon carbide (SiC) devices. As its particular nature, the high-energy and the high-temperature ion implantation is required. Especially, in the SIT(Static Induction Transistor)⁽¹⁾ as shown in figure 1, the width between p-gate and p-gate has an important role in the electric characteristics. It is important to establish the ion implantation to be able to form the deep p-layer selectively. However, the polymer photoresist which is commonly used in the silicon (Si) device manufacturing cannot be used for the SiC devices because of the high-temperature ion implantation. Then, we developed the silicon-dioxide (SiO₂) mask using the photolithography and the dry-etching processes. We obtained the mask of the line width of 1.2 μm and the thickness of 3.2 μm.

Figure 2 shows the aluminum ion distribution computed by the TRIM program. The energy of the ion is MeV. The aluminum ions are penetrated into the SiC substrate on the case of the SiO₂ thickness of 2.0 μm. On the case of SiO₂ thickness of 2.6 μm the aluminum ions are fully cut. We set the SiO₂ thickness of 3.2 μm, which is estimated to calculate 20% margins.

We used the chip of the size of 15mm x 15mm. The lithography and the dry-etching were performed using the chip fixed on a 5-inch Si wafer. The SiO₂ of the thickness of 3.2 μm was deposited by the low-pressure chemical vapor deposition (LPCVD). Figure 3 shows the cross-sectional scanning electron microscopy (SEM) photograph of the SiO₂ which was dry-etched using the photoresist of the thickness of 4.2 μm. The CHF₃ and the CF₄ gases are used on the dry-etching. The photoresist was completely lost and the SiO₂ was also etched. Then we performed the ultraviolet (UV) irradiation on the polymer photoresist. Figure 4 shows the cross-sectional SEM photograph of the SiO₂ which was dry-etched using the UV irradiated photoresist of the thickness of 2.5 μm. The photoresist was remained the thickness

of $1.2 \mu\text{m}$ and the SiO_2 was almost vertically etched. Particularly, the side of the SiO_2 has no notches, and the dispersion of the electric characteristics keeps controllable.

We developed the SiO_2 mask of the width of $1.2 \mu\text{m}$ and the thickness of $3.2 \mu\text{m}$ which was wholly cut the aluminum ions implanted by the energy of the MeV.

This work was performed under the management of FED as a part of the MITI NSS Program (R & D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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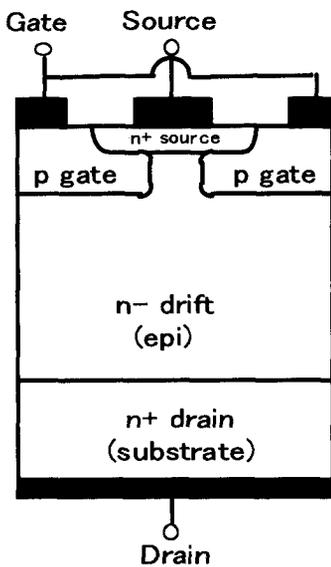


Fig.1 The device structure of SIT

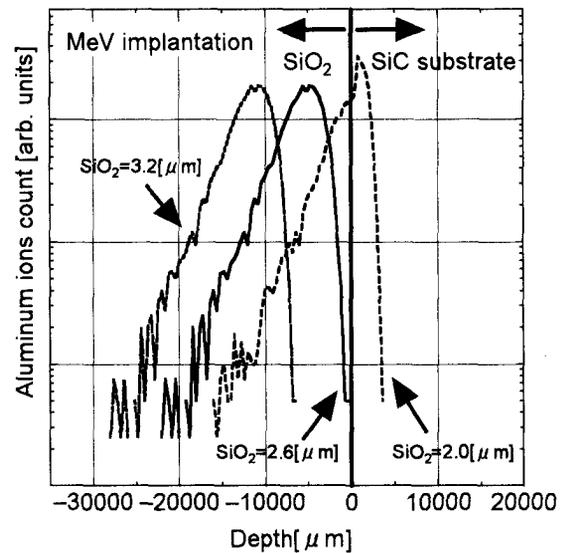


Fig.2 The aluminum ion distribution Depended on the SiO_2 thickness

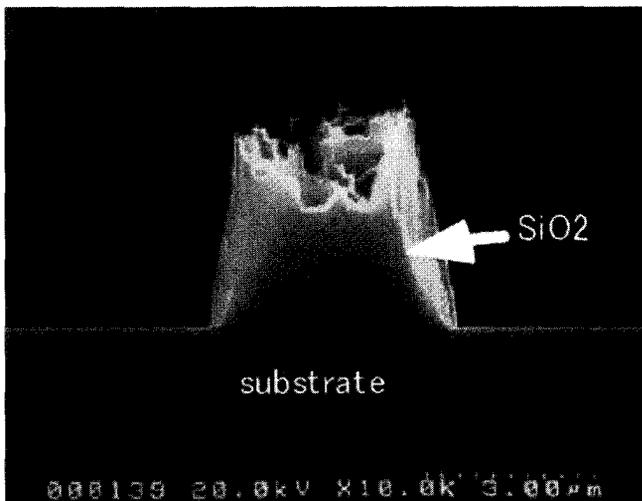


Fig.3 Cross sectional SEM photograph of the SiO_2 dry-etched using $4.2 \mu\text{m}$ photoresist without the UV irradiation

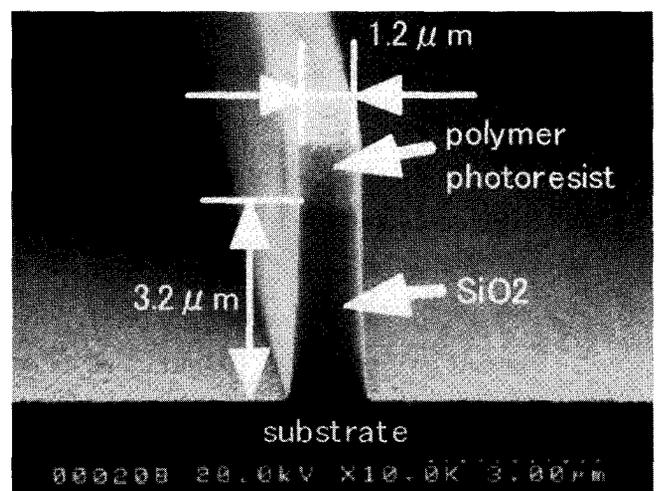


Fig.4 Cross sectional SEM photograph of the SiO_2 dry-etched using $2.5 \mu\text{m}$ photoresist with the UV irradiation

Electrical characteristics of Al⁺ ion-implanted 4H-SiC

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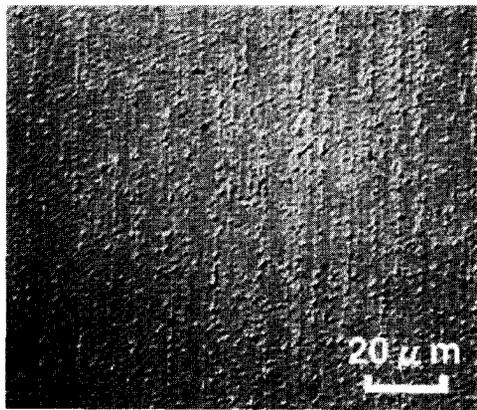
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4H-SiC is the most promising SiC polytype for manufacturing high-power, high-temperature and high-speed electronic devices with outstanding capabilities. Many efforts to obtain a good p-type SiC layer by ion implantation, using either aluminum or boron ions, have encountered difficulties such as high sheet resistance and low activation efficiency [1], [2]. In this work, an attempt was made to perform low-resistivity p-type doping in a 4H-SiC epilayer by using aluminum ion-implantation.

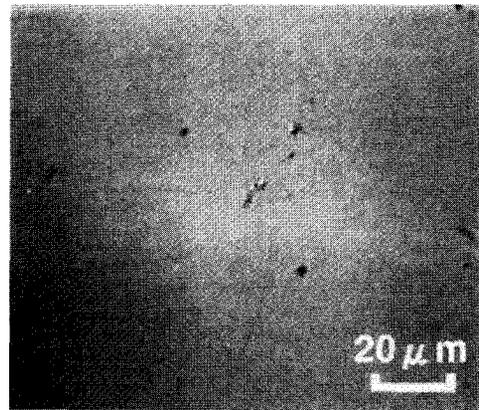
The target material, purchased from Cree Inc., was a 4H-SiC substrate with a 4- μ m-thick epitaxial layer. The doping of the epitaxial layer was 1×10^{16} cm⁻³ n-type. Specific energy/dose schedules for aluminum implantation were 180 keV/ 2.7×10^{15} cm⁻², 100 keV/ 1.4×10^{15} cm⁻² and 50 keV/ 9.0×10^{14} cm⁻². All implantations were performed at 800°C. Post-implantation annealing was done for 10 minutes at 1600~1800°C in an argon atmosphere. In order to prevent morphological surface degradation, samples were encapsulated in a dummy-SiC wafer during annealing. Nomarski differential interference contrast (NDIC) micrographs of the samples annealed with and without the dummy-SiC wafer are shown in Fig. 1. Significant surface degradation is observed for the sample annealed without the dummy-SiC wafer. On the other hand, the sample annealed with the dummy-SiC wafer shows a smooth surface morphology. To investigate the electrical properties of the samples annealed with the dummy-SiC wafer, Hall measurements were performed with the conventional Van der Pauw method. Ohmic contacts were fabricated of Ti/Al, followed by annealing at 1000°C. Sheet resistance R_s is shown as a function of the annealing temperature in Fig. 2. The value of R_s decreases with increasing annealing temperature between 1600~1800°C. R_s as low as 2.3k Ω / \square , a record low for any implanted p-type SiC layers, was obtained in the sample annealed at 1800°C. Sheet carrier concentration N_s and Hall mobility μ are shown in Fig. 3. N_s is about two orders of magnitude larger when the annealing temperature is increased from 1600°C to 1800°C. The decline in sheet resistance R_s is mainly due to the improvement of N_s with a higher annealing temperature.

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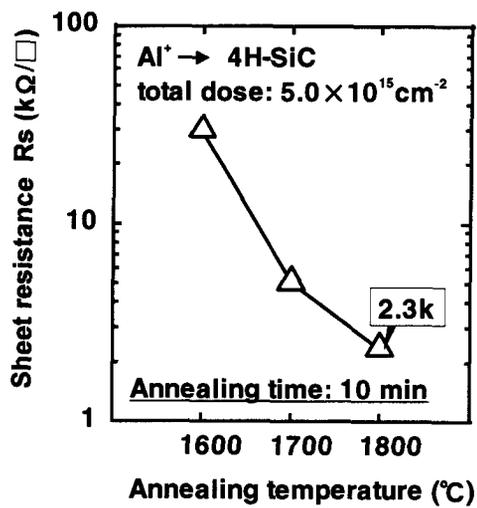
(A)



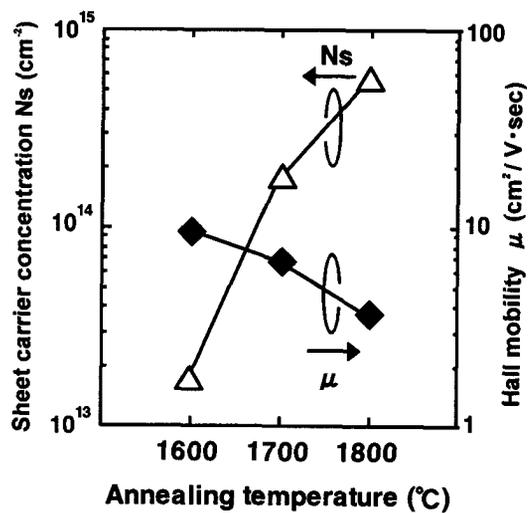
(B)

Fig. 1

Nomarski differential interference contrast (NDIC) micrographs of samples annealed (A) with and (B) without a dummy-SiC wafer.

Fig. 2

Sheet resistance R_s as a function of annealing temperature.

Fig. 3

Sheet carrier concentration N_s and Hall mobility μ as a function of annealing temperature.

Micro-structural and electrical properties of Al implanted & lamp annealed 4H-SiC

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The ion-implantation process has been a great success and being used extensively in Si-device technology, however, for SiC devices, it still lacks the critical know how related to the defect kinetics. One of the key issue for realizing the SiC planar devices is to eliminate the ion-implantation process induced damages as well as to achieve the high electrical activation for dopants to match the design requirements. However, the high temperature activation annealing process of SiC usually deteriorates the important chemical and morphological surface that eventually leads to poor electrical properties.

The micro-structural and electrical properties of Al implanted 4H-SiC annealed using a halogen lamp furnace has been investigated with the aim to minimize the effect of high temperature activation processing viz., step bunching and surface graphitisation. Earlier, Panknin et al.[1] reported high electrical activation for the Xenon array flash annealed Al implanted 6H-SiC, however, defect kinetics of the flash annealed samples were not discussed. A twin halogen lamp annealing system was used to electrically activate the implanted Al dopant. Al implantation dose was $1.0 \times 10^{15} \text{ cm}^{-2}$ and implantation was performed at 1000°C . The samples were subjected to lamp exposure from either or both sides to anneal at different temperatures. Transmission electron microscopy (TEM) was used to probe the micro-structural changes of lamp annealed 4H-SiC samples. During the activation annealing the micro-structural defects are formed and the generation of such defects upon annealing are investigated with respect to dopant electrical activation and leakage current to establish a possible correlation between the said properties. The electrical activation result suggests that the halogen lamp annealing process is as effective as conventional furnace annealing process and almost independent of time scale of performed experiments at high temperature region ($\sim 1800^\circ\text{C}$) for Al dopant. Also, contrary to the strong B transient enhanced diffusion in SiC, no significant diffusion of Al was observed [2]. The uncapped 4H-SiC samples show the improvement in the surface morphology after the high temperature lamp annealing process. However, the sublimation of the surface layer due to high surface temperature during the long direct lamp exposures was observed. TEM analysis confirms the suppression of surface graphitisation, which is commonly observed for conventional furnace annealing process. The observed circular dislocation loops, composed of either clustered interstitial atoms/dopant Al residing on basal planes and/or an extra SiC plane show a strong dependence on the annealing time. The electron energy loss spectroscopy (EELS) was used to investigate the micro-structure of dislocation loops. Basically, the implantation at elevated temperature of 1000°C leads to the substantial amount of defect reduction. During the high temperature activation annealing process, density of these dislocation loops decreases with time, although they grow in size. The test structure of pn junction with no passivation and edge termination shows the low level of leakage currents ($< 1 \times 10^{-8} \text{ A/cm}^2$). Any correlation between the dislocation loop density or size on the pn leakage current was not observed.

In summary, lamp annealing process is effective for the dopant activation process compare to the conventional furnace process as significant improvements in the sheet resistance and the pn leakage current were observed for the lamp annealed 4H-SiC samples. However, a relatively high density of dislocation loops were observed for the lamp annealed ones. The possible formation kinetics of these micro-structural defects will be discussed.

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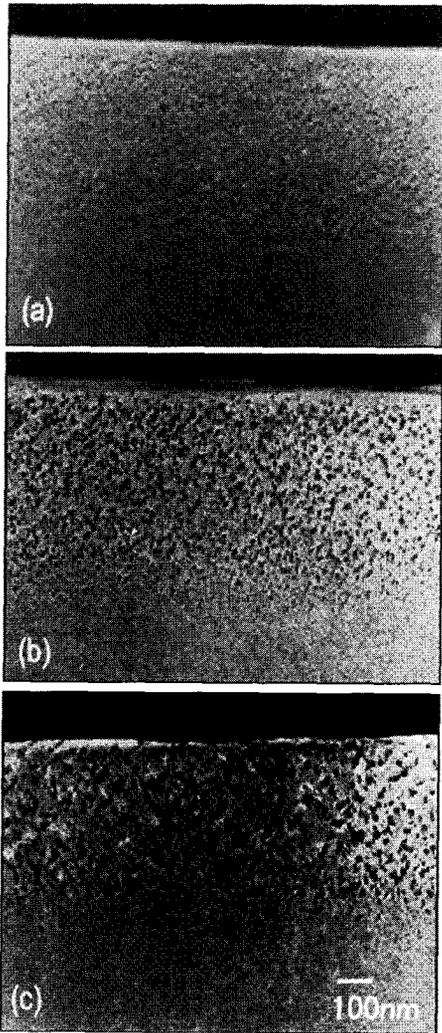


Fig.1 Cross-sectional transmission electron microscopy images of Al implanted 4H-SiC annealed using the halogen lamp furnace at (a) Temp.=1600°C for 30 sec., (b) Temp.=1600°C for 1min., and (c) Temp.=1600°C for 10min. The Al implantation dose was $1.0 \times 10^{15} \text{cm}^{-2}$ and implantation was performed at 1000°C.

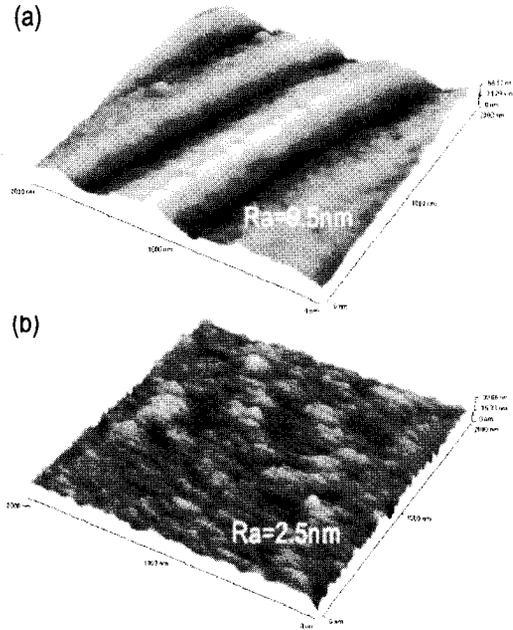


Fig. 2 AFM images of Al implanted 4H-SiC annealed using (a) the conventional furnace at Temp.=1600°C for 30min., and (b) the halogen lamp furnace at Temp.=1600°C for 30sec.

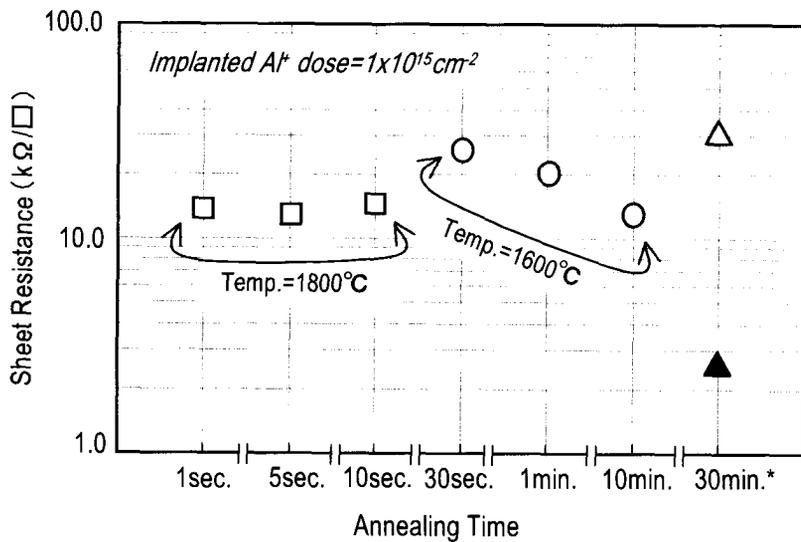


Fig. 3 Sheet resistance of Al implanted 4H-SiC as a function of activation annealing time[#] for different temperatures. The open and solid triangle data points represent the 1600°C furnace annealed samples with Al dose of $1 \times 10^{15} \text{cm}^{-2}$ and $1 \times 10^{16} \text{cm}^{-2}$, respectively. (*Furnace annealed 4H-SiC sample; [#]Excluding the ramp-up/ramp-down time)

Range distributions of implanted ions in silicon carbide

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In modern semiconductor technology the access to precise process simulators has become vital to decrease the development time and cost for new devices. To predict ion implanted doping profiles two types of simulators are mainly used: (i) Simulators based on physical models of the ion stopping processes. Most of these use different types of Monte-Carlo algorithms and can be – with appropriate empirical fine tuning – very accurate, although too time consuming for the purpose of implantation profile design.[1] (ii) A convenient alternative is based on the fact that most ion range profiles can be represented, to a high degree of accuracy, by its first four distribution moments (R_p , ΔR_p , γ , and β) using Pearson frequency distribution functions.[2] In this way, depth profiles of multiple ion implantations can be quickly and precisely simulated by interpolation between established distribution moments, providing that the amount of experimental data is large enough.

In this contribution we have assembled range data from 120 single energy implantations into SiC of ¹H, ²H, ⁷Li, ¹¹B, ¹⁴N, ¹⁶O, ²⁷Al, ³¹P, ⁷⁵As, and ⁶⁹Ga, in the energy range 1 keV – 4 MeV. The range data for more than 40 of these implantations are previously unpublished while the remaining distribution moments have been obtained from the literature. The implantations were performed, with few exceptions, using crystalline SiC and under conditions (implantation dose and temperature) so that amorphization and significant surface swelling was avoided. For the new data, the first four distribution moments were extracted using a least square fitting procedure of Pearson functions to the concentration versus depth profiles obtained by secondary ion mass spectrometry (SIMS), exemplified for ¹¹B in Fig. 1. To acquire a compact interpolation scheme for the experimental moments analytical functions, with 2 – 4 fitting parameters each, were fitted to the data (Fig. 2). The experimental data for ¹H, ⁷Li, ¹⁶O, and ⁶⁹Ga were too scarce for this fitting procedure. To compensate this deficiency, Monte-Carlo simulations were performed to fill up the empty gaps in the moments versus energy plots of these ions. In these simulations we used the newly developed ion implantation code SIIMPL [3] which is based on the binary collision approximation [1] and was carefully calibrated to the existing experimental data of each ion.

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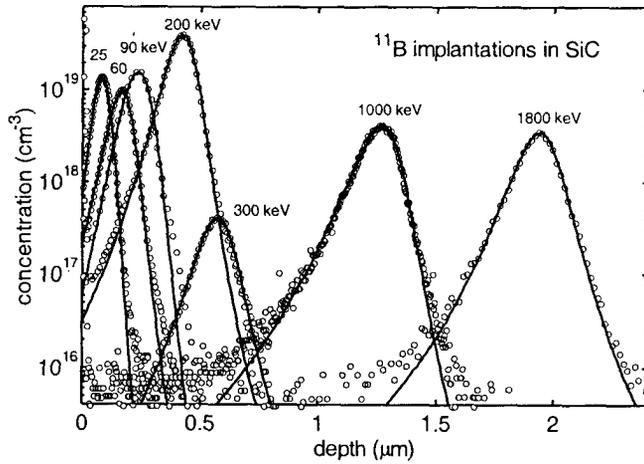
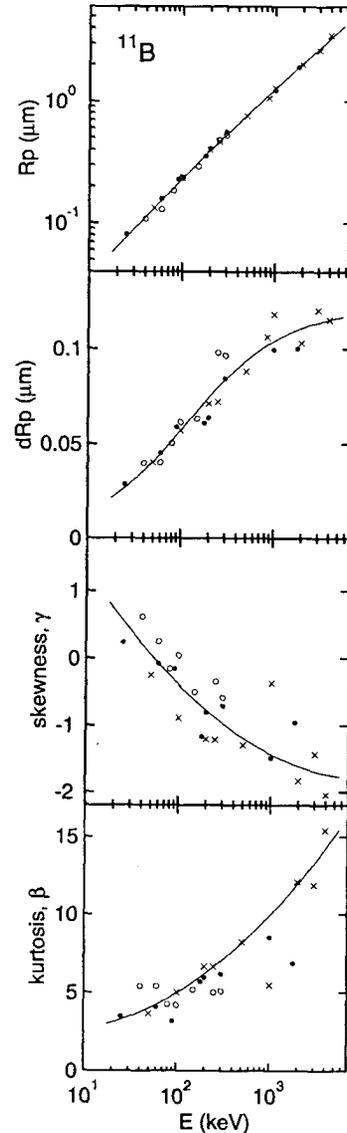


Fig. 1. SIMS measurements of concentration versus depth for ^{11}B implants into SiC (\circ). Pearson functions have been fitted to the profiles (solid lines) to extract the first four distribution moments of the implants.

Fig. 2. First four distribution moments of ^{11}B implants into SiC originating from: (\bullet) this study, (\circ) Ref.[4], and (\times) Ref.[5]. The solid lines represent least square fits of moment functions to the experimental data.



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Post-implantation annealing effects on the surface morphology and electrical characteristics of 6H-SiC implanted with aluminum.

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Ion implantation is indispensable for the fabrication of electronic devices based on crystalline silicon carbide (SiC), because the conventional thermal diffusion technique cannot be applied to the device fabrication of SiC from the fact that donor or acceptor impurities like N or Al have quite low diffusion coefficients in SiC crystal. After ion implantation, annealing at high temperatures above 1500°C is necessary to activate the dopants electrically as well as to recover the crystallinity of SiC damaged by ion implantation. Annealing at such high temperatures often makes the surface of SiC rough, which is undesirable for fabrication of electronic devices based on SiC. Thus both the surface morphology and dopant activation should be considered when optimizing the post implantation annealing process. For this purpose, we have investigated the surface morphology and electrical characteristics of 6H-SiC implanted with Al and subsequently annealed under different conditions.

The samples used in this study were n-type, 3.5°-off 6H-SiC(0001) epitaxial films grown on 6H-SiC single crystals which were purchased from CREE Research Inc. Five fold (20, 50, 110, 200 and 340 keV) implantation of Al ions was carried out to form a box profile with a mean Al concentration of $2 \times 10^{18}/\text{cm}^3$ and to a depth of 0.5µm. The samples were subsequently annealed for 30 minutes in flowing Ar gas at different temperatures of 1550°C, 1650°C and 1750°C. Different annealing periods (3 and 10 minutes) were also carried out at 1650°C and 1750°C.

The surface morphology of these samples was characterized using atomic force

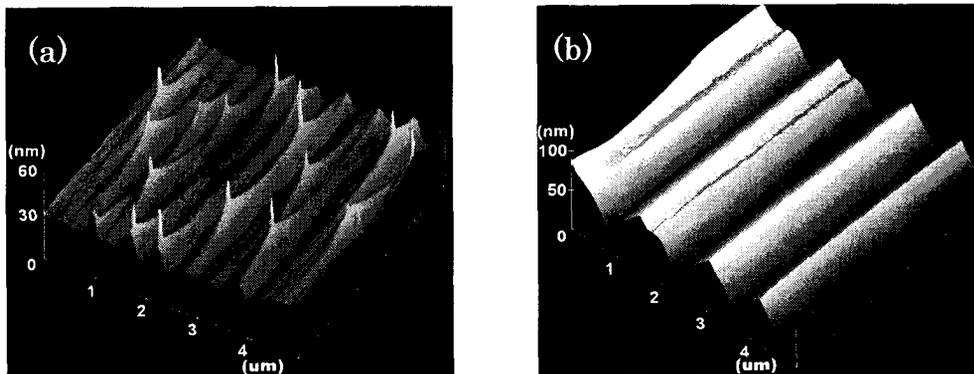


Fig.1 AFM images for Al⁺ implanted 6H-SiC(0001) 3.5°-off surfaces after annealing at (a)1550°C and (b)1750°C for 30 minutes

microscopy(AFM). All samples showed rough surfaces after annealing. Figures 1(a) and 1(b) show AFM images after annealing at 1550°C and 1750°C, respectively, for 30 minutes. While the sample annealed at 1550°C shows slender and hillock like features with sharp spike, those annealed at the higher temperature exhibits straight grooves. The orientations of these features are parallel to each other. Each groove has a plane of which direction is approximately 3.5°-off from the sample face. Some large hillocks also have the 3.5°-off plane on their surfaces. Thus these features must be huge bunches of bi-layer steps and include the (0001)-Si face as a part of their surfaces. Figures 2(a) and 2(b) show the AFM images for the samples annealed at 1650°C for 3 and 30 minutes, respectively. By increasing the annealing time, hillock-type features in Fig. 2(a) disappeared and instead groove-type features appeared as shown in Fig. 2(b). The surface morphology of the samples annealed under the other conditions can be also classified at these two types, i.e., grooves and hillocks, although the size and density of the features (grooves or hillocks) changed with annealing condition. The height and lateral size of the features increased with increasing annealing temperature and time, whereas the density of the features decreased with increasing temperature. That is, the density of hillocks/grooves depends on annealing temperature only, even though the size and/or the type of the features change at different annealing duration.

These results imply that hillocks are the nuclei of the huge step bunching, i.e., the hillocks become grooves after their growing to a certain extent. The density of grooves depends strongly on the density of hillocks at the initial stage of groove formation, suggesting that the mean distance between adjacent grooves is controlled by changing the annealing temperature. It indicates the possibility that the formation of a large amount of nuclei and their growth by annealing at low temperatures and following annealing at higher temperatures (two step annealing) provide the surface with small roughness.

The electrical characteristics of these samples will be shown and discussed in conjunction with the surface morphology in the conference.

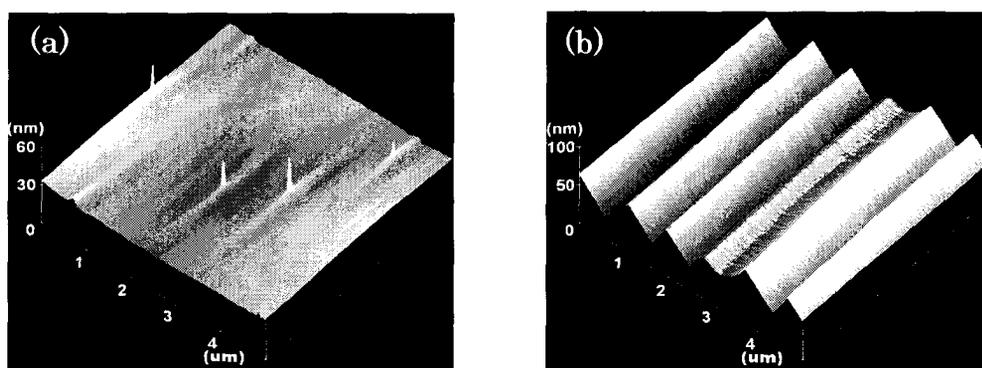


Fig.2 AFM images for Al⁺ implanted 6H-SiC(0001) 3.5°-off surfaces after annealing at 1650°C for (a)3 minutes and (b)30 minutes

Realization of a high current and low R_{ON} 600V Current Limiting Device

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Silicon carbide technologies for the manufacturing of power devices seem to be promising in the near future. The first SiC power device commercially available is a Schottky diode proposed by Infineon society (ranging: 300 V / 10 A and 600 V / 4-6 A). In the field of the SiC switches, the current trends are the Accu-MOSFET and JFET structures which exhibit the best specific on-resistance/breakdown voltage ratio experimentally obtained (Accu-MOSFET: 16 m Ω .cm²/1600 V [1] ; JFET: 10 m Ω .cm²/600 V, 14 m Ω .cm²/1800 V [2]).

The aim of this paper is to show the first experimental results of a 600 V 4H-SiC current limiting device (Fig. 1). This device limits the current which flows through it as the bias voltage between its two contacts increases. The static curves obtained from the first run (T=300 K) show a current limitation ability with a saturation voltage ranging from 10 V to 15 V. The electrical device characterization shows a $R_{ON} \approx 150$ m Ω .cm² and a current density of 100 A.cm⁻² under 50 V. The forward conduction is ensured by an N type implanted channel (doping species: nitrogen) over an P⁺ implanted layer (doping species: aluminum). The electrical characterization of the N_{CHANNEL}/P⁺ layer (analyzed by C(V) and SIMS methods) shows a good channel mobility (100 cm².V⁻¹.s⁻¹ for a 2 \times 10¹⁷ cm⁻³ N compensated doping concentration). The prototypes of the second run reach a saturation current density of 900 A.cm⁻² (Fig. 2), with a specific on-resistance of 13 m Ω .cm² (Fig. 3). The 4H-SiC current limiting devices of the second run belong to the best set of Accu-MOSFETs devices obtained in the literature.

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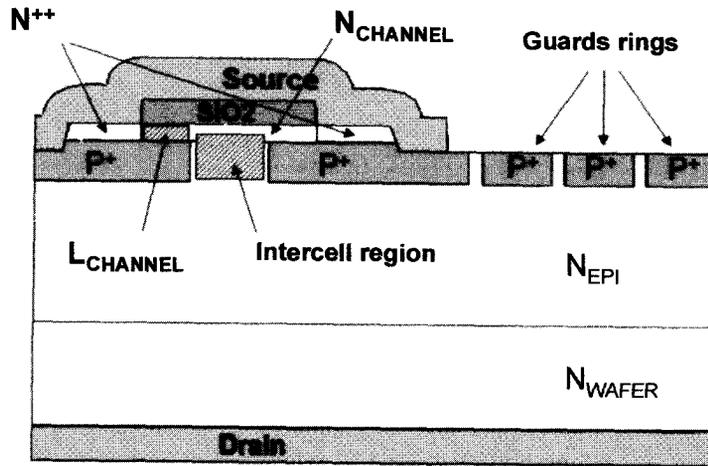


Fig. 1 : Vertical cross section of the device and its guard rings peripheral protection (the channel region, L_{CHANNEL} , and the 'intercell' region are noted).

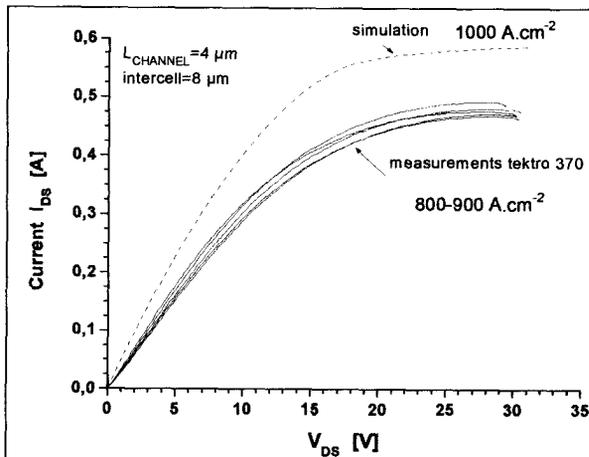


Fig. 2 : Comparison between a DESSIS ISE[®] simulation [3] and experimental results for a current limiting device (channel length : 4 μm / intercell length : 8 μm). In the experimental results using the tektronix 370 curve tracer, the temperature inside the device, particularly at the end of the channel is unknown.

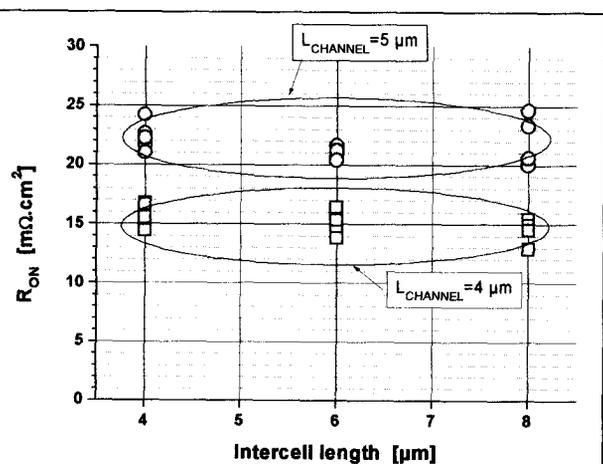


Fig. 3 : Experimental specific on-resistance plotted versus the 'intercell' length.

Unipolar and Bipolar SiC Integral Cascoded Switches with MOS and Junction Gate - Simulation Study

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Silicon carbide greatly expands the voltage range of unipolar and bipolar power devices as compared to silicon. Unipolar devices with blocking voltage of 4.5 kV and even more can ideally be made having lower conduction and switching losses as compared to bipolar devices. SiC unipolar devices thus cover the needs of most of the motor drives, switched mode power supplies and automotive applications. However, for power transmission and traction applications devices with blocking voltages higher than 10 kV are of interest. In these applications bipolar SiC devices have to be used [1].

In this study we investigated a family of integral cascode switches built upon the principle of a buried grid. The buried grid constitutes the gate of the vertical junction field effect transistor (VJFET) or thyristor (VJFET_h). It is normally shorted to the source or emitter electrode and its primary function is to take up the high voltage applied to the drain or collector. The upper part of the structure contains a low voltage VJFET or UMOSFET. The buried grid shields the upper part of the structure giving reduced electrical field at the trench corners and at the surface grid, respectively [2,3]. The surface gate of the upper part of the structure constitutes the control gate of the entire switch. The investigated switches are designed to be controlled by a gate voltages between 2 and -10 Volts. With the buried gate shorted to the source, the device is blocking full voltage with a negative voltage ≥ 10 V applied to the surface gate and it is conducting with a positive voltage of maximum 2 V applied to the same gate. Connecting the high voltage grid to the source or cathode greatly reduces the switching losses [4]. The JFET with junction gate control constitutes an alternative to the MOS technology [5]. The attractiveness of the cascode concept is that it expands the range of application of a VJFET and facilitates realisation of both medium and very high voltage switches on the basis of a single technology.

Switches with two voltage designs, 3.3 kV and 10 kV, defined as 80% of the calculated bulk breakdown value, are investigated. The 3.3 kV switches are unipolar cascodes based on a VJFET controlled by a low voltage JFET and UMOSFET, respectively. The 10 kV switches are bipolar cascodes based on a VJFET_h controlled by a low voltage JFET and UMOSFET, respectively. The 10 kV structures contain a p-type emitter at the collector side for hole injection. The cross-section of the 6 μm long upper part of the devices is shown in Fig.1. The n-base layer thickness and doping is 32 μm and $4\text{e}15 \text{ cm}^{-3}$, respectively, in the 3.3 kV design and 102 μm and $8\text{e}14 \text{ cm}^{-3}$, respectively, (plus 50 μm , $5\text{e}15 \text{ cm}^{-3}$ n-stop) in the 10 kV design. The carrier lifetime is set to 2 μs for the bipolar switches and to 0.5 μs for the SiC antiparallel diode. The channel mobility of the UMOSFET is set to 10% of the bulk mobility value. In Fig 2 the simulated data for on state voltage with 2 V (JFET) and 10 V (UMOSFET) applied to the control gate are shown. As can be seen in Figs 5 and 6 the junction gate devices show softer switching behaviour as compared to the MOS gate devices.

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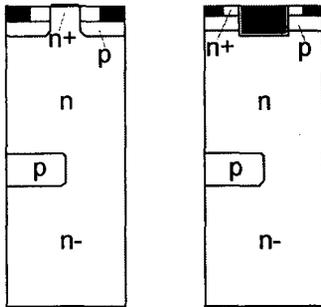


Fig. 1 Cross-section of simulated structures showing MOS and junction-type upper gates and buried lower gate.

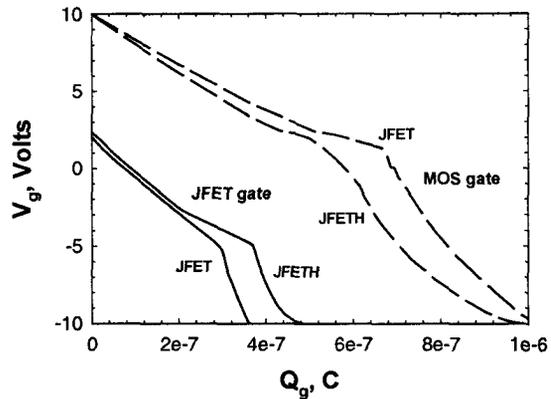


Fig. 4 Transfer characteristics (Turn-off).

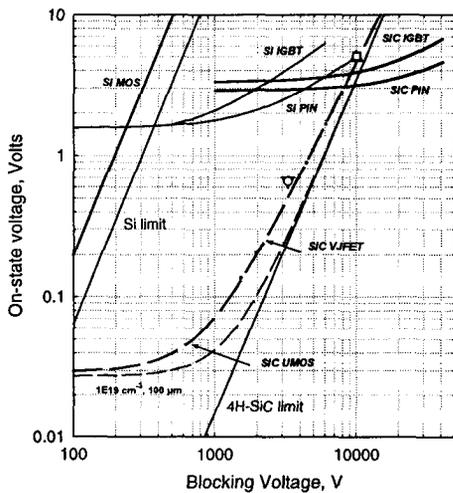


Fig. 2 On-state voltages of the simulated structures with MOS gate (empty symbols) and JFET gate (full triangles) at 100 A/cm^2 . Other data based on simulations of simple structures without buried grid [1].

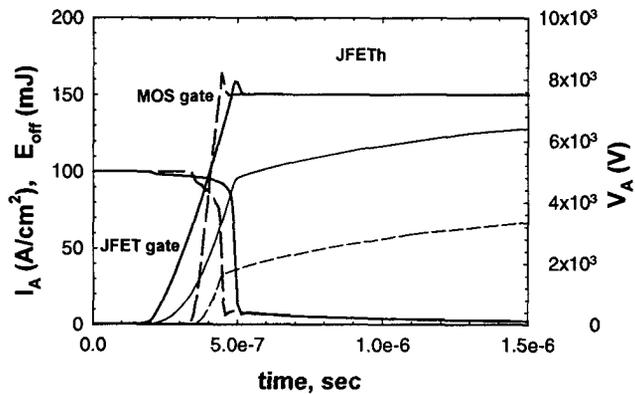


Fig 5 Turn-off of 10 kV structures, $R_g = 10 \Omega$.

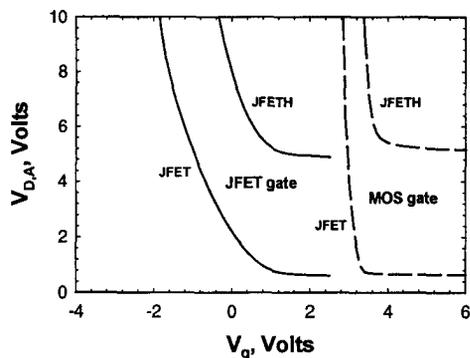


Fig. 3 On-state voltage at 100 A/cm^2 as a function of control gate voltage.

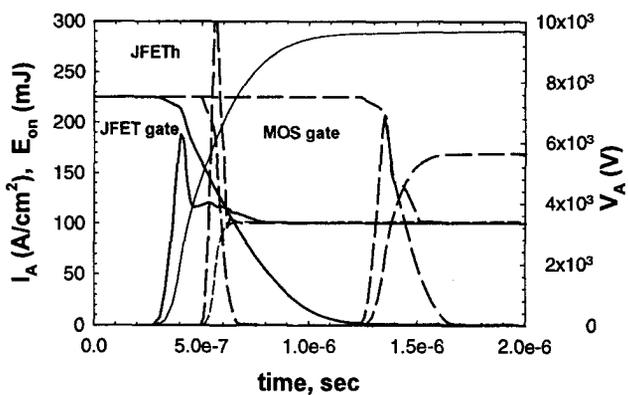


Fig 6 Turn-on of 10 kV structures, $R_g = 20$ and 50Ω for MOS case and 50Ω for JFET case.

Influence of the trenching effect on the characteristics of buried-gate SiC junction field-effect transistors

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Junction field-effect transistors (JFETs) in SiC have drawn attention due to the inherent stability of the p-n junction gate, compared to the Schottky or MOS interface, as well as their relatively simple structure. To date the viability of SiC buried-gate JFETs for high temperature and high voltage operation has been demonstrated by various groups [1,2].

For buried-gate SiC JFET structures, as in most of SiC power devices, the dry-etch is one of the most important process steps required. Plasma assisted dry etching methods are generally used techniques to etch SiC in the absence of proper wet etchants of SiC. However, deep cuts at the bottom of the sidewalls, the so-called trenching effect, are known to occur in most dry etching conditions [3]. The trenching effect is attributed to the deflection of ions on the sidewall inducing enhanced ion bombardment at the bottom.

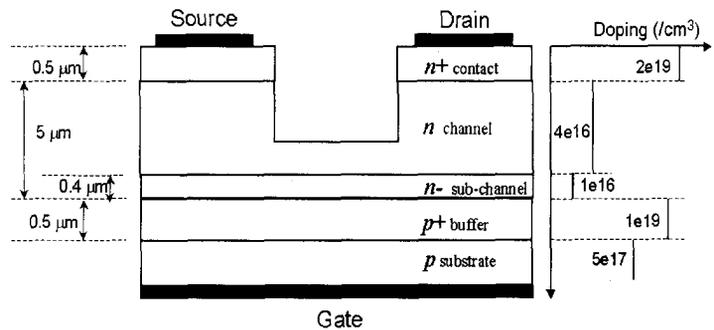


Fig.1 Cross-sectional Schematic diagram of a typical 4H-SiC buried-gate JFET

In this work, we investigate the influence of the trenching effect on the characteristics of SiC JFETs and processes for controlling the trench edge angle are presented. A 4H-SiC wafer from CREE Inc. with epitaxy grown at Linköping University is used for the experiments and the numerical simulation of the device was carried out using ATLAS software from SILVACO Inc.

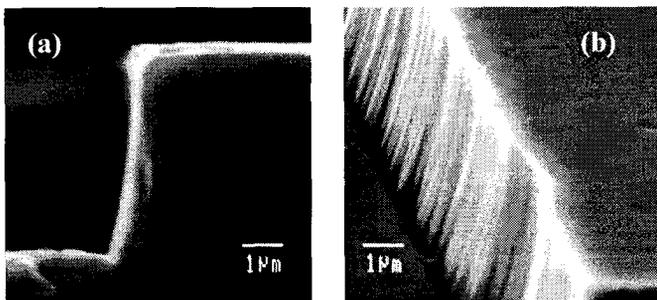


Fig.2 SEM images showing the trench effect on the bottom of the sidewall: (a) cross-sectional profile and (b) tilted view

Fig.1 shows a cross-section of the fabricated buried-gate JFETs using a two-mask layer process. The channel was formed using an inductively coupled plasma (ICP) dry etch in SF₆/Ar. Typical SEM images of the etched profile using a Ni mask, indicating good anisotropy with trenching effect, are shown in Fig.2. The etch

rate of SiC is ~ 110 nm/min and the trenching profile has depth of 0.2-0.3 μm for a ~ 4.5 μm deep etch. The simulated results on the typical structure with the trenching effect agree well with the measured data showing a slight decrease in the current density of around 10 %, but improved linearity in the gate-drain characteristics and maximum transconductances up to ~ 25 mS/mm from the measurements were obtained with devices with trenching. If the channel becomes too thin, the on-resistance increases while the pinch-off voltage decreases, which agrees well both with 1 dimensional analysis and 2 dimensional numerical simulations.

In Fig.3, typical I-V characteristics of well-saturated curves are shown. A decrease in the breakdown voltage of JFET is the most undesirable effect of trenching owing to the field crowding at the trench corner, see Fig.4-(a). To avoid this effect, a PECVD grown SiO_2 with wet-etched slope is used to transfer a sloped sidewall during dry etching of SiC as shown in Fig.4-(b) and Fig. 5. The design criteria will be discussed and an optimum design will be presented.

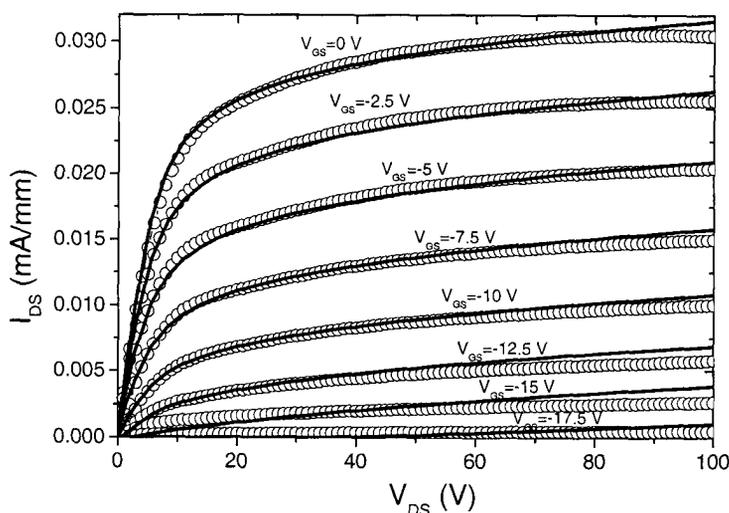


Fig.3 Comparison of simulated and measured drain current vs drain-source voltage for different gate voltages in a JFET of 5 μm channel length. Solid lines are from simulations and open circles are measured curves.

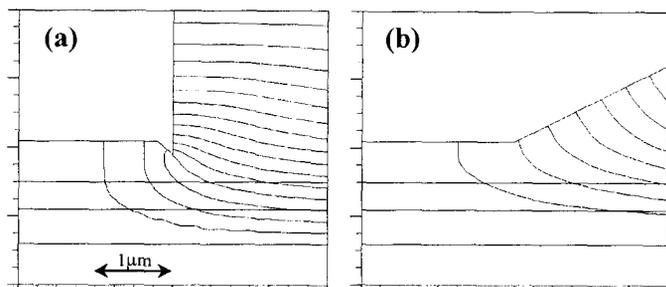


Fig.4 Simulation results showing potential distributions for two different different dry etch profiles, (a) with trenching effect and (b) with angled etching ($V_{DS}=500$ V, step of equi-potential lines = 56 V)

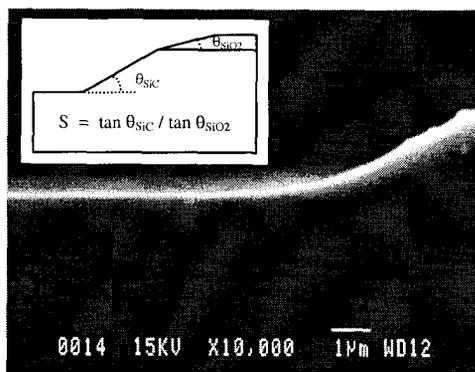


Fig.5 SEM image showing trench corner rounding using angled oxide mask after removal of oxide mask (inset; schematic diagram of oxide mask and SiC)

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Simulation study of a new current limiting device : a vertical α -SiC etched JFET- Controlled Current Limiter.

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Keyword : Silicon Carbide, current limiter, JFET, serial protection device.

Considering fault current limiters for serial protection, a lot of structures exist, from regulation to other complex systems. Up to now, only a few current limiters based on semiconductor structures have been described in papers [1],[2],[3],[4].

Although Current Regulative Diode component exist [5], their voltage and current capabilities ($V_{BR}=100$ V, $I_{max}=10$ mA), do not allow to use them in power systems. A Comparison between a Silicon and a 6H-SiC CRD (Current Regulative Diode) equivalent outline the benefits of a SiC CRD as current limiter (Fig. 1). Unfortunately, the required dimensions of implanted layers are too small in regard to current state of art of SiC technology.

Silicon carbide, owing to electrical properties, allows to foresee the realization of new power components with higher capabilities than silicon. Its band-gap energy ($3eV@300K$) and its thermal conductivity ($\lambda=4.9$ W.cm⁻¹.K⁻¹) allow to fabricate components such as diodes with reverse breakdown voltage up to 6.2 kV [6]. Figure 2 illustrates the capabilities of silicon carbide compared to conventional semiconductor materials. Factors of merits are introduced to compare those semiconductors : JFM [7], which outline the potentialities of silicon carbide, in terms of high power and high frequency with respect to silicon. Thermal and voltage capabilities of silicon carbide are advantageous to realize a current limiter. As in passive state, the voltage drop across the component must be as low as possible, in the active state, (limiting phase), a current limiter must sustain both high current and high voltage. The resulting power must not cause the component destruction. Therefore, a new bi-directional current limiter structure based on a vertical Silicon Carbide etched JFET, with both buried gate and source (figure 3) is proposed below.

This device was designed for applications like motor starting phase (figure 7), short circuit protection, circuit breaker with higher performances. Simulations were performed with ISE software [8] to evaluate static and transient electrical characteristics of the JFET, according to several specifications : voltage capability (1.7 kV), current rating (> 1A). Simulations allow to estimate geometrical and doping characteristics, (as presented in Fig. 4), as well as the technological steps required to realize such a component. Controllability (thanks to the buried gate P layer), self heating, peripheral effects on the electrical characteristics (such as fixed oxide charges) have also been analyzed (figures 5 and 6). Simulations have been performed for bi-directional devices in order to minimize power dissipation during limitation state, owing to the presence of the gate. Finally a combined peripheral protection with both field plate and JTE (Junction Termination Extension) was designed to sustain the required voltage (1.7 kV). The simulated resistance in the linear mode is 170 m Ω .cm² for the 6H-SiC device for the 1.7kV application. The fabrication of this device is currently on the way and first electrical characterization results are expected within few months.

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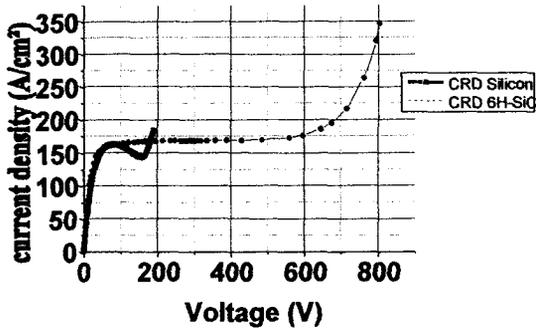


Figure n°1. Comparison between Si and 6H-SiC CRD.

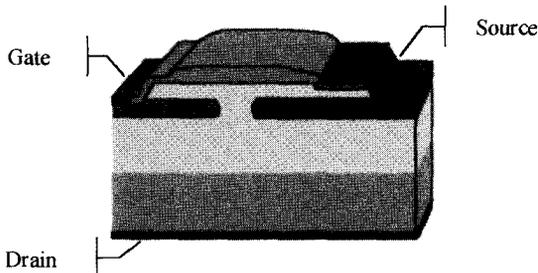


Figure n°3. Cross section view of the JFET. section

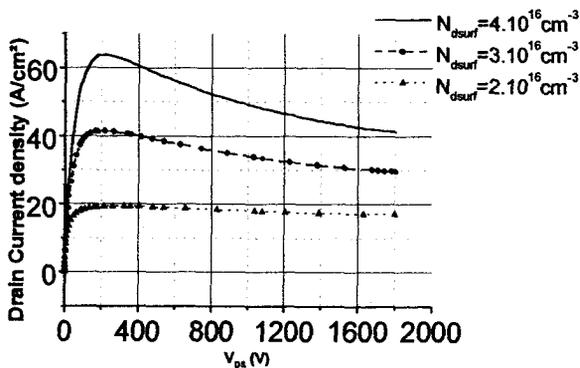


Figure n°5. Simulated drain to source characteristics of the JFET for various doping level of the top channel region.

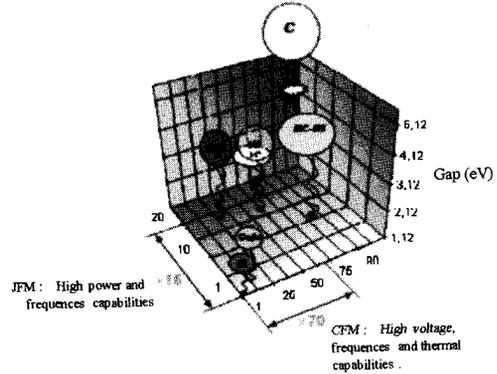


Figure n°2 : SiC versus Si, GaN...

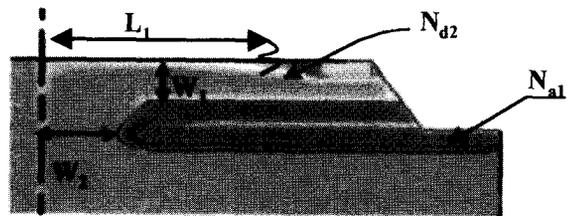


Figure n°4. Simulated cross section view of the JFET with main parameters to optimize

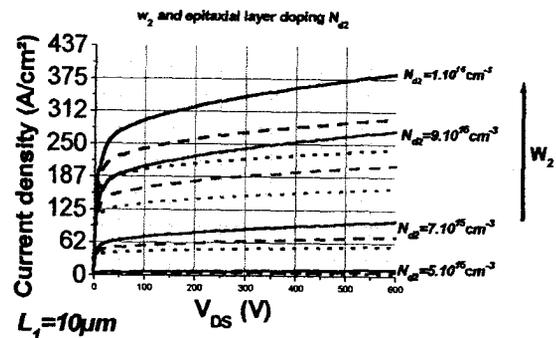


Figure n°6. Electrical characteristics for various epitaxial layer doping level and channel thickness

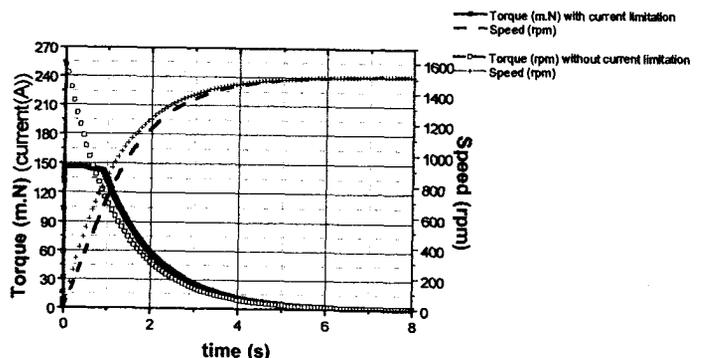


Figure n°7. Motor starting with a current limiter

Static and dynamic behaviour of SiC JFET/Si MOSFET cascode configuration for high performance power switches

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Abstract.

This paper is concerned with a detailed device and mix-mode circuit numerical analysis of SiC power switches. Two structures have been chosen, a SiC Trench MOSFET and SiC JFET coupled with a Si MOSFET in a Cascode configuration. The paper provides for the first time an insight into the physics of switching of the two structures and proves that the Cascode configuration is a superior alternative to the classical SiC Trench MOSFET owing to higher switching frequency, lower on-state resistance and reduced overall transient losses. In addition the SiC Trench MOSFET suffers from low channel mobility, may encounter oxide breakdown and punch-through during blocking mode.

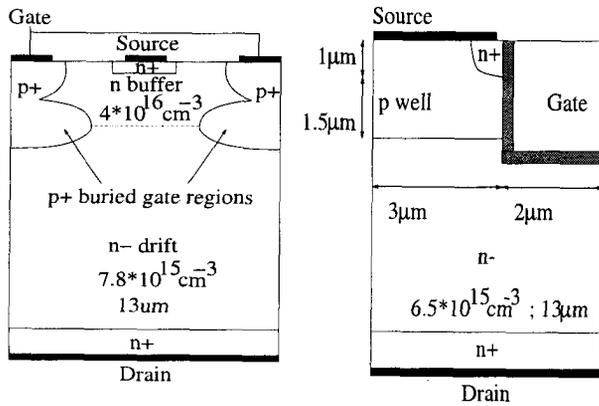
SiC JFET and SiC Trench MOSFET.

The cross sections of 1.2kV SiC JFET and Trench MOSFET are depicted in fig. 1a and 1b respectively. The SiC JFET structure consists of two main regions, the n- drift layer that supports high voltages, and the more highly doped n buffer layer, placed on the top which controls the conductive state and in particular the gate threshold voltage (i.e. pinch-off voltage) [1]. The buffer layer doping is carefully controlled to minimise the on-state resistance with no deterioration in the breakdown performance. Fig. 2 shows that the breakdown occurs below the buffer layer at the p+ gate/n-drift region interface. The doping of the drift region of the SiC Trench MOSFET is lower than that of the SiC JFET to avoid oxide breakdown. This, coupled with the high channel resistance on account of the poor channel mobility makes the on-state resistance of the SiC Trench MOSFET ($24\text{m}\Omega\text{cm}^2$) approximately one order of magnitude higher than that of the SiC JFET ($2.3\text{m}\Omega\text{cm}^2$).

Cascode Configuration.

The SiC JFET is a normally on device, and as such, not suitable in most of the power switching applications. To provide a normally-off operation and a full MOS voltage control the Cascode configuration was proposed in [2] and subsequently demonstrated in [3]. The idea is to connect the high voltage SiC JFET (e.g. 1.2 kV) in series with a low voltage Si MOSFET (e.g. 80 V) as shown in Fig. 3. The static potential sharing within the Cascode structure during the voltage blocking mode is shown in Fig. 4. An increase in the voltage supported by the Si MOSFET induces a more negative bias to the SiC JFET gate, thus blocking a higher voltage across the JFET drift region. The sharing is found to be linear in both static and dynamic conditions. No over-voltage spike is found during transient in the low voltage Si Trench MOSFET ensuring a safe high voltage switching operation. The inductive switching behaviour of the Cascode circuit has been evaluated using a load inductance of $50\mu\text{H}$ and a MOSFET gate resistance of 30Ω . The turn-off current curves are shown in fig. 5. The line voltage is 800V and the on-state current 10A. Interestingly, and unlike in the SiC Trench MOSFET, the voltage across the JFET drain-source terminals oscillates, thus producing corresponding current peaks. This behaviour is rather complex but can be briefly explained by the fact that whenever a voltage overshoot occurs on the JFET drain, the p+ gate/n- drift diode takes a high fraction of the current so that the load current is diverted through this gate junction. In fig. 6 the turn-off curves of a 1.2kV SiC trench MOSFET are shown. The device has been tested under the same conditions as the Cascode circuit. As can be observed, the SiC MOSFET turns off in 410ns, which means it is almost twice slower than the Cascode circuit, which switches off in 210ns. The difference is attributed to the reduced Miller capacitance of the SiC JFET/ Si MOSFET Cascode circuit.

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(a) (b)
 Fig. 1 Cross-sections of the (a) - SiC 1.2kV JFET and (b) - 1.2kV SiC Trench MOSFET.

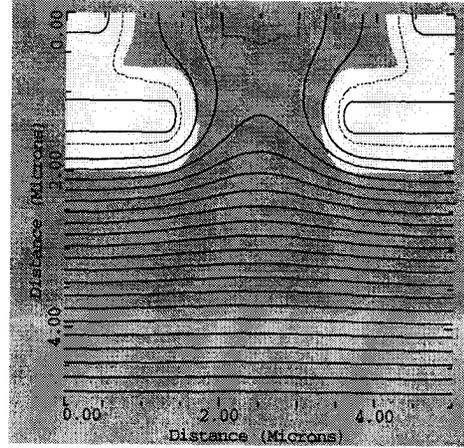


Fig. 2 Potential lines in the SiC JFET at $V_{DS}=1400\text{V}$

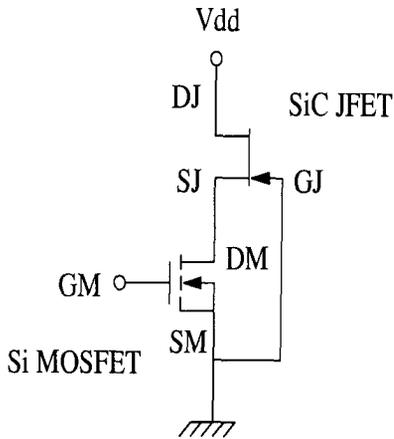


Fig. 3 The SiC JFET and the Si MOSFET connected in a cascode configuration.

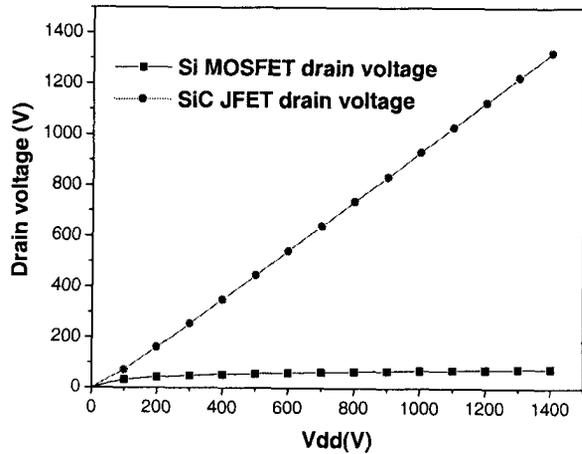


Fig. 4 The static share of the potential in the SiC JFET and the Si MOSFET

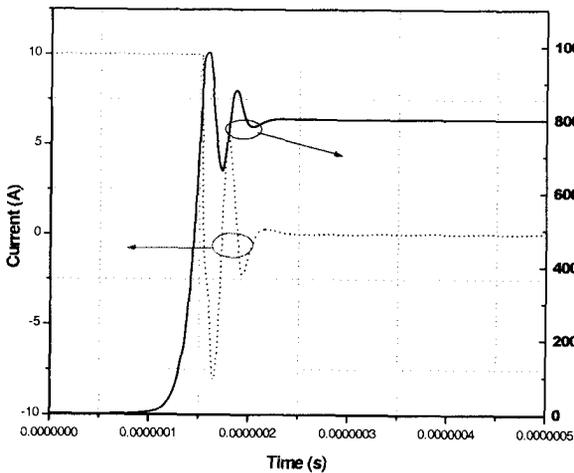


Fig. 5 The SiC JFET/Si MOSFET cascode circuit turn-off curves

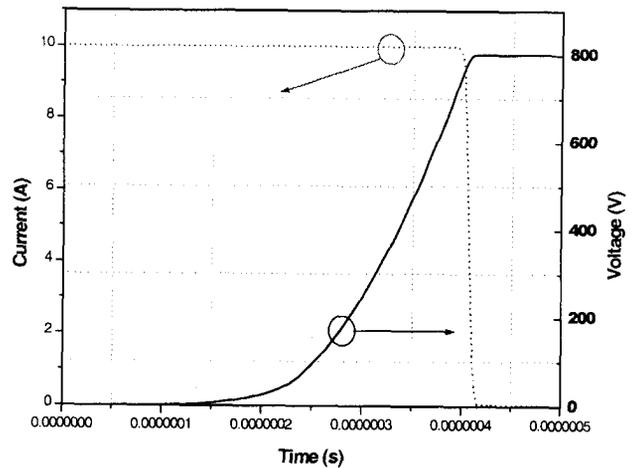


Fig. 6 The 1.2kV SiC trench MOSFET turn-off curves

Design and Processing of High-Voltage 4H-SiC Trench Junction Field-Effect Transistors

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SiC has been recognized as the choice for high-voltage, high power applications due to its superior properties such as high breakdown field and high thermal conductivity. The JFET is a basic voltage-control power device [1]. Compared with high-voltage power BJTs, JFETs have several advantages as power switching devices, such as its high input impedance and switching speed and has a larger safe operating area. Since SiC MOSFETs still need to address the low channel mobility problem [2], SiC JFET seems to be a promising alternative because the high mobility in a bulk channel. Recently, some progress has been made in SiC JFET [3].

The schematic cross-section of our vertical trench JFET structure is shown in Fig.1. The gate is formed by trench filled with P-type poly-silicon. Unlike conventional JFETs, the sidewalls of the p+ gates are isolated from the channel region with an insulating oxide. This sidewall oxide can decrease the leakage current during blocking. With the trench and sidewall oxide, it is possible to form an accumulation layer, thus will reduce the overall specific on-resistance. But the trench depth will decrease effective drift region length, this may have influence on the blocking characteristics. In this paper, we will show our recent progress in determining the performance of this JFET and proposed fabrication sequence.

In Fig.2a, we show the simulated unit cell of the JFET. The thickness of the N-epilayer is 12 μ m including the channel and the drift region. Fig.2 b shows the comparison of the forward blocking characteristics with different aspect ratios. Device with 2 μ m L_t (trench depth) and 1 μ m W_m (mesa width) achieves a blocking voltage as high as 1700V. Devices with aspect ratios of 4:2 and 3:2 have the same breakdown voltage. The electrical field at breakdown is shown in Fig. 3. The device breakdown occurs at the lower corners of the trench.

Since the drift region has a doping concentration of $1 \times 10^{16} \text{cm}^{-3}$, this JFET is normally on. The simulation results of a 2 μ m L_t and 1 μ m W_m device and devices with different aspect ratios are shown in Fig.4. The specific on-resistance of the devices with different aspect ratios is ranged from 0.7 to 1.5 $\text{m}\Omega\text{-cm}^2$ with 0 gate bias. The specific on-resistance will decrease with the mesa width increases. Also, to reduce the on resistance, we need to increase the drift region doping. But both will degrade the forward blocking capability. The simulation results of the JFET are compared with other fabricated unipolar SiC devices in Fig. 5.

The fabrication of this trench JFET is now in progress. Devices are fabricated using 4H-SiC wafers. The steps of the fabrication sequence are illustrated in Fig. 6.

We are examining a novel vertical trench JFET with low specific-on resistance and high blocking voltage. The processing steps are also presented. Device fabrication is in progress.

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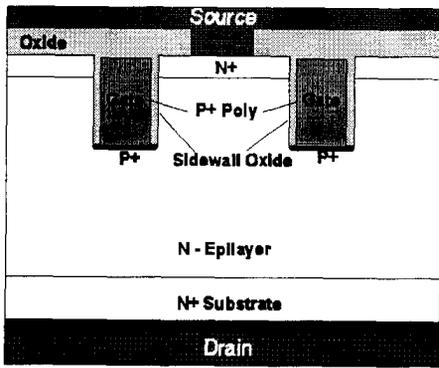


Fig. 1 Schematic cross section of the trench JFET

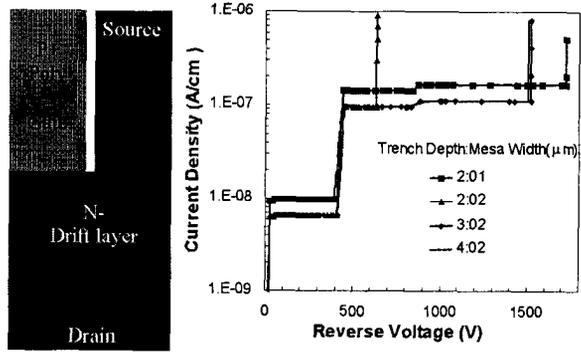


Fig. 2 Simulation structure (a: left) and forward blocking characteristics (b) of the trench JFET

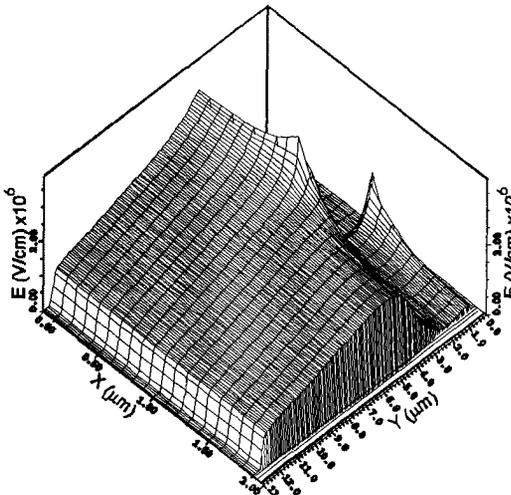


Fig. 3 Electrical field at breakdown voltage

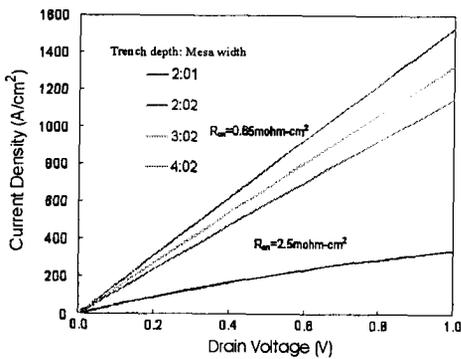
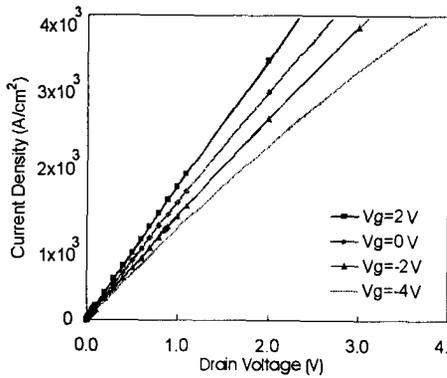


Fig. 4 Forward conduction characteristics

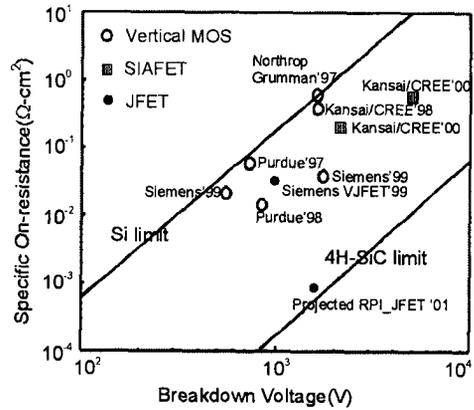


Fig. 5 Demonstrated MOSFETs and JFETs in 4H- and 6H-SiC and comparison with our projected JFET

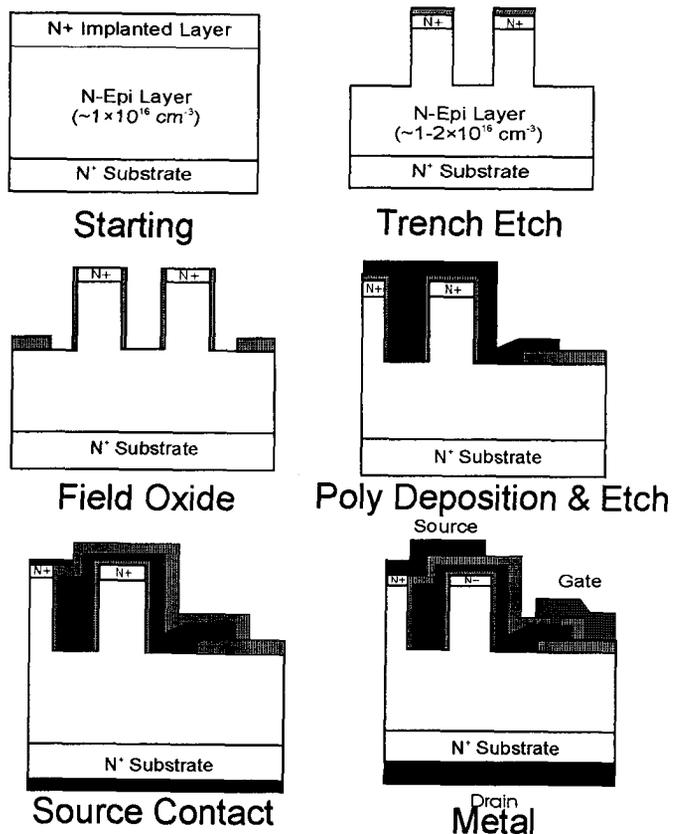


Fig. 6 Steps of the JFET Fabrication

Design and Fabrication of Dual-Gate 4H-SiC JFETs

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Dual-Gate JFETs, consisting of a buried p⁺ gate (4H-SiC(0001) Si-face substrate) layer, n-type channel layer doped in the low 10^{16} cm^{-3} , and top p⁺ gate layer were designed and fabricated. These particular devices were designed to be normally-on, with a pinch-off voltage of approximately minus one volt, for use in analog I.C.'s exposed to harsh environments. These desired parameters dictated the doping concentration and thickness of the n-type channel epitaxial layer. Following the one-dimensional design and two-dimensional simulation using Atlas software from Silvaco, the actual fabrication of these devices began with the growth of n channel and p⁺ cap epitaxial layers on 4H p-type SiC substrates. The growth was performed in a horizontal cold-wall CVD reactor on a graphite susceptor at a set point of 1535°C. The n channel layer and p⁺ cap layer were grown using a fixed Si/C ratio to establish an n-type doping level of $2 \times 10^{16} \text{ cm}^{-3}$ and the introduction of trimethylaluminum (TMA) to establish degenerate p-type doping. The two layers were grown consecutively in separate n and p⁺ growth runs. All etching was conducted using reactive ion etching, and metal deposition was conducted using DC sputtering for nickel and thermal evaporation for titanium-gold. The source and drain implantation was conducted at 500°C using nitrogen, as follows: $1.12 \times 10^{15} \text{ cm}^{-2}$ at 220 keV, $1.1 \times 10^{15} \text{ cm}^{-2}$ at 190 keV, $1.09 \times 10^{15} \text{ cm}^{-2}$ at 150 keV, and $0.92 \times 10^{15} \text{ cm}^{-2}$ at 90 keV. A photograph of the JFET die is shown in Fig. 1 along with the device cross-section. Both single-finger devices and multi-finger devices were fabricated, using gate widths of 290 μm and gate lengths of 12, 16, and 20 μm , along with test structures.

Subsequent characterization of the devices confirmed that the performance of the dual-gate JFETs was much improved over that of the single-gate JFETs. For the dual-gate JFETs, a typical pinch-off voltage around 2 volts was observed, with transconductance from 0.151 to 0.845 mS/mm. The single-gate JFETs exhibited a typical pinch-off voltage around 0.5 volts, with transconductance from 0.047 to 0.057 mS/mm. In Fig. 2, the improvements in current and gate control are clearly visible. As fabricated, the JFETs function as expected, but greater current and transconductance should be realized by simply scaling down the gate length and reducing the series resistance in the source and drain regions.

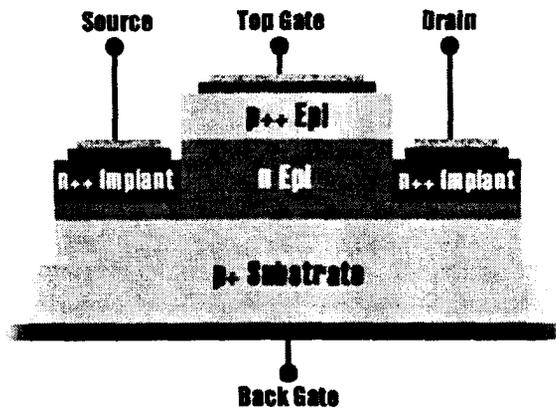
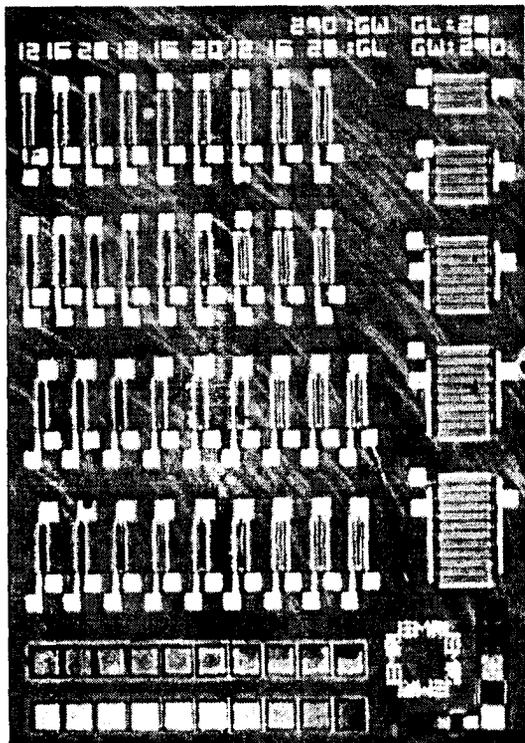


Fig. 1. Plan view (left) of the JFET die. Note varying gate lengths (12, 16, 20 μm), denoted by "GL". Also note the interdigitated multi-finger devices on the right and the TLM test structures at the bottom. The cross section (above) shows the device structure.

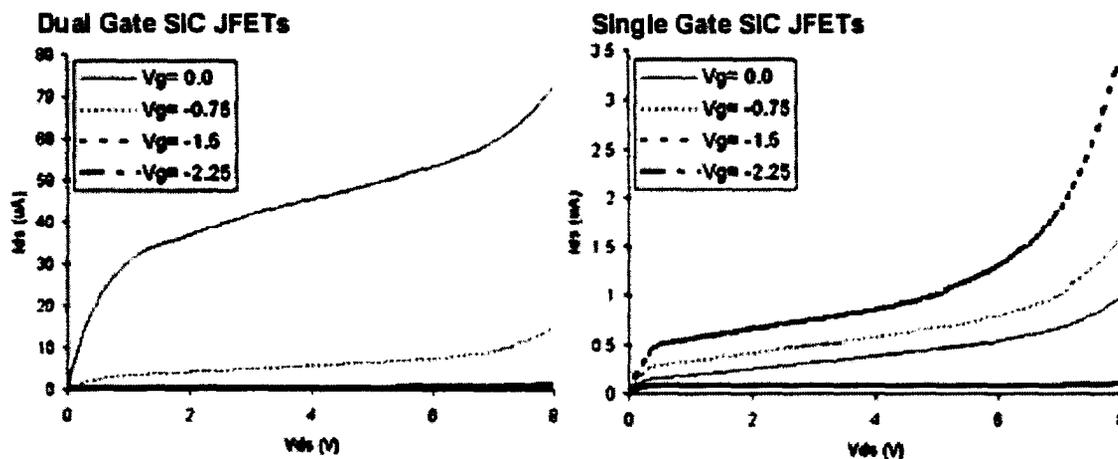


Fig. 2. Comparison of dual-gate versus single-gate single-fingered SiC JFETs with gate lengths of 20 μm and gate widths of 290 μm . Note that the ratio of I_{DS} (dual-gate) to I_{DS} (single-gate) is approximately 50 at a V_{DS} of 4V.

4H- and 6H-SiC MOSFETs Fabricated on Sloped Sidewalls Formed by Molten KOH Etching

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Introduction: SiC power MOSFETs, probably an ideal switch with normally-off operation, have suffered from an unacceptably low channel mobility. Vertical trench-gate UMOSFETs possess an advantage of higher cell density, leading to lower effective MOS channel resistance than planar DMOSFETs. SiC UMOSFETs have, however, exhibited very low inversion channel mobilities of 1~5 cm²/Vs (the best: 14 cm²/Vs [1]) and high threshold voltages of 8~15 V. This poor performance may be attributed to a high density of interface states as well as plasma damage on the sidewalls introduced during dry etching to create the trench structure. In this work, the authors have fabricated vertical 4H- and 6H-SiC MOSFETs on sloped sidewalls formed by molten KOH etching. The performance of MOSFETs on damage-free sidewalls with different slope angles and crystal orientations is discussed.

MOSFET fabrication: The schematic structure of a fabricated MOSFET is illustrated in Fig.1. The starting material was n⁺/p/n-type 4H- or 6H-SiC epilayers grown on n⁺-type off-axis (000 $\bar{1}$) substrates. Sloped sidewalls were formed by molten KOH etching at 450~500°C with 1 μ m-thick Al as a mask. The slope of sidewalls could be controlled by adjusting etching temperature, the steeper slope for the higher etching temperature. A typical cross-sectional SEM image of the sidewall is shown in Fig.2. The slope angle is approximately 36° in this case, and the surface is rather flat without roughening and faceting. After sacrificial oxidation, 45~56 nm-thick gate oxides were formed by wet-oxidation at 1050°C for 70 min. The channel length is 8.5~10.7 μ m, depending on the slope angle, and the channel width is 150 μ m. MOSFETs were fabricated on sidewalls inclined toward (1 $\bar{1}$ 00) or (11 $\bar{2}$ 0) to investigate the crystal orientation dependence.

Results and Discussion: All the MOSFETs fabricated were operational with normally-off characteristics as shown in Fig.3. The channel mobility and threshold voltage strongly depend on the slope angle, crystal orientation, and polytype, as expected. The highest mobility was 15 cm²/Vs for 4H-SiC and 32 cm²/Vs for 6H-SiC MOSFETs which were obtained on the sidewall inclined toward (1 $\bar{1}$ 00) with an angle of 36° formed by etching at 475°C. These values are reasonably high as an inversion channel mobility, compared to previous works published by several institutes (It should be noted that the bulk mobility in 6H-SiC along this direction is low, ~140 cm²/Vs, due to the large anisotropy). Figure 4 represents the average channel mobilities (μ_{FE} at $V_G \sim 10V$) determined from transfer characteristics of several MOSFETs fabricated on various sidewalls. Higher channel mobility was obtained for MOSFETs with a larger slope angle in the investigated range. Since the SiC(000 $\bar{1}$) face generally shows poor MOS interface quality, the channel mobility may have been improved by increasing the inclination (slope angle) from the SiC(000 $\bar{1}$) face in this study. Surprisingly, the MOSFETs on the sidewall 36°-inclined toward (1 $\bar{1}$ 00) exhibited a higher channel mobility, compared to the MOSFETs inclined toward (11 $\bar{2}$ 0).

This result might be inconsistent with previous works [2,3], where the $(1\bar{1}20)$ face provides low interface state density and high channel mobility. However, the sloped sidewalls have specific bond configuration different from the exact $(1\bar{1}20)$ or $(1\bar{1}00)$ faces. The threshold voltage was determined to be 2.5~4.6 V for 6H-SiC and 5.5~7.1 V for 4H-SiC MOSFETs, and was high for a MOSFET with a low channel mobility. This correlation indicates that the electron trapping and Coulomb scattering may limit the channel mobility, as in SiC(0001) MOSFETs. Thus, the choice of crystal orientation is important even in fabrication of UMOSFETs on SiC{0001} wafers.

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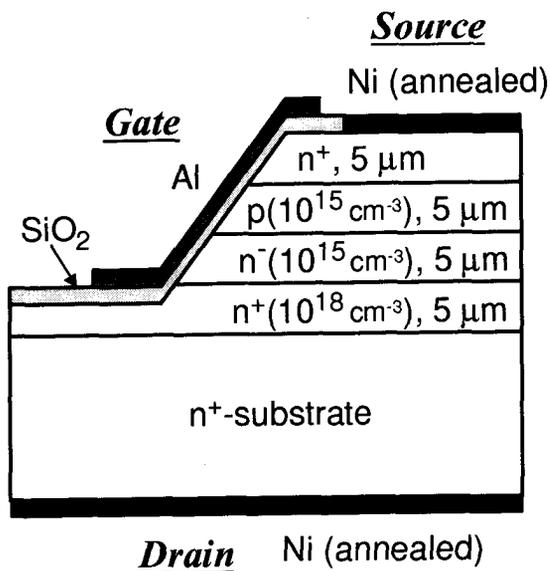


Fig.1 Schematic structure of a fabricated MOSFET.

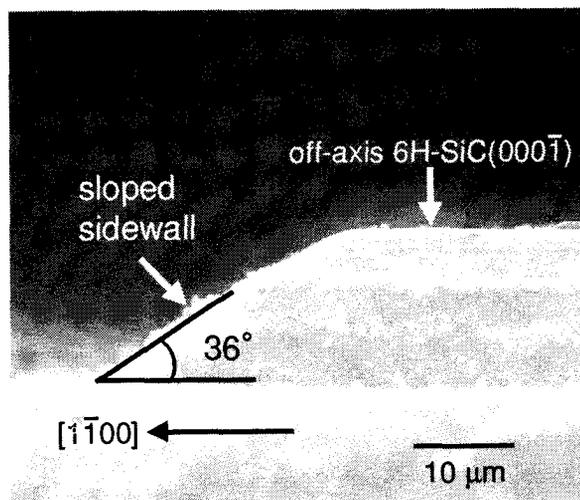


Fig.2 Cross-sectional SEM image of a sloped sidewall. (6H-SiC inclined toward $(1\bar{1}00)$, etching at 475°C)

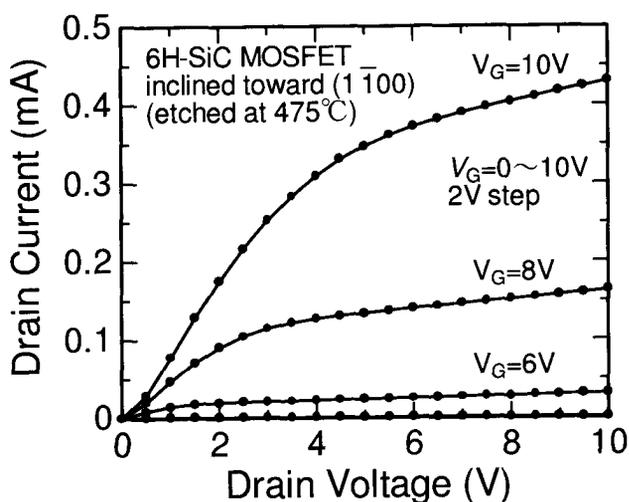


Fig.3 Typical drain characteristics of a MOSFET. (6H-SiC inclined toward $(1\bar{1}00)$, etching at 475°C)

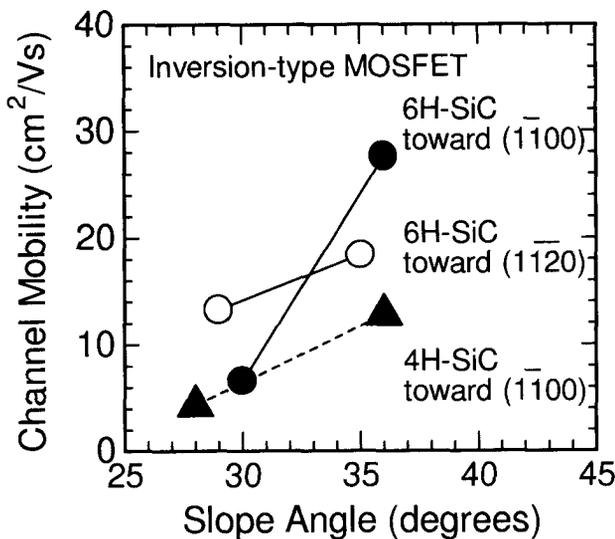


Fig.4 Channel mobility as a function of slope angle, crystal orientation, and polytype.

The development of ultra high frequency power 6H-SiC vertical static induction transistor with p-n junction as a gate

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Silicon carbide has attracted considerable interest as a material for high power, high frequency devices. The unique such properties as high thermal conductivity, anomaly large breakdown fields and others are perspective potential for a development effective devices for a microwave region particularly. During the last ten years new results from the strong field vertical (along C axis) transport study on silicon carbide polytypes were obtained which are very perspective for microwave operation [1]. In the first place it is the discovering of negative differential conduction caused by electron Bragg reflection from miniband edge in natural superlattice.

A transistor with static induction (SIT) is one of the highly efficient and power microwave device. A development of microwave SiC power transistor with vertical design has a great interest now [2]. Such transistor was formed with Shottky gate contact [3], that reduces the work temperature and radiation limits. The p-n junction employment instead the Shottky gate contact enhances these limits essentially.

On the base of n^+ -substrate we created n^- epi layer with concentration $10^{15} - 10^{16} \text{ cm}^{-3}$ and width 2-5 μm , which is covered by n^+ top layer (0.2-0.3 μm). On the base of such $n^+ - n^- - n^+$ structure by special technology the SiC unipolar static induction transistor with p-n junction as a gate have been developed for the first time. The current channel sizes were equaled to $40 \times 2 \times 3 \mu\text{m}^3$, fig.1. So far we fabricated the simple variant of this transistor with the periphery 200 microns, therewith the effective devices have the periphery 1cm and more [3]. The I-V characteristic presented SIT shown in fig.1 has two ranges: linear and breakdown (there are experimental data proving its breakdown nature). The influence of the gate voltage on the linear range is the same as in transistor. The parameter S is equaled to $S = 4 \text{ mA/V}$ (fig.2, a). It is a little value due to the little periphery. If the periphery is increased in 50 times S will be 200 mA/V. The breakdown region is caused by mobile domain which arises because of negative differential conduction caused by electron Bragg reflection from miniband edge in natural superlattice [1]. It is unusual breakdown. It arises in a field equal 150 kV/cm. This field is much less than breakdown field in 6H-SiC equal 2000-2500 kV/cm. But the field in mobile domain is much more than surrounding field in the channel and it provides the breakdown. If it is right the breakdown has to be removed by the domain destroying. It is done by subjecting the cross field of the gate to the domain. Really, we are observing at the some gate voltage a drastic current drop in the channel (Fig.2 a, b). Such switch off effect perhaps is a very interesting from developing novel device of view. A future investigation will show as far as it is the power and rapid effect. But it should be emphasized that we know how to design such transistor to remove the breakdown range and to create the device with transistor effect only.

Thus, this investigation can give the base for developing such novel devices as:

1. The unipolar microwave SiC power transistor with vertical design or SIT.
2. The microwave generator and amplifier based on the Bragg reflection effect in natural SiC superlattice.
3. The power and rapid switch off SiC device.

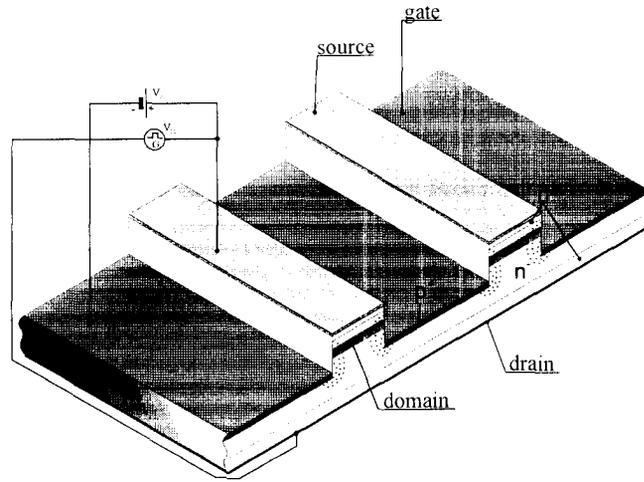


Fig.1. The common view of static induction transistor structure with mobile domain in channel.

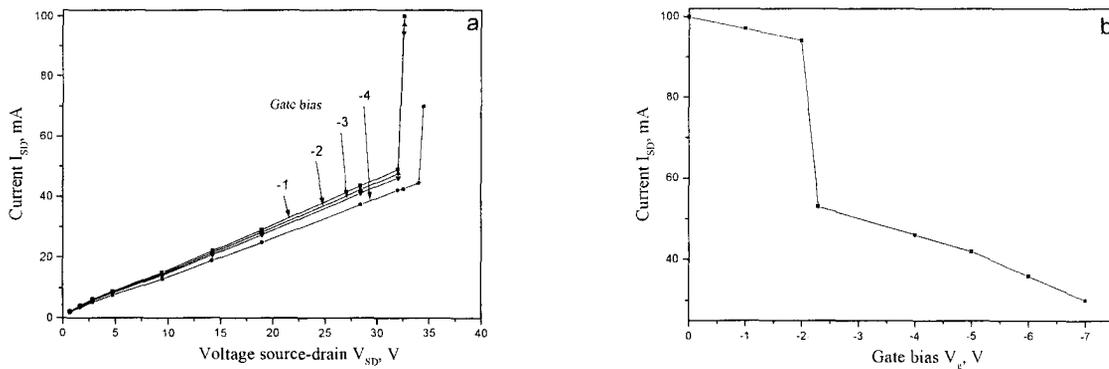


Fig.2. I_{DS} - V_{DS} characteristics (a) and I_{DS} - V_g characteristics (b).

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Fabrication and initial characterization of 4H-SiC epilayer channel MOSFETs

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Power electronics technology wants SiC MOSFETs. Although steady progress has been made, many obstacles need to be overcome to realize practical SiC MOSFETs. A promising solution to improve the on-state characteristics of SiC MOSFETs is the use of accumulation epilayer MOS channel [1, 2]. In this paper, we report on fabrication processes (especially on channel epilayer growth) and initial characterization of newly-designed 4H-SiC single-implanted epi-channel MOSFETs.

The structure of the MOSFETs fabricated in this work is shown in Fig. 1. A substrate used for the MOSFET processing was 8° off (0001) 4H-SiC. A 14- μm -thickness n-epilayer (1st epilayer, $8 \times 10^{15} \text{ cm}^{-3}$, drift layer) was grown on the substrate using our hot wall CVD system. The p-type body region ($2 \times 10^{18} \text{ cm}^{-3}$, 0.8 μm thickness) was formed by box-profile Al ion implantation ($1.8 \times 10^{14} \text{ cm}^{-2}$, 40-700 keV) through a patterned SiO₂ mask. After removal of the SiO₂ mask, a 0.5- μm -thickness n-epilayer (2nd epilayer, $1 \times 10^{17} \text{ cm}^{-3}$, channel layer) was grown onto the epiwafer. Recently, we investigated structural and electrical quality of epilayers grown on an Al-ion-implanted layer [3]. No degradation in the epilayer quality was observed for the Al implantation dose up to $1.8 \times 10^{15} \text{ cm}^{-2}$, thus we consider that the quality of the 2nd epilayer for the MOSFETs is high enough to fabricate MOS channel. Activation annealing for the p-body Al acceptors was performed just after the 2nd epilayer growth in the CVD reactor at 1750 °C for 45 min in an Ar ambient. In general, activation annealed SiC surfaces have several problems, such as bunched steps, selective desorption of Si atoms and impurity adsorption. In our case, neatly aligned steps of 30-40 nm height (this value is comparable to gate oxide thickness) were emerged and a thin layer of very low resistivity was formed on the surface. To remove the surface layer, we etched the epiwafer surface by RIE to the depth of 0.1 μm . Epitaxial growth is an effective measure to obtain flat SiC surface. To flatten the epiwafer surface, an n-type 3rd epilayer ($1 \times 10^{19} \text{ cm}^{-3}$, source contact layer) was grown onto the etched surface. After the 3rd epilayer growth, while grooves decorated by the epitaxial growth remained thinly on the surface, the surface roughness was improved markedly. Next, the surface epilayer in the channel and p-body contact regions were etched off by RIE. We set the remaining n-epilayer thickness in the channel region at 0.24 μm , aiming at normally-off MOSFET operation. A sacrificial oxide was grown at 1100 °C for 2 h. After removal of the sacrificial oxide, the gate oxidation was performed in an O₂/H₂O ambient at 1100 °C for 2 h, followed by a reoxidation in the same ambient at 950 °C for 2 h. p-Body contact and non-annealing ohmic contact to the n⁺ source and backside drain regions were formed by Al. Al gate electrode was formed by e-beam evaporation. Fig.2 shows a top view photograph of the fabricated MOSFET. The comb shape gate of the MOSFET is 5 μm long and 20x600 μm wide. Ten gate electrode fingers (each gate finger contains two MOS channels) are aligned in the 600x630 μm^2 active area.

Fig. 3 shows I_D - V_D characteristics of the MOSFET. Normally-off operation with I_D at $V_G=0$ V being

in the system noise is obtained. On-resistance calculated from the slope for $V_G=20$ V is $102 \text{ m}\Omega\text{cm}^2$. Fig. 4 shows I_D - V_G characteristics of the MOSFET. Field effect mobility, μ_{FE} , is estimated to be $13.9\text{cm}^2/\text{Vs}$ in the low V_G range. However, with an increase in V_G , the μ_{FE} decreases steeply to the normal μ_{FE} value of 4H-SiC inversion MOS channel. Details of the V_G dependence of the μ_{FE} are not clear, but we speculate that the behavior is ascribed to the near conduction band edge carrier traps, which is a vital problem in 4H-SiC MOSFETs. Typical breakdown voltage at $V_{GS}=0$ V was 350-400 V. After breakdown, melting of electrode metal was observed on the periphery of electrodes near the guard ring. The immature breakdown is possibly due to the guard ring which is not optimized. Further extensive improvements are required to obtain practical SiC MOSFETs.

This work was performed under the management of FED as a part of the METI project (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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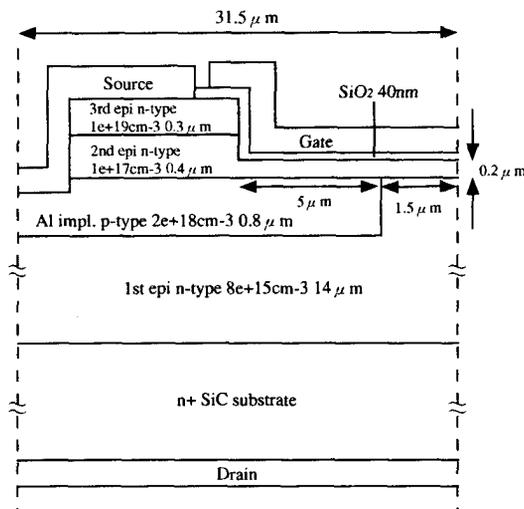


Fig.1 Schematic cross section of a MOSFET cell.

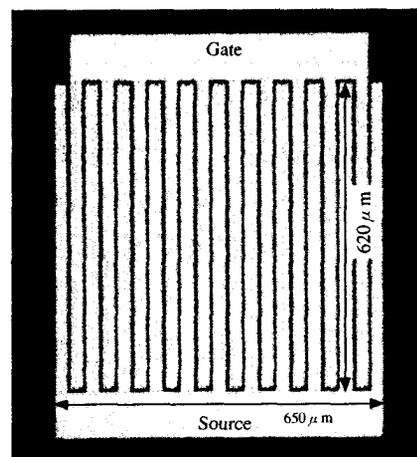


Fig. 2 Top view of fabricated MOSFET.

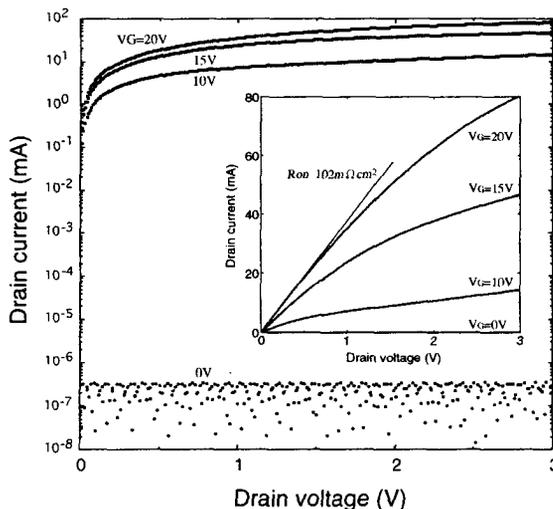


Fig. 3 I_D - V_D characteristics of fabricated 4H-SiC MOSFET.

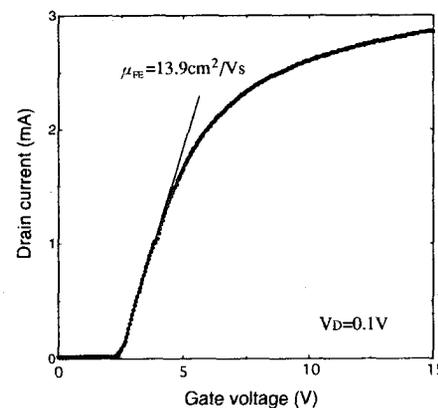


Fig. 4 I_D - V_G characteristics of fabricated MOSFET.

Evaluation of SiC MESFET structures using large signal time domain simulations

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The SiC MESFET is a promising component for applications such as high power amplifiers and high level mixers in the 2-12 GHz range. To realise these promises a good understanding of how to optimise the performance of the transistors when using real materials is needed. Semi-insulating 4H-SiC substrates have a high density of crystalline defects like micropipes, screw and edge dislocations. The substrates can also have a high density of intrinsic defects that create trapping levels in the band gap. To lessen the negative influence of the substrate, a p-type buffer layer is usually grown between the substrate and the channel layer. The resulting pn-junction aims to isolate the channel from the substrate. In this way a low parasitic output conductance at dc can be achieved. Experiments have however indicated that the large signal response of the transistor at higher frequencies can be very poor also when the dc-characteristics are good. It is therefore important to have a better understanding of how the p-type buffer layer doping and thickness affects the output rf power.

In this abstract we describe a novel way to investigate the large signal time domain response of 4H-SiC MESFETs. We have utilised the device simulator Medici in time domain circuit simulations of different SiC transistor structures. A simple amplifier circuit was used where a dc bias and an rf input voltage were applied to the gate while a dc bias and an rf output voltage were simultaneously applied to the drain terminal acting as an active matching to the transistor [1]. The matching conditions were adjusted by altering both the amplitude and phase difference of the rf voltage source at the gate and drain. The rf active matching voltage source connected directly to the drain terminal delivers a sine wave at the fundamental frequency thereby acting as a short at the higher harmonic frequencies. The results from the time domain simulations (terminal voltages and currents) were Fourier transformed and then input and output power and impedance, PAE etc as a function of frequency could be calculated. The method indicates the output power that can be achieved in the best case with pure sinusoidal input and output voltages, and we believe it to be a valuable design tool for the improvement of high frequency characteristics of power semiconductor devices. All simulations were performed with a fixed lattice temperature of 300 K. A number of SiC MESFET structures was simulated. Figure 1 shows the simulated class B drain current and voltage waveform for a structure with a 1500 nm thick p-type buffer layer with an unintentionally graded doping varying from $1 \times 10^{17} \text{ cm}^{-3}$ in the upper part to $1 \times 10^{15} \text{ cm}^{-3}$ next to the substrate. The channel layer had a nominal n-type doping of $2 \times 10^{17} \text{ cm}^{-3}$ and was 500 nm thick.

Measurements on a similar device showed a good dc characteristic with a complete channel pinch off at -9 V and a maximum of drain current of 250 mA/mm. The measured output rf power was however low.

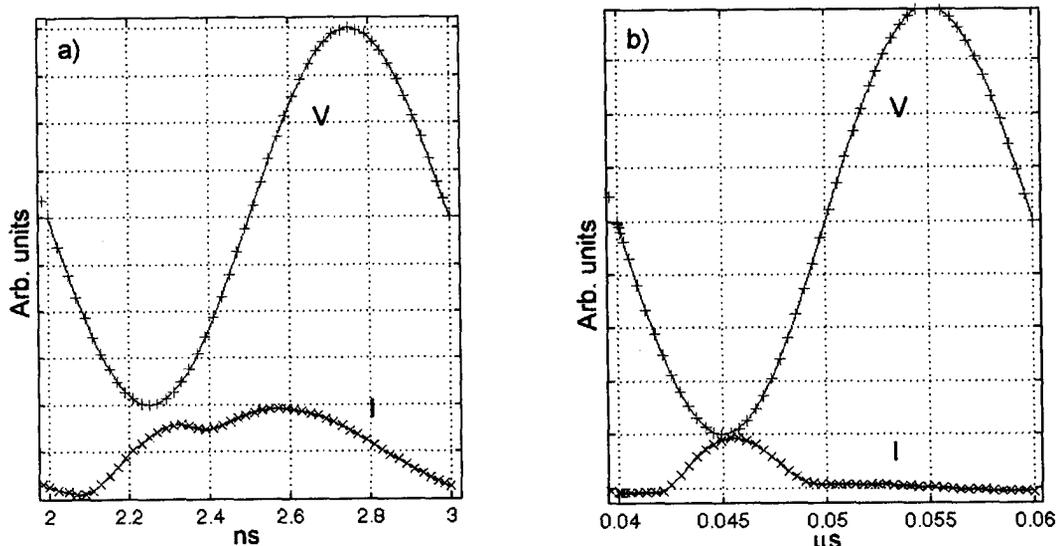


Figure 1. Class B drain current and voltage waveforms for a transistor with a thick buffer at 1 GHz (a) and 50 MHz (b).

As can be seen the device works well at 50 MHz but at 1 GHz the transistor is not delivering any power to the load due to the out of phase maximum of the drain current. The details of the simulation analysis indicated that this abnormality in the drain current is due to interaction with the p-type buffer layer. This phenomenon was not observed in dc or small-signal rf simulations.

Several other MESFET structures have been evaluated in order to obtain better rf powers. Figure 2 shows the simulated results for a structure with a 100 nm thick p-type buffer layer with a doping of $3 \times 10^{17} \text{ cm}^{-3}$. The channel layer had an n-type doping of $4 \times 10^{17} \text{ cm}^{-3}$ and was 300 nm thick. The simulation indicates an output power of 4.5 W/mm with a 56% PAE at 1 GHz.

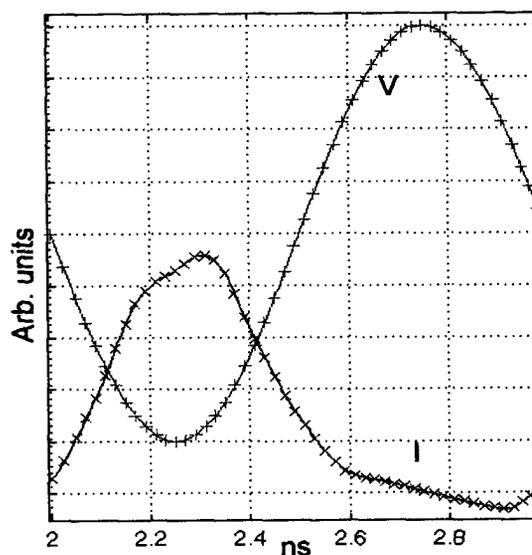


Figure 2. Class B drain current and voltage waveforms at 1 GHz for a transistor with a thin highly doped buffer.

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Surface control of 4H SiC MESFETs

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The high breakdown voltage, thermal conductivity, and saturated velocity make silicon carbide highly suitable for microwave device applications, with 80W CW and 120W pulsed demonstrated at 3.1GHz and >4W/mm power density demonstrated for SiC MESFETs [1]. However, SiC MESFETs have been reported to suffer from dispersion and instabilities in current with time. These instabilities take the form of "current collapse" when operated under CW bias conditions. This has serious implications for the use of these devices in microwave power amplifiers. The instability has been reported to be either due to surface charge trapping between the source and drain contacts on either side of the gate contact [2] or to bulk traps [3]. This work reports a significant reduction in this effect and demonstrates that the devices are capable of operation at temperatures as high as 400°C.

SiC MESFETs with sub-micron gates have been fabricated using conventional techniques as previously reported [4]. These devices have shown excellent rf power output under pulsed conditions, 17 watts has been achieved at 4GHz for a total gate width of 7.5mm, equivalent to 2.2W/mm. However these FETs show current collapse under CW conditions and the I/V characteristics are also light sensitive. Process improvements have been introduced which have virtually eliminated the light sensitivity and significantly reduced the amount of current collapse at CW. These have included an oxide passivation and a gate recess (figure 1). Devices have now been fabricated using this process and have achieved $f_T=6\text{GHz}$, $f_{MAX}=18\text{GHz}$ for a 500/0.7 μm device.

The improvement in current collapse may be illustrated by making pulsed measurements under different quiescent bias conditions. Figure 2 shows results using the modified process. The pulse measurements were made firstly with equilibrium quiescent conditions ($V_{ds}=0$, $V_{gs}=0$). The pulse measurements were then repeated with a quiescent bias corresponding to class AB operating conditions ($V_{ds}=20\text{V}$, $V_{gs}=-15\text{V}$). The pulse length was 0.5 μs , with a 1000 μs quiescent period. The optimised device shows only a small reduction in I_{dss} for the class AB operating point indicating that current collapse has been significantly improved.

Figure 3 shows a slow swept IV characteristic for a device operating at an ambient temperature of 400°C with only a ~35% reduction in I_{dss} . In addition, the gate current had only increased from <100pA/mm to 30 $\mu\text{A/mm}$. This extremely good tolerance of high temperatures suggests these MESFET devices have the potential for highly reliable operation.

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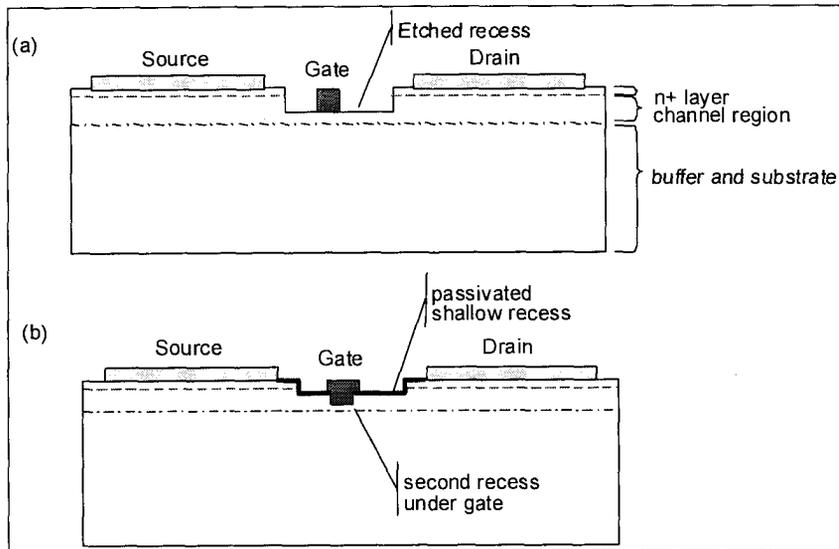


Figure 1. Schematic cross-section of a SiC MESFET. (a) conventional process, (b) improved process.

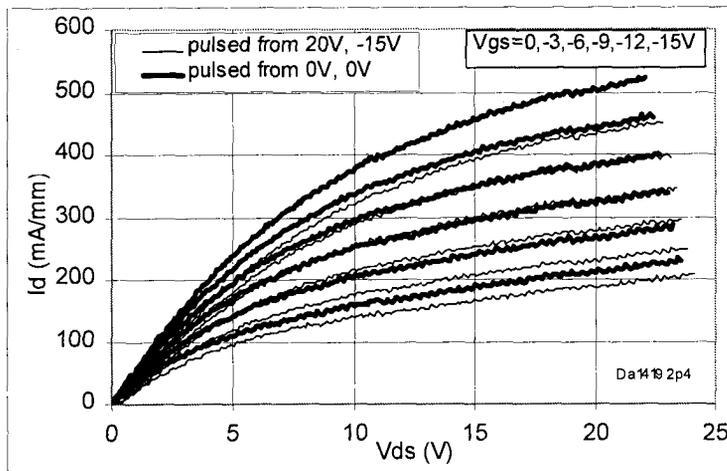


Figure 2. Pulse IV measurement of passivated 500/0.7 μm MESFET.

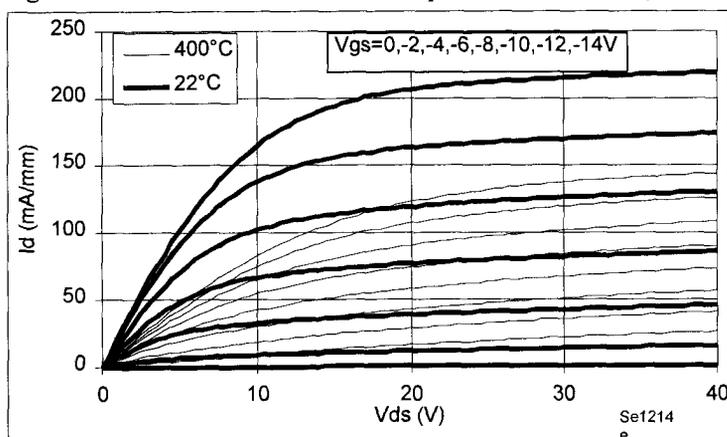


Figure 3. Comparison IV of 100/0.7 μm MESFET at 22 and 400°C.

Photon emission analysis of defect-free 4H-SiC p-n diodes in the avalanche regime

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Knowledge of the actual uniformity of avalanche breakdown in 4H-SiC diodes is of great importance when developing electronic devices operating in this regime, i.e. SiC Zener [1] and IMPATT diodes [2]. Using a photon emission setup and observing through the substrate (Figure 1) the light associated with the avalanche, we have investigated the breakdown characteristics of silicon carbide p⁺-n-n⁺ 4H-SiC diodes.

For this work, the back side of epitaxial wafer has been polished before device processing in order to allow back side observations. Detailed description of other fabrication steps and electrical characterization of these diodes can be found elsewhere [1, 2]. The diodes exhibited a stable behavior under avalanche conditions and a positive temperature coefficient of breakdown voltage which indicated the absence of microplasma or defective sites. The avalanche regime occurs around 280 V at room temperature and is characterized by a strong luminescence in the optical range (from 1.1 to 3.1 eV) (Figure 2 and 3) which can be detected and spatially resolved by photon emission techniques.

The light emission properties and its relation with the current density (Figure 4 and 5) is first investigated at forward voltage bias as well as in avalanche regime in order to determine its physical origin. The electroluminescence is then used as a tool for assessing the breakdown uniformity of the diodes.

Our results show that in the detected range, light (noted I_v) originates from the radiative recombination of injected holes in the n layer in the case of forward operation. In the case of avalanche operation, different hypothesis will be discussed. Whereas the light emission is uniform throughout the surface in the forward regime (Figure 2 (a) and (b)), it is not the case during avalanche breakdown. The breakdown seems to occur preferentially along parallel stripes independent of the diode location on the wafer and geometry (Figure 2 (c) and (d)). As the avalanche current is increased, the stripes widen and the emission tends to occur on the whole surface. To the best of our knowledge, this is the first time such observation is reported in 4H-SiC diodes. We believe that the stripes indicate regions of enhanced impact ionization but, contrary to microplasma, they do not seem to affect the electrical characteristics of the diodes and do not lead to catastrophic failure of the devices.

Similar electroluminescence striations in silicon p-n junctions at avalanche breakdown have been reported in 1963 [3]. At that time they were attributed to doping fluctuations due to the Czochralski process used to fabricate the diodes. In our case non uniform doping due to epitaxial growth can also be proposed as a mechanism for EL striations.

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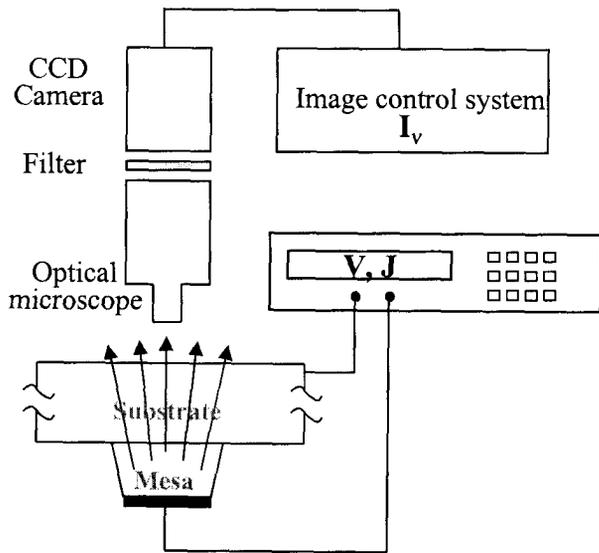


Figure 1 : Experimental setup (backside observation configuration).

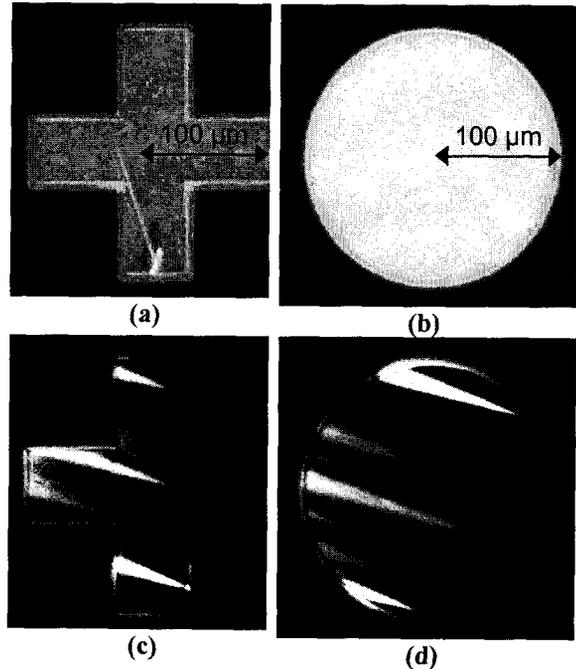


Figure 2 : Photon emission images of (a) & (b) forward biased diodes, (c) & (d) diodes under avalanche condition.

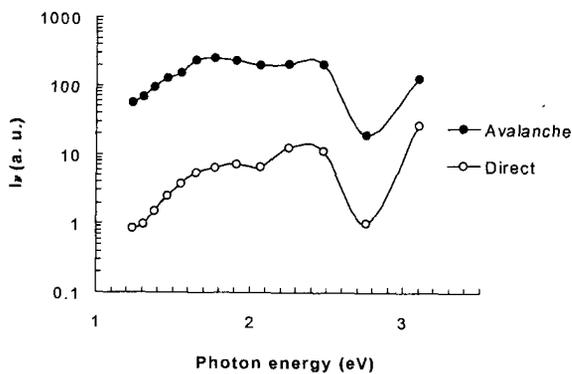


Figure 3 : Spectral analysis of the light emitted in direct and avalanche regimes.

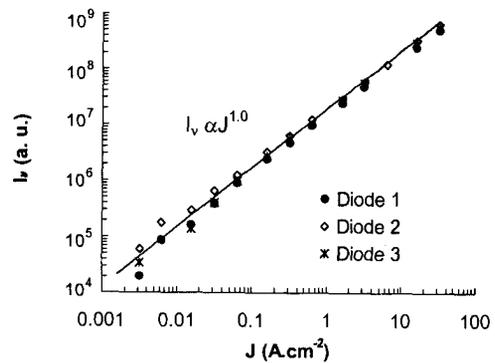


Figure 4 : Relationship between I_v and J in the avalanche regime.

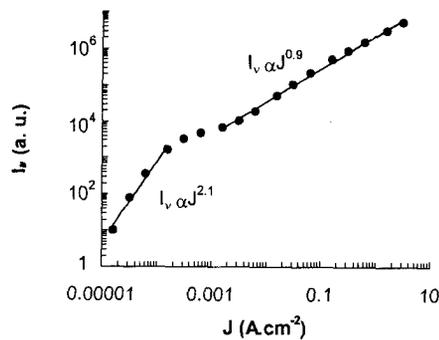


Figure 5 : Relationship between I_v and J in the recombination dominated ($I_v \propto J^{2.1}$) and injection dominated ($I_v \propto J^{0.9}$) forward regimes.

Silicon Carbide Microwave Limiters

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We report on the first microwave limiters fabricated from silicon carbide. Microwave limiters are two port microwave circuits intended to protect sensitive input circuits of communication and other microwave equipment against occasional power surges. Due to high thermo-conductivity, high operation temperature, and short recovery time, silicon carbide diodes are attractive devices to build high power microwave limiters.

We report on modeling and experimental results on development of SiC based microwave limiters. Ni based Schottky diodes were fabricated implementing all nickel technology for ohmic and Schottky contacts fabrication. We used 6H-SiC commercial epi-structure with base layer of 2.5 μm thick and doping level $2 \times 10^{15} \text{ cm}^{-3}$ for diode fabrication. Circular diodes of 200 μm diameter were fabricated. Diode chips were diced and assembled in microwave fixture for small signal microwave measurements. Small signal insertion and return loss were measured for 6H-SiC Schottky diode in the frequency band from 0.04 to 2.00 GHz. Small signal insertion loss for 6H-SiC diode loaded in parallel 50 Ω transmission line is lower than 1.5 dB up to 0.6 GHz. Return loss (reflection) varies from -25 dB at 0.04 GHz to -12 dB at 0.6 GHz and -6 dB at 2.0 GHz.

It was shown that simplified circuit consisting of two parallel back-to-back Schottky diodes with described above parameters can operate as microwave limiter up to 0.6 GHz. Broadening of operating frequency range requiring diodes and circuit optimization will be discussed.

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4H-SiC MESFET Large Signal Modeling Using Modified Materka Model

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4H-SiC(silicon carbide) MESFET large signal model was studied using modified Materka-Kacprzak model [1]. The MESFET characteristics for the large signal model were obtained from a device simulation using Silvaco's 2D device simulator, ATLAS. The simulated device structure is shown at Fig 1 [2]. The device simulation results was compared with the reported data of the same structure [1] and showed a good agreement. The small signal and large signal model was established from the MESFET characteristics. For the large signal modeling modified Materka model was employed. Fig 2 and Fig 3 show the comparison between simulated and modeled data. The small signal model showed a good match between measured (simulated) and modeled data with a small error rate in S-parameters (Table 1). The modeled large signal parameters are shown at Table 2. Both measured (simulated) and modeled results showed identical DC characteristics, i.e., -8V pinch off voltage, G_m of 45ms/mm and I_{DSS} of 270mA/mm under $V_{GS}=0V$, $V_{DS}=25V$ conditions. Based on the large signal parameters, power characteristics are predicted. From the Class A power simulation at 2GHz and at the bias of $V_{GS}=-4V$ and $V_{DS}=25V$, a 10dB Gain, a 34dBm (1dB compression point) output power, a 7.6W/mm power density, and a 37% PAE(power added efficiency) were obtained (Fig. 4). The power simulation results are compatible with the reported results. As the IIP3 (input third order intercept point) is about 10 dB higher than input P1dB, IIP3 is expected to be around 34 dBm.

Acknowledgement

This work was done as a part of SiC Device Development Program(SiCDDP) supported by MOCIE(Ministry of Commerce, Industry and Energy), Korea.

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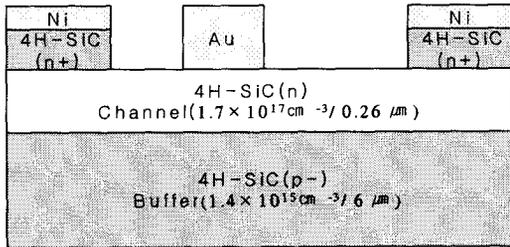


Fig 1. Cross section of a 4H-SiC MESFET

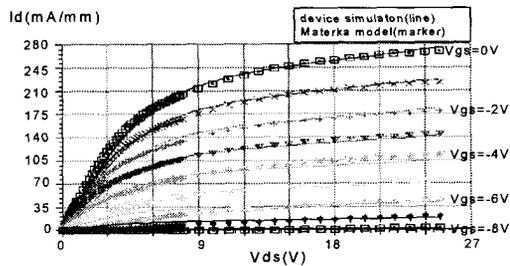


Fig 2. I-V characteristics of a 4H-SiC MESFET

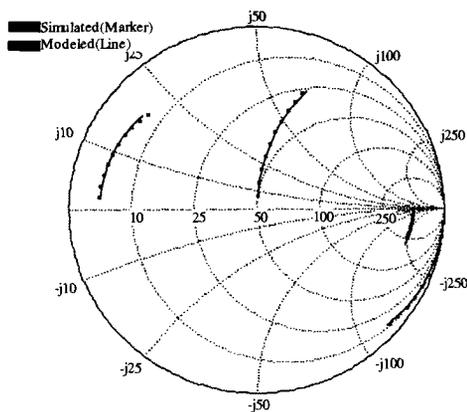


Fig 3. Simulated and Modeled S-parameter at $V_{GS}=-4V, V_{DS}=25V, 1GHz-10GHz$

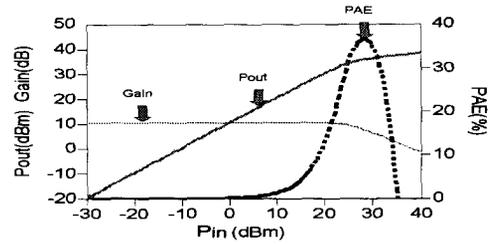


Fig 4. Power simulation for a 4H-SiC MESFET at 2GHz

S_{11}	S_{21}	S_{12}	S_{22}
2.2%	6.7%	3.6%	4.5%

Table 1. Error rate of simulated and modeled S-parameter

$IDSS$ 0.6879E-1 (A)	KI 1.6
$VP0$ -8 (V)	CIS 0.127E-13 (F)
$GAMA$ -0.125E-1 (1/V)	$CF0$ 0.605E-13 (F)
E 0.92	KF 0.62 (V)
KE -0.115 (1/V)	RG 3.45 (Ω)
SL 0.17E-1 (A/V)	RD 5.13 (Ω)
KG 0.25E-2 (V)	RS 3.57 (Ω)
T 0.39E-13 (sec)	LG 0.54E-10 (H)
SS 0.95E-3 (A/V)	LD 0.19E-10 (H)
$IG0$ 0.1E-30 (A)	LS 0.84E-09 (H)
$AFAG$ 20.55 (V)	CDS 0.11E-13 (F)
$IB0$ 0.25E-2 (A)	$CDS0$ 0.12E-08 (F)
$AFAB$ 1.2 (V)	$RDSD$ 706 (Ω)
VBC 200 (V)	CGE 0.82E-13 (F)
$R10$ 13.99 (Ω)	CDE 0.85E-14 (F)

Table 2. Large signal model parameter of 4H-SiC MESFET at 1-10GHz

Optical Properties of Metallic Nanocrystals in SiC

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ABSTRACT

by implanting Au, Ag, Cu, and keV Sn into SiC at room or elevated temperature followed by annealing at various temperatures. Using optical absorption spectrophotometry, we determined the location of the absorption band due to metal nanocrystals in SiC, as well as their average size. Elevated temperature implantation reduces optical absorption in the substrate due to ion implantation induced defects.

INTRODUCTION

The exceptional properties of SiC, as a high-temperature wide-bandgap semiconductor possessing a high index of refraction and high fracture toughness, make it a suitable candidate for device fabrication in harsh environments. In recent years, more attention has been given to both linear and nonlinear properties of the material caused by optical absorption due to the

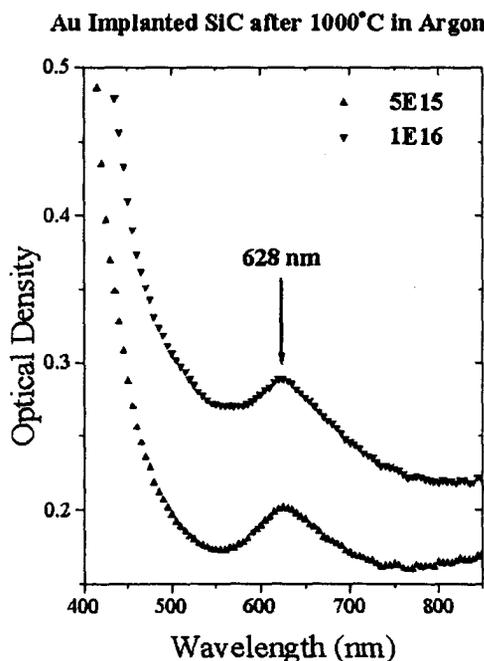
the SiC used in this work was 2.26. From Equation (2) one can predict the photon wavelengths for the surface plasmon resonance frequencies for metallic colloids in the photorefractive host materials. For the in-house measured index, $n_0 = 2.26$, the absorption bands for SiC with Au, Ag, Cu, and Sn colloids shift to 625 nm, 509 nm, 617 nm, and 382 nm, respectively.

RESULTS AND DISCUSSION

We have implanted SiC crystals with ions such as 2.0 MeV Au, 3.0 MeV Ag, 2.0 MeV Cu, and 100 keV Sn at fluences between $5 \times 10^{15}/\text{cm}^2$ to $3 \times 10^{17}/\text{cm}^2$ both at room temperature and at 500°C .

Figure 1 shows typical optical absorption spectra for SiC implanted with MeV Au and annealed at 1000°C in ambient argon. As implantation fluence increases the absorption baseline shifts. Using the measured absorption band, 628 nm, and Equation (2), the calculated index of refraction for SiC at the implanted volume is 2.3. As the annealing temperature increases, the index of refraction becomes larger, resulting in a red shift in the absorption band.

Figure 1. Gold implanted SiC, after heat treatment, at two different ion fluences.



Similar results for Ag, Cu and Sn implantations produced absorption bands at 493 nm, 659 nm, and 406 nm.

CONCLUSION

Metallic nanocrystals formation was observed in SiC implanted with Ag, Au, Cu and Sn ions. Implantation at room temperature results in a large increase in optical absorption that can mask the surface plasmon resonance absorption band. Implanting at elevated temperature (500°C), which inhibits the formation of defects, alleviated this difficulty. The broad plasmon resonance for each absorption band indicates that the nanocrystals are very small.

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