

Poster Session I

Micropipe Formation Model via Surface Step Interaction

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Flux Controlled Sublimation Growth by an Innerguide-Tube

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A New Type SiC Gas Sensor with a pn-Junction Structure

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An Effective High Voltage Termination for SiCPlanar pn Junctions for Use in High Voltage Devices and UV Detectors

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Micropipe Formation Model *via* Surface Step Interaction

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Silicon carbide (SiC) single crystals, a promising material for high power and high temperature semiconductor devices, still suffer from crystallographic defects, so-called "micropipes." Micropipes are known to be hollow defects aligned along the growth direction of the crystal. As they penetrate the entire crystal, they are a significant problem in growing high quality SiC single crystals, since they become "killer" defects if they intersect the active regions of SiC devices. The origin of such hollow defects was proposed by Frank [1] who considered dislocations with an extremely large Burgers vector. If the Burgers vector of a dislocation exceeds a critical value (approximately 2nm), then it is, due to large strain energy, energetically favored to remove the core material and to produce an additional surface in the form of micropipe.

The magnitude of the Burgers vector of micropipes in SiC crystals ranges from 2 to greater than 10 times the unit c lattice parameter. In principle, a dislocation with a Burgers vector of multiple unit cell size $b=nc$ is energetically unfavorable compared to a distribution of n elementary dislocations with a Burgers vector $b=c$. Thus, if a screw dislocation with a Burgers vector nc (super screw dislocation) exists, it would tend to dissociate into n separate unit c screw dislocations. In other words, screw dislocations with the same-sign Burgers vector repel each other. However, super screw dislocations (micropipes) are easily produced in SiC crystals and stably propagate during crystal growth. These experimental observations are not satisfactorily understood yet, and how dislocations are brought together to produce micropipes and why such super screw dislocations are stable in SiC crystals are still puzzling questions.

In this paper, we propose a micropipe formation model *via* surface step interaction, where the strong repulsive interaction between surface steps on the SiC(0001) surface is a major driving force for coalescing unit cell size screw dislocations.

There are three elements that are necessary for this mechanism to be operative. First, a high density of screw dislocations is needed to feed the process. Micropipes are very often observed at the foreign polytype and secondary phase inclusions during growth, where high density screw dislocations are introduced. Second, a large repulsive interaction between surface steps is required for the coalescence of unit c screw dislocations. This is explained by the large step height and stiffness observed on the SiC(0001) surface [2]. Finally, once micropipes are formed, they need to stably propagate in SiC crystals. Spiral growth mechanism ensures stable lateral advancement of steps of multiple unit cell height, which kinetically prevents the dissociation of the bunched steps and thus prevents micropipes.

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The development of 2in 6H-SiC wafer with high thermal conductivity

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1 Introduction

6H type SiC, which is known as a wide gap semiconductor, is recently taken notice as substrates for GaN and SiC epitaxial layers. Their applications of optical and high frequency devices require high quality substrates with high and low-resistivity, respectively.

In this research, we made 2 in, high quality 6H type SiC bulk single crystals by the sublimation method, and successfully controlled their conductivities.

2. Experiments

Bulk single crystals were grown by the sublimation method. The crucible assembly consisted of a graphite support to which the seed crystal was attached and a graphite crucible containing the source powder. Mirror-polished SiC wafer was used as the seed crystal. The seed crystal and the source powder in the crucible were heated between 2200 °C and 2400 °C in the atmospheric pressure of inert gases. During the crystal growth, total pressure was 1 ~ 10kPa, and nitrogen gas was introduced into the furnace as the dopant for the crystal with low resistivities .

3. Results

We successfully made 2 in N-doped and undoped 6H type SiC single crystals. Fig.1 shows N-doped and undoped 2in 6H-type SiC. We measured the electrical, crystallographic and thermal characteristics.

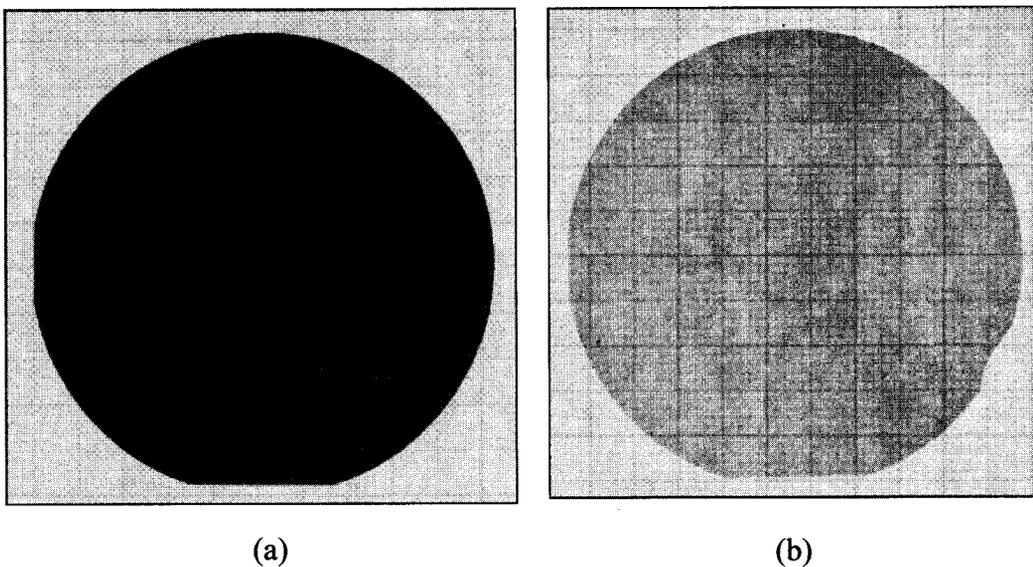


Fig.1 (a)N-doped and (b)undoped 6H-SiC wafer

(1) Electrical characterization

The resistivities of N-doped and undoped wafers, measured on the van der Pauw method at room temperature, were $0.04 \Omega \cdot \text{m}$ and $>10^5 \Omega \cdot \text{cm}$, respectively. We confirmed that these values are low and high enough for optical and high frequency respective device applications

(2) Crystallographic characterization

We etched these wafer surfaces by molten KOH at 500°C , and observed them by the optical microscopy. The micropipe densities of low and high-resistivity wafers were 29cm^{-2} and 22cm^{-2} , respectively.

X-ray diffraction measurement was conducted using a double-axis diffractometer, where a four-crystal monochromator was used for Cu K α 1 radiation. The rocking curves of both low and high-resistivity wafers showed a narrow single diffraction peak with FWHM of 34 arcsec at the center of each wafer. We confirmed that each wafer has low dislocation densities and the low disorder of lattice arrangement.

(3) Thermal characterization

We measured the thermal conductivity of the undoped wafer and the N-doped wafer, which were 471W/mK and 420W/mK , respectively, by the alternative optical method at room temperature (300K). These are above that of Cu (400W/mK) and as high as the value ever reported on the 2 in wafer grown by the seeded sublimation method. Fig.2 shows the temperature dependence of the thermal conductivity.

At 600K , the thermal conductivity of the undoped wafer and the N-doped wafer were 190W/mK and 210W/mK , respectively.

When the temperature was raised, the thermal conductivity of the 6H-SiC with low-resistivity came to exceed that of the 6H-SiC with high-resistivity. In the thermal conductivity model, there are two mechanisms, which are due to the lattice vibration and the free electron. In general, the thermal propagation by the lattice vibration becomes predominant at the low temperature and the thermal propagation with the free electron becomes predominant at the high temperature. The nitrogen impurities in 6H-SiC promotes the thermal propagation with the free electron though suppresses the thermal propagation with the lattice vibration. Therefore the thermal conductivity of N-doped SiC has less temperature dependency and is even higher than that of undoped SiC at high temperature.

4. Summary

We successfully made 6H-SiC with high thermal conductivity and confirmed that they had low dislocation density and low disorder of lattice arrangement.

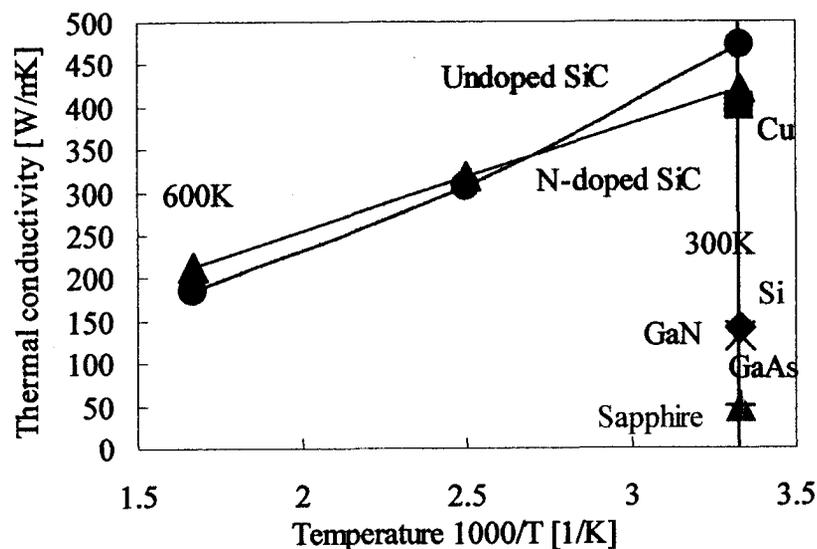


Fig.2 Temperature dependence of thermal conductivity

Flux Controlled Sublimation Growth by an Inner Guide-Tube

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Silicon carbide (SiC) power devices are expected to reduce energy loss of the electric power converter dramatically. The improvement of the quality and the enlargement of SiC substrate are problems for practical use of the SiC power devices and their applications. Single crystal growth of a high quality and large diameter bulk SiC is the technological point for the above problems. Single crystal of the bulk SiC has been grown by modified Lely method (sublimation method) [1]. Enlargement of single crystal from small seed crystal has been investigated using the modified platform on which the seed crystal was attached [2]. But we found that the quality of the single crystal was degraded by polycrystals grown around the single crystal. In this work, we newly developed the inner structure of the crucible in order to enlarge the single crystal without polycrystal around it. The effect of the growth parameters on the shape and the quality of the crystal was investigated.

SiC bulk single crystals were grown in an RF induction furnace. An inner guide-tube in the shape of a hollow truncated cone was installed between a seed crystal and source material. It was supported on the inner wall of a cylindrical graphite crucible. (Fig.1) This guide-tube functioned to control flux of sublimation gas from source material and formed a growth space separated from the polycrystal and the extra space. The geometrical parameters of the guide-tube are shown in Fig.1. The temperatures of the top and bottom of the crucible were in the range of 2150-2250°C (T_{top}, T_{bottom}). Since the temperature of the guide-tube (T_g) was important for the crystal growth, T_g was controlled indirectly changing the RF coil position and/or the geometrical parameters of the guide-tube. The effect of the growth conditions such as the geometrical parameters and temperatures on the shape and the quality of the grown crystals was examined. In comparison, crystals were also grown in a simple crucible without the guide-tube. The crystal quality was characterized by polarizing microscopy and X-ray topography.

A crystal ingot grown in the crucible with the guide-tube is shown in Fig.2. The single crystal was successfully grown separated from polycrystal. The ratio of the growth rate of single crystal and polycrystal was the range of 1.5-4 depending on the growth parameters and typical value was around 2. That ratio was 0.7-1 in the case of growth without the guide-tube. This means that the guide-tube enhanced the growth rate of the single crystal relatively compared with that of the polycrystal by controlling flux of sublimation gas. It is possible that the single crystal is grown separated from polycrystal selecting the height of platform (H), the gap between the platform and the guide-tube (x, y) and growth time. The broadening angle of the single crystal could also be controlled by changing the taper angle of the guide-tube (θ) and the angles in the range of 0-30° were practically obtained. Crystal defects such as crack, subgrain boundary and macrodefect were drastically reduced compared with that of the crystal grown together with the polycrystal. X-ray topography images of the single crystals

with and without the polycrystal are shown in Fig.3. Misoriented areas in the periphery were observed in the both crystals but the patterns were different. The periods of the patterns was larger in the crystal without polycrystal. There still remained misoriented areas even though the effect of the polycrystal vanished from the single crystal. This would be due to the thermal stress and/or the high enlargement rate as discussed by Bakin et al in Ref.[3].

In conclusion, the single crystal was successfully grown separated from polycrystal using a new type of crucible with an inner guide-tube. Consequently, the quality of the grown crystal was improved. High quality and large size bulk SiC is expected to be produced by the present method.

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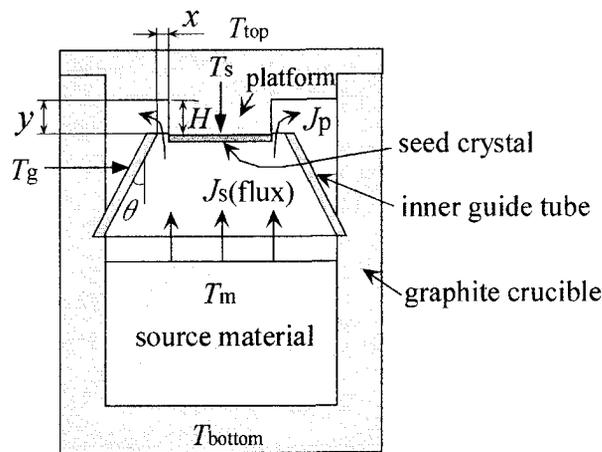


Fig.1 Schematic diagram of the growth crucible. The growth parameters are shown.

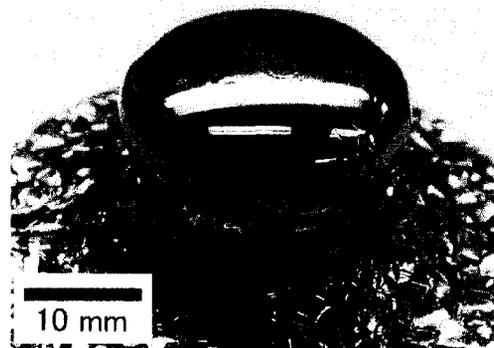
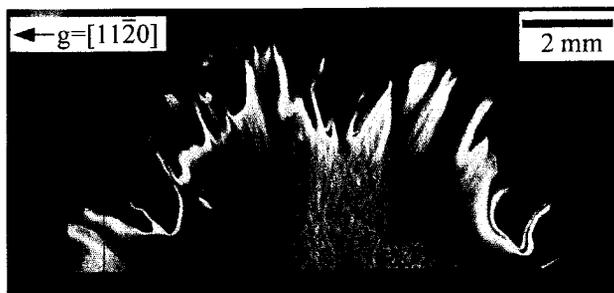
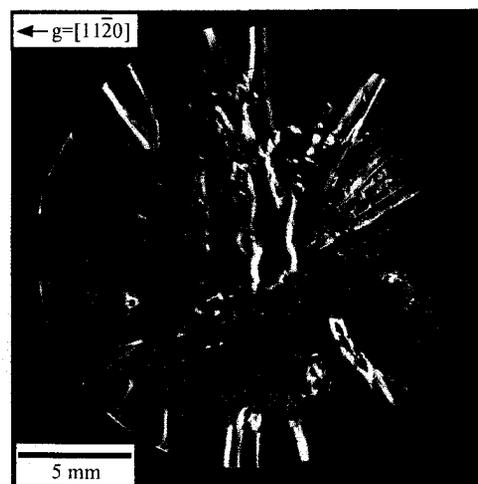


Fig.2 Photograph of the grown crystal.



(a)



(b)

Fig.3 X-ray topography images of the grown crystals. (a) grown with polycrystal by conventional crucible, (b) grown without polycrystal by the inner guide-tube.

Growth and evaluation of high quality SiC crystal by sublimation method

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Various defects which exist in a substrate are taken over to epitaxial film and they have a bad influence on electronics devices. [1] [2] Consequently the performance of electronic devices are not enough.

In order to reduce these defects, it needs to analyze them in detail and obtain a detailed information of these defects. However, as the conventional crystal made by the sublimation method of defect density was very high, their detailed information was not able to be obtained. In this study we grew the low defect density SiC crystal by the sublimation method, and we report the defect of the crystal.

The crystal was grown by the sublimation method that utilizes the lely crystal as a seed crystal. The source was polish abrasive powder of #240. The seed crystal and source powder was installed in the graphite crucible, and was overheated to 2200 degrees C. The atmosphere of growth system was argon at 13.3kPa. Growth was performed on Si-face. The optical microscope observation, X-ray topograph, and the etch pit observation by KOH etching were performed for the crystal evaluation.

The polarizing microscope photograph is shown in Fig. 1. The micro pipe could be confirmed by interference patterns observed by photoelastic measurements under the crossed polars condition. The sample shown in the photograph has contrast with the uniform whole surface, we don't observe interference pattern by photoelastic measurements. Hence this crystal does not have a large strain and there is no micro pipe.

The result of section topograph was shown in Fig.2. The direct image and dynamic image by defects was observed in the section topographic image. The direct image that is black point is mainly edge dislocation. And the dynamic image that is white diagonal line seems to be stacking fault. Pendellösung fringes is also observed. It means that the crystal quality is very high.

According to the etch pit observation by KOH etching, the etch pit density was $4 \times 10^3 \text{cm}^{-1}$ and there was no deviation in a distribution of etch pits.

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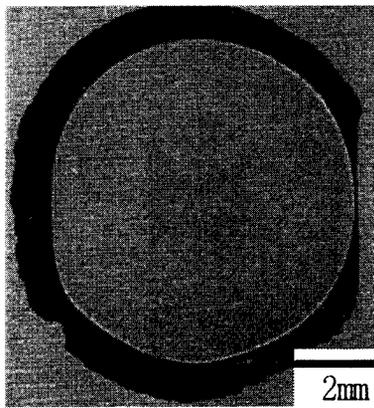


Fig.1 High quality SiC crystal of polarizing optical microscope image

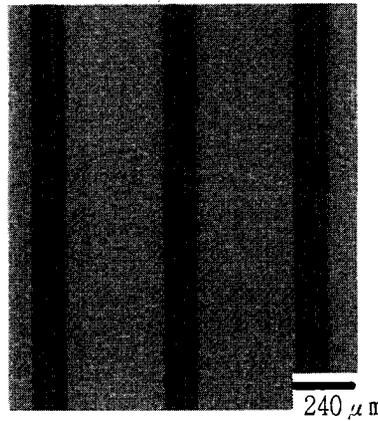


Fig.2 (11-20) Section topographs of SiC crystal by sublimation method. Mo $K\alpha$ radiation. Sample thickness of 270μm

REDUCTION OF MACRODEFECTS IN BULK SiC SINGLE CRYSTALS

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Keywords: bulk crystal growth, macrodefects, sublimation, crystal quality

Modern semiconductor industry yearns for Silicon Carbide (SiC) monocrystalline substrates because its unique electrical and thermal properties. SiC single crystal substrates are wanted for electronic devices (such as HF transistors, power rectifiers, high temperature sensors and controllers, etc), as well as for opto-electronics because SiC appears to have a very low mismatch of lattice parameters with basic active opto-electronic materials. It is common sense that an industrial scale SiC electronics starts as soon as market offers 4-inch diameter wafers with low defect density at reasonable price. Peculiarities (high temperatures, spatial and temporal instabilities of gas/vapor distribution, existence of porous graphite elements in growth zone, intricate temperature distribution in the growth chamber) of sublimation method of the crystal growth make this task at least very complicated one. To challenge this requirement Sterling has developed a proprietary technology that provides the feasibility to increase the grown boule diameter without deterioration by macrodefects. As far as the boule enlargement is concerned, a proper choice of a ratio between a vertical and radial components of the temperature gradient is critical to this process. Therefore the boule diameter has been realized through the development of proper technology for gradual increase of the grown crystal size and the design of a specific crystal growth chamber.

Macrodefects and imperfections in bulk SiC single crystal destroy the crystal quality. Crystal perfection is a critical issue for device performance, as in many applications the functional capability of the electronic device is limited by the size of the defect-free area. The aim is to eliminate or to reduce the defect density to the lowest possible level. Macrodefects include micropipes, low-angle-grain-boundaries, hexagonal voids, foreign material inclusions, and other attributes such as lattice/wafer bending originating from lattice distortion. It was observed that the defective portion of the crystal boule correlates strongly with quality of growth in the near-seed region. The seed attachment and treatment are factors playing the main roles in the defect generation. Therefore, the seed treatment, type of attachment of the seed, seem to be the crucial factors connected with effects taken place at the interface between the seed and seed attachment. Other factors having an impact on the increase of the defect-free region are the seed polarity (Si or C-face), seed quality, and source material. Methods of statistics and design of experiments were explored to clarify factors influencing the crystal quality. Now Sterling produces 2"-diameter SiC wafers with less than 7 micropipe/cm² without other macrodefects, and a radii of wafer lattice curvature exceeding 75 m. On its way to 4" diameter wafer commercial production, Sterling has demonstrated successful R&D growth of the single crystal boules of 92 mm diameter (See Fig. 1 as an example).



Fig. 1 Photo of Sterling's boule (after grinding)

Evolution of crystal mosaicity during physical vapor transport growth of SiC

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Recent reports on device degradation due to crystal mosaicity (domain structure) in SiC substrates have prompted interest in the origin and cause of crystal mosaicity in SiC crystals. The present authors revealed in the previous report [1] that the mosaicity originates in low angle grain boundaries existing in SiC crystals. Low angle grain boundaries are a critical defect which prevents the implementation of large-size ($\geq 1 \text{ cm}^2$) SiC devices. We have found that one of the major causes of low angle grain boundaries and the resulting mosaicity is the inclusion of foreign polytypes during growth [1]. The non-basal plane interfaces between the different polytypes accommodate crystallographic imperfections which relax into polygonized low angle grain boundaries during growth.

In this paper, an experimental investigation of the crystal mosaicity in SiC crystals grown by the physical vapor transport (PVT) method is presented. We investigate how the mosaicity in SiC crystals evolves during PVT growth. High resolution x-ray diffractometry (HRXRD) was employed to examine the relative misorientation between adjacent domains as well as elucidate the formation mechanism of crystal mosaicity in SiC crystals.

6H- and 4H-SiC crystals were grown along the [0001] and [11 $\bar{2}$ 0] directions by the PVT method, and the grown crystals were sliced into wafers having (0001), (1 $\bar{1}$ 00) and (11 $\bar{2}$ 0) orientations. HRXRD measurements were performed using a double-axis diffractometer, where a four-crystal monochromator was used for $\text{Cu}_{K\alpha 1}$ radiation. Analysis of x-ray rocking curves was used to quantitatively assess the lattice misorientation. In these experiments, the symmetric reflections of 0004, 0006, 11 $\bar{2}$ 0 and 3 $\bar{3}$ 00 in the rocking curves for 6H- and 4H-SiC crystals were acquired.

For the vertically sliced wafers along the growth direction, the incident plane was chosen either parallel or perpendicular to the growth direction. Analysis of such wafers showed that the domain structure was grown-in and originated in the seed crystal. We have examined polytype-mixed SiC crystals, *e.g.* 6H inclusions in 4H-SiC crystals. A series of rocking curves were measured from vertically sliced wafers from such crystals, where the shape and width of rocking curve varied for different diffraction scans along the growth direction. The rocking curves with the incident plane parallel to the growth direction showed a narrow single diffraction peak across the wafers, while the ones with the incident plane perpendicular to the growth direction exhibited a broader peak and often split into multiple peaks as the scans went far from the near seed polytype-mixed regions.

The polytypic inclusions would result in stresses due to the differences in the lattice constant and the coefficient of thermal expansion between different polytypes. During growth, the stresses are released by the introduction of dislocations, which are further activated to glide and climb in the crystals to minimize their total strain energy by aligning themselves along $\langle 1\bar{1}00 \rangle$, forming low angle grain boundaries.

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4H Polytype Grain Formation in PVT-grown 6H-SiC Ingots

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Recent progress in SiC sublimation growth technology based on the modified Lely method has spurred both a reduction of defect densities in SiC wafers and an enlargement of the wafer diameter. 4 inch-diameter 6H-SiC wafers have already been demonstrated, and remarkably smaller values of the micropipe density of the order of $<10\text{cm}^{-2}$ have been achieved for commercial 2 inch-SiC wafers [1]. A key for further development of device applications exploiting the attributes of SiC is to establish the control of optimum SiC growth with higher accuracy, which could be a path to larger SiC wafers of much improved crystal quality. In Nippon Steel Corporation, continuous challenges for fuller understanding of the growth mechanism have enabled us to accomplish the industrial production of SiC wafers with extremely low mosaicity over the whole wafer area [2], and further active R&Ds for the realisation of commercially-available 4 inch single crystal wafers are now underway.

Unwanted turbulence in optimum SiC growth still sometimes occurs, causing fatal failure in obtaining single crystal SiC ingots. A typical example of such flawed ingots is the multi-domained ingot in which large SiC grains are formed with their crystal directions strongly misoriented with regard to the SiC matrix. Similar multi-domained crystals have been reported by Tuominen *et al.* [3], suggesting that microcavities or micropipes created due to back-side evaporation could be responsible for such grain formation. Rost *et al.* [4] have pointed out another possibility that carbon inclusions could also cause the misoriented grains. Intense analyses of the multi-domained ingots we have obtained so far have been carried out in order to understand the generation mechanism of the misoriented grains, and the results obtained are presented in this paper.

Particular interest is to be addressed to our experimental fact that almost all the misoriented grains in the flawed 6H-SiC ingots we studied in this paper have the 4H polytype structure. Detailed analyses of the grains by means of X-ray pole figure measurements have suggested that the crystallographic direction of the grains has apparent correlation with that of the 6H-SiC matrix. Microstructural investigations have clarified that there exists a band region consisting of randomly-distributed fine SiC inclusions of around several tens μm in diameter. Raman analyses using a conventional Raman spectrometer are now underway for the detailed polytype identification of the inclusions. Although the formation mechanism is still in debate, we suggest that, upon the fact that the misoriented grains start from this band region, the inclusions observed are likely to be embryos of the misoriented grains, and some of which grow faster to become larger in the subsequent PVT growth.

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PVT Bulk Process Investigation: Experimental and Theoretical Approach

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Growth rate is one of the primary factors determining the crystal morphology and the density of defects in SiC crystals grown from vapor phase. It has been indicated [1] that there is an upper limit of the growth rate at which formation of inclusions, bubbles, veils, pipe-like channels, twinning and misoriented regions occurs in the growing boule of SiC. Therefore, defects in SiC are closely related to the growth rate value and the magnitude of temperature gradients in the crystal. Our experimental observations of SiC crystals grown by PVT technique show that majority of the defects listed above are located near (~2 mm) to the seed. As growth proceeds the defect density reduces. It has been found that the transition layer thickness reduces for a low axial temperature gradient condition. This resulted in the defect density reduction within the transition layer and SiC wafers production having micropipe density $<25/\text{cm}^2$. The analytical study presented here describes dynamics of the growth process at the initial stage of crystallization.

The source/seed temperature difference $\Delta T = (T_V - T_S)$ as well as the pressure in the system, are the main parameters that determine the growth rate via vapor flux intensity across the source/seed gap in the crucible (where T_V is the sublimation temperature of SiC source material and T_S is the temperature at the surface of growth). The mass conservation law applied to the total vapor flux is a fundamental relationship used for growth rate calculations: $dS/dt = \Omega \cdot F$ (Ω is the volume of SiC molecule; F is the total flux containing all the SiC vapor components [1,2]). However, the phase transformation heat released at the growth front and the heat radiated from the internal surface of the mass transport gap in the growth cell will also affect the dynamics of crystal growth. There is evidence [1] that inefficient heat dissipation in the growing crystal limits crystallization even at the initial stage of growth, when the crystal thickness is relatively small, $S(t) \approx 1.0$ mm. To maintain a necessary growth rate, an appropriate intensity of heat dissipation through the crystal volume must be ensured. In this case the Stefan's condition defines the correlation between heat balance at the surface of phase transformation and the appropriate growth rate: $\lambda \cdot \nabla T|_s = \Delta H \cdot \gamma \cdot dS/dt + Q$ (where λ is the thermal conductivity of SiC; $\nabla T|_s$ is the temperature gradient in the crystal; ΔH is the enthalpy of crystallization; γ is the density of SiC and $Q = Q_V + Q_W$ is the total amount of heat absorbed by the growing surface (Q_V – from the source top surface and Q_W – from the walls of the mass transport gap). Both these factors (vapor flux intensity and heat dissipation through the crystal) will simultaneously define self-consistent thermal conditions at the surface of phase transformation that determine dynamics of crystal growth during the entire time of the process.

To enable direct analytical analysis of the growth dynamics, dependent on mass (vapor) transport and heat dissipation, the rate of growth must be expressed in terms of mass/heat transport parameters. This can be done on the basis of a solution to the mass conservation and the

heat balance equations, resulting in an expression of the growth rate as a function of the instantaneous thickness of the growing crystal:

$$dS/dt = \Omega \cdot \theta \cdot \Delta T_G \cdot G(S), \quad (1)$$

where $G(S) = (1 - \mu \cdot S)/(1 + \eta \cdot S)$, $\mu = 2 \cdot \lambda \cdot Q_W / \Delta T_G \cdot (\pi)^{1/2}$ and $\eta = 2 \cdot \lambda \cdot (Q_V + \Delta H \cdot \gamma \cdot \Omega \cdot \theta) / (\pi)^{1/2}$. The μ and η parameters determine the maximal possible thickness of the crystal and the dynamics of growth; $\Delta T_G = (T_V - T_C)$ is the temperature difference between source and backside of the crystal; $\theta \approx P_V \cdot W / R \cdot T^2 \cdot \beta$, where P_V is equilibrium pressure in the crucible at the temperature of sublimation T_V , W is the activation energy of SiC sublimation [3], R is the universal gas constant, T is the average temperature in the crucible; $\beta = \Delta T / R_D$, R_D is the diffusive resistance of the growth cell. As is clear from (1), the growth rate has its maximal value at the initial stage of growth that is determined only by mass transportation conditions $dS/dt \approx \Omega \cdot \theta \cdot \Delta T_G$, ($T_S = T_C$ at $S \approx 0$). Further, the growth rate decreases with increasing crystal thickness, approaching zero when $\mu \cdot S \sim 1$. Furthermore according to (1), the maximal thickness of SiC crystal, which is possible to obtain at a given thermal condition, is proportional to the temperature difference in the crucible, ΔT_G : $S_M \approx \Delta T_G \cdot (\pi)^{1/2} / 2 \cdot \lambda \cdot Q_W$. The dynamics of growth rate variations is mostly determined by the dimensionless parameter $\eta = 2 \cdot \lambda \cdot (Q_V + \Delta H \cdot \gamma \cdot \Omega \cdot \theta) / (\pi)^{1/2}$. As follows from this formula the parameter η is the function of the vapor flux intensity, $\Omega \cdot \theta$. Hence the vapor flux intensity does not have a significant influence on the growth rate dS/dt , and the influence of heat dissipation becomes dominant, when the crystal thickness is sufficiently large. If during a growth processes the temperature difference ΔT_G is maintained constant (the source temperature T_V as well as the crystal backside temperature T_C are strictly controlled), the temperature at the surface of phase transformation will asymptotically approach the temperature of sublimation:

$$T_S(S) = T_V - \Delta T_G \cdot G(S). \quad (2)$$

The growth rate can be stabilized at a given value V_0 for any crystal thickness by tailoring the temperature (heat dissipation) at the crystal backside. As it follows, the temperature difference $\Delta T_G(S)$, stabilizing the rate of growth, is a linear function of crystal thickness:

$$\Delta T_G(S) = V_0 / \chi + ((V_0 / \chi) \cdot \eta + \omega) \cdot S, \quad (3)$$

where $\chi = \Omega \cdot \theta$ and $\omega = 2 \cdot \lambda \cdot Q_W / (\pi)^{1/2}$. As can be seen from (3), the latent heat of crystallization becomes dominant and defines the heat balance conditions at the growth surface when the rate of growth is sufficiently high $((V_0 / \chi) \cdot \eta \gg \omega)$.

As a result of the increasing temperature difference ΔT_G , one can expect corresponding increase of thermal stresses in the growing crystal. A 2-D analysis showed that the axial temperature distribution is almost linear, and has no significant influence on the formation of thermal stress in the crystal. However the radial temperature gradient is a primary factor in the development of thermal stress that can lead to generation of dislocations in the crystal volume if the stress exceeds $\sigma_{CRS} \approx 1$ Mpa, which is the critical resolved shear stress in SiC.

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Resistivity Mapping of Semi-insulating 6H-SiC Wafers

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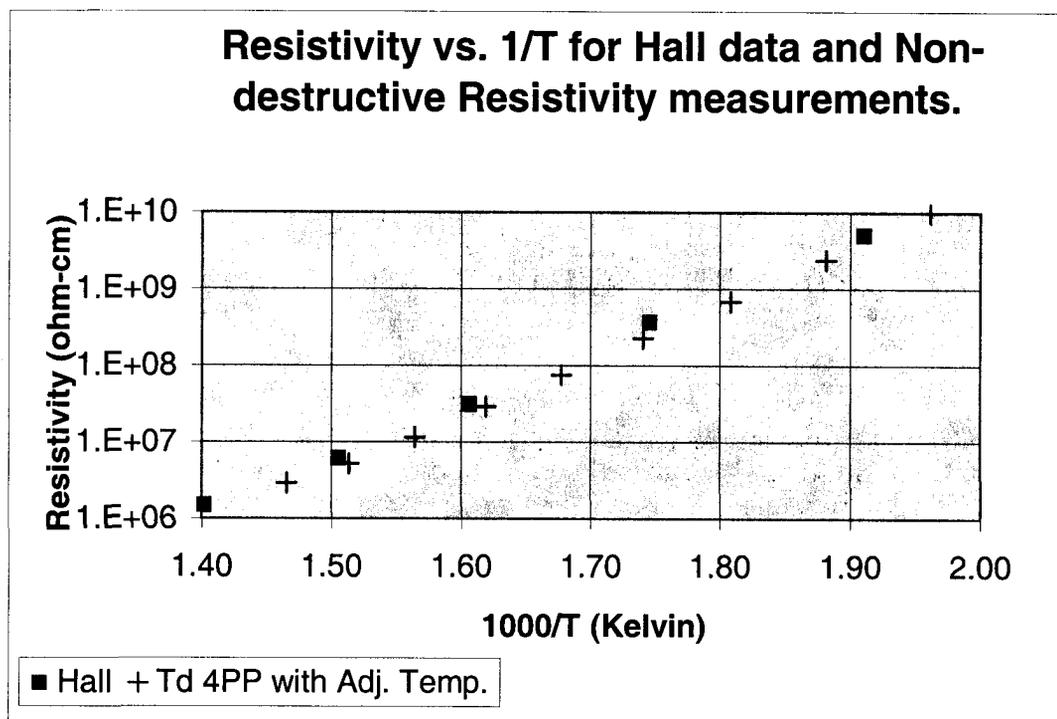
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Abstract. Semi-Insulating 6H-SiC wafers with room temperature resistivity data from 10^6 ohm-cm to 10^9 ohm-cm and greater are compared with Hall effect measurements. The transport data observed by Hall effect are compared to multi-point non-destructive resistivity maps of semi-insulating wafers. A high degree of agreement is obtained from non-destructive resistivity measurements and Hall effect measurements on corresponding regions. The spatial distribution and nature of the high resistivity behavior are also discussed.



Polytype Control in Sublimation Growth of 4H-SiC Single Crystals

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Among the common SiC polytypes, 4H-SiC is desirable for fabrication of high power and high temperature semiconductor devices. Commercially available 4H-SiC crystals are grown by using the sublimation physical vapor transport technique. In sublimation growth of SiC, 6H is generally believed to be the most stable polytype and 4H-SiC crystals grown under certain growth conditions were observed to have 6H or 15R inclusions. These polytype inclusions in 4H-SiC crystals are believed to be responsible for generating defects, particularly micropipes, in the crystals and therefore they should be eliminated.

Several recent studies on control of 4H formation were published in the literature [1, 2]. Since each study was done in a somewhat unique sublimation growth environment, a detailed investigation of our own 4H sublimation growth process will provide further information leading to a better understanding of 4H polytype formation. In this investigation, we examined the influence of several growth parameters on the formation of 6H and 15R polytype inclusions in the sublimation growths that were intended to produce 4H-SiC crystals. Among the growth parameters, temperature, pressure and thermal gradient were studied extensively. 6H and 4H seeds of on-axis and off-axis types were used in the study. One focus of this study was on the effectiveness of the use of 4H seeds with off-axis angles up to 8° to control the formation of 4H at the seed/newly-grown-crystal interface regions in a way similar to the step-flow mechanism that is used widely in CVD epitaxial growth of 4H thin films on 4H SiC wafers. To avoid the interference of impurities with the growth parameters under study, ultra-high purity SiC source materials, as well as graphite parts, were used in all the sublimation growth experiments. The sample SiC boules were sliced both parallel and perpendicular to the growth axis for characterization. The SiC boules under study were n-type doped with nitrogen at concentrations of approximately 5×10^{18} atm/cm³. In SiC crystals with such high nitrogen doping concentrations, all three major polytypes, i.e. 4H, 6H and 15R, in the crystals can be identified by examination under an optical microscope because these polytypes appear in distinctively different colors. X-ray transmission Laue diffraction technique was also used for the identification of polytype inclusions in the SiC samples.

Our experimental results suggested that, among the major growth parameters, the growth temperature played the most important role. Under the growth conditions in this study, lowering growth temperature favored the formation of 4H and increasing growth temperature favored the formation of 6H, while within a range of growth temperatures, 4H, 6H and 15R mixed polytypes were frequently observed, particularly at seed/crystal

interfaces. When on-axis seeds were used, 4H seeds seemed to help stabilize 4H polytype better than 6H seeds. On the other hand, under the growth conditions that favored 4H growth for on-axis seeds, using 4H off-axis seeds essentially guaranteed a uniform 4H to 4H growth at the seed/crystal interfaces. In figure 1, two optical micrographs of 4H wafers containing the seed/crystal interfaces were shown where (a) the existence and (b) the absence of 6H/15R inclusions in 4H crystals were demonstrated. Based on the results of the current study, 4H off-axis seeds should be used in order to achieve a uniform 4H-to-4H growth at the seed/crystal interface.

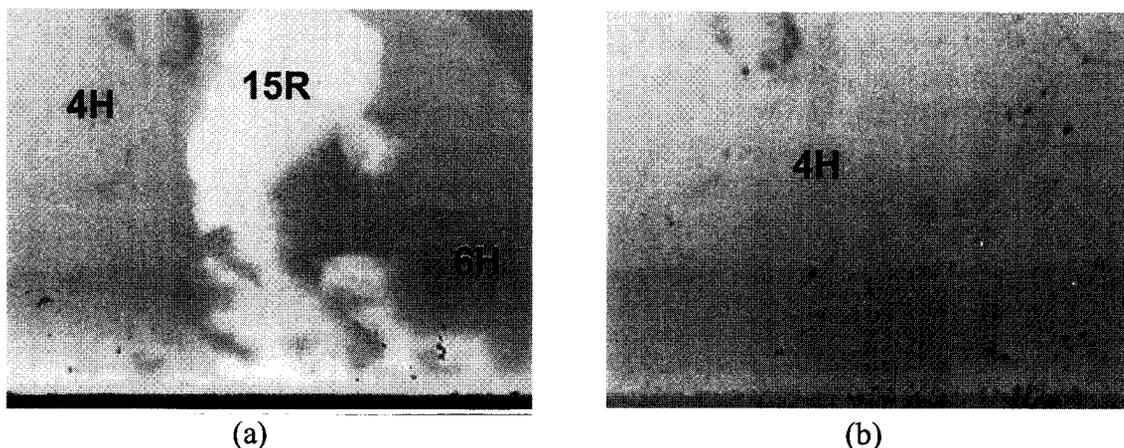


Figure 1. Optical micrographs of 4H wafers containing the seed/crystal interfaces show that (a) the existence and (b) the absence of 6H/15R inclusions.

Details of the sublimation growth and polytype characterization results will be presented and crystal defects, such as micropipes and grain boundaries, in the 4H-SiC crystals under study will also be analyzed and discussed.

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Model for Macroscopic Slits in 6H- and 4H-SiC Single Crystals

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Abstract

The development of defects in SiC bulk crystals at the MLM growth is often caused by too large axial temperature gradients in the growing crystal. The axial temperature gradient can be decreased by optimisation of the graphite crucible or by changing the position of the induction coil.

Additionally, a smaller seed temperature has the same effect, because the radiation heat loss at the backside of the seed holder is proportionally T^4 . Furthermore, 4H should grow more stable at lower temperatures.

This temperature influence was used for the growth of 6H and 4H single crystals under stable conditions. The single crystals were grown with 30-36 mm in diameter and a micropipe density between 50-200 cm^2 . A short-time nitrogen doping marked different growth sections. The seed temperature was varied between 2050°C and 2250°C. The seed polytype was selected corresponding to the wanted polytype and cutted with 3.5° off for 6H and 8° for 4H to $\langle 11\bar{2}0 \rangle$ orientation. To ensure the polytype stability the C-terminated surface was used for 4H-crystals. 6H-crystals could generally be grown on both sides although a higher polytype stability on the Si-terminated surface was observed.

The investigations of wafers and axial slices were realized by means of microscopy in polarised light, photoluminescence at room temperature, and Scanning Electron Microscopy (SEM).

Decreasing the seed temperature macroscopic slits will be developed in growth direction (fig.1,2). The lateral extension is orientated preferentially in $\langle 1\bar{1}00 \rangle$ - and $\langle 11\bar{2}0 \rangle$ -directions.

The origin for such defects can be localized at other defects extended nearly perpendicular to the growth direction. Examples for such source defects are lamellas of other polytypes (15R) and a new kind of macropipes which are oriented vertical to the growth direction.

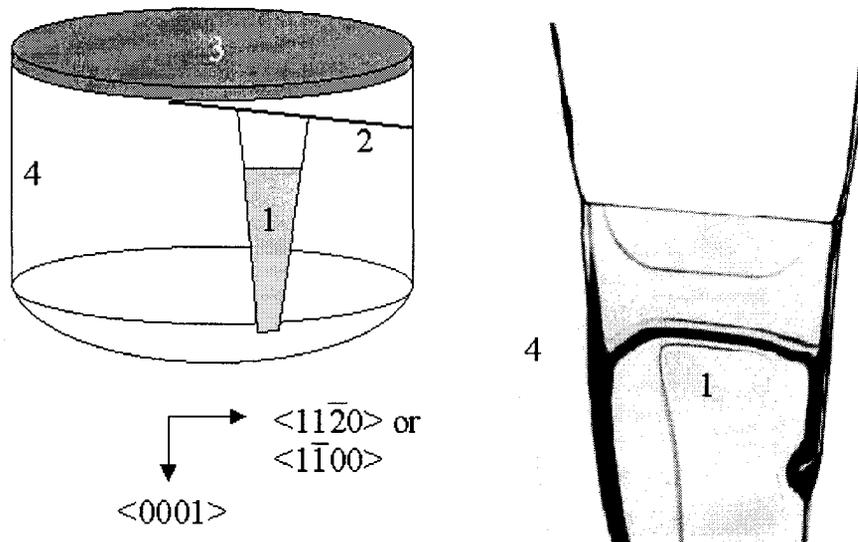


Fig.1: Sketch and micrograph of a macroscopic slit in SiC-crystals; 1- macroscopic slit, 2- needle like inclusion (15R), 3- seed, 4- bulk

As a first attempt of explanation the influence of the mechanically induced stress field on the supersaturation can be used. In accordance with the argumentation in [1] a step train can be blocked by a stress field elongated parallel or almost parallel to the surface. Following growth steps cannot enter this step bunching like region. A stable slit is formed. Then a „Schwoebel effect“ is responsible for the stable enlargement also in the growth direction [2]. Typically the size of slits is 3-100 μ m in width and 2mm up to 15mm in length. This geometry shows a good accordance with the theoretical considerations.

The main responsibility of polytype changes for the formation of the macroscopic slits is shown when polytype changes are prevented by increasing the seed temperature or other measures. Macroscopic slits are quite rare under such conditions.

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Nucleation-induced stacking faults in PVT SiC layers grown on (0001) Lely seedsJ. Q. Liu, E. K. Sanchez, and M. SkowronskiDepartment of Materials Science and Engineering, Carnegie Mellon University,
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The structure of seed/crystal interfaces has been investigated by conventional and high resolution transmission electron microscopy (TEM). 6H-SiC layers have been deposited by Physical Vapor Transport method on high quality on- and off-orientation Lely seeds. Growth experiments have been performed between 2200 and 2300 °C with 20 °C/cm axial temperature gradient and argon pressure between 10 and 500 Torr. The seed surfaces have been etched in hydrogen in order to remove the residual damage due to seed surface polishing. Screw dislocation free Lely platelets have been carefully selected in order to eliminate step sources on the seed surface and force growth by two dimensional island nucleation.

Cross-sectional TEM of seed/layer interface revealed presence of a band of stacking faults (Fig. 1) with thickness between 1 and 20 μm . The total number of faults in the band was between 2 to 100. The stacking sequences of the faulted band have been analyzed by high resolution TEM as a function of growth conditions. With the increasing growth rate and the silicon overpressure, the probability of cubic stacking is increasing. Bands of up to 6 bilayers with the cubic stacking were observed. This stacking disorder was interpreted as due to low stacking fault energy in SiC polytypes and 2D island nucleation on step free seed surface.

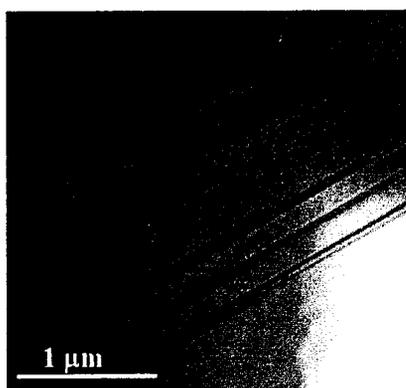


Fig. 1 Stacking faults observed by TEM at the Lely seed-crystal interface.

After island coalescence, different stacking sequences in neighboring islands are accommodated in the form of partial dislocations with the dislocation line in the basal plane. Existence of both Shockley and Frank partial dislocations has been inferred from the analysis of stacking sequences. A model of threading edge and screw dislocation nucleation associated with the presence of stacking faults along the interface is proposed.

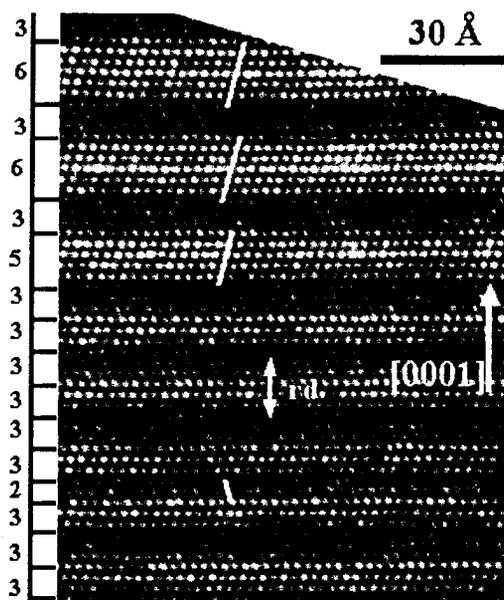


Fig. 2 High resolution TEM image showing stacking disorder during 2D SiC growth.

Solid phase epitaxial growth of different polytypes of bulk single SiC crystals

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Introduction

Physical Vaport Transport (PVT), Liquid Phase Epitaxy (LPE) and High Temperature Chemical Vapor Deposition (HTCVD) are the main reported growth techniques for the fabrication of bulk SiC single crystals. More recently, solid phase epitaxy has proved its potential to process high quality bulk 6H-SiC bulk crystals [1].

In this paper, the solid phase epitaxial growth of different SiC polytypes is described and discussed.

A single crystal seed of 35 mm in diameter and a 50 mm polycrystalline 3C-SiC wafer were mirror-polished and firmly assembled. Seeds of different polytypes has been used. The solid phase epitaxial growth was conducted in a graphite crucible heated at high temperature (2600 K) and for an argon pressure of 400 Pa. SiC powder surrounds the crucible chamber. A thin wall of porous graphite separates the chamber from the powder. The other parts of the reactor were kept identical as in our sublimation reactor [2]. In figure 1, the thermal fields in the standard reactor used for PVT and the modified reactor for SPE are shown.

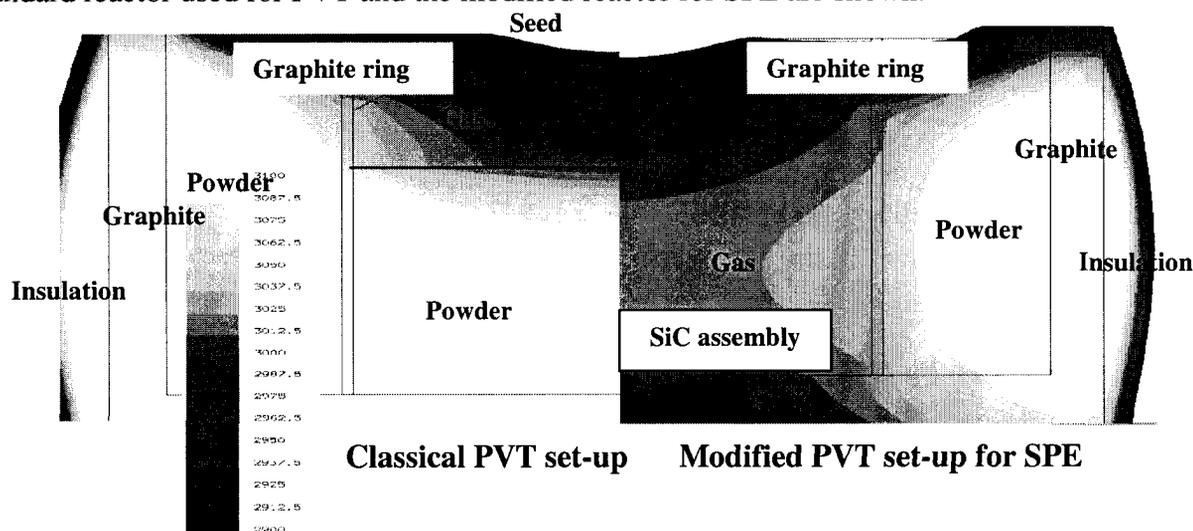


Figure 1 : Thermal fields in the PVT reactor (right) and in the modified reactor for SPE (left).

Results and discussion

The results show that solid phase epitaxy has been effective for the growth of bulk single crystals. The epitaxial alignment of the polycrystalline 3C wafer in the polytype of the seed

can be induced in the temperature and temperature gradient fields depicted in figure 1 and in an ambiance containing Ar, Si₂C, SiC₂ and Si.

Milita et al. [3] have already analyzed by X-Ray synchrotron topography the solid phase epitaxy process. In the classical PVT seeded technique, the SiC crystal growth occurs in two distinct region. In its core, there is the main crystal which is of high crystalline quality and grows directly above the seed. Around the main crystal, on the graphite lid, grows at first small misoriented crystallites. The crystallites with a common axis and similar in orientation to the main crystal grow faster at the expense of the randomly growing crystallites, which finally disappear. The correlated crystallites finally are integrated into the main crystal. This in situ solid phase epitaxy allows the enlargement of the growing crystal. This phenomenon is the driving force for the SPE process.

Conclusions

We have shown that the recrystallization of polycrystalline 3C-SiC wafers can be induced from single SiC crystal seeds by a solid phase transformation at temperatures above 2300 K and in an ambiance containing Si- and C- gaseous species. The rate of transformation is about 300 μm/h. If the annealing time is prolonged, the crystal quality of the grown crystal improves and the resulting epitaxial layer contained only a small amount of crystallographic defects.

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Dislocation constraint by etch back process of seed crystal in the SiC bulk crystal growth

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In this study, we report on the dislocation and defects constraint in the initial SiC growth using the etch back process by the modified Lely method. The seed crystals for the growth were prepared by three kinds of 6H-SiC crystals. One is the as-grown crystal with 3mm thickness developed by the Lely method, which has a shell like shape composed of (0001) plane and hexangular pyramidal planes. Others are (0001) plate crystals with 0.5~7mm thickness grown by the Lely and the modified Lely methods. The seed was fixed on the lid ($\phi 10 \times 5$ mm) projected from the top to the inside of the carbon crucible, and the raw material of the SiC powder was filled in the bottom. In this structure, the seed crystal more than 2mm thick initially is etched back soon after reaching the general growth condition in the crucible. The turning from the pre-growth etch back to the growth could be performed without changing heating condition of the crucible. This process has been performed for optimizing the surface condition on the seed crystal and effected on the dislocation and defects constraint in the initial growth. Possible reasons of the etching mechanism and the defects constraint will be discussed in the session.

Fig. 1 is an X-ray topograph obtained with $g=11\bar{2}0$ from the sectional specimen of the SiC crystal grown by the modified Lely method on a (0001) Lely plate seed crystal with 0.5mm thick. As the seed crystal is less than 2mm thick, the pre-growth etch back process could not be performed in this case. The crystal quality of the Lely seed crystal seems to be perfect, however, an intense broad line (A) on the interface between the seed and the grown crystal and many fine lines (B) elongated along the growth direction from the seed surface can be observed. (A) shows that the grown crystal layer is distorted by the high density of dislocation [1]. On the other hand, (B) shows strain fields from line defects such as micropipes and screw dislocations. It seems that the high density of dislocations are connecting each other during the growth, and release stress as a result of their combination. If the stress is released imperfectly, the dislocations appear like a line defect of micropipes and/or screw dislocations, which is considered as one of the reasons for defects generation in the modified Lely crystals.

The second SiC growth was performed on the as-grown Lely seed crystal. Fig. 2 is an optical micrograph obtained from the sectional specimen of the grown crystal, which contains both images of the seed crystal and the grown crystal. The figure shows that the grown crystal has no micropipe. The top part of the crystal in Region α was sublimed and was etched back before the start of the growth, the height of the seed crystal was decreased from 3mm to 2mm till the dome like shape. This etch back was automatically switched over to the growth. On the other hand, the Region β is the grown area on the unetched surface that is original surface of hexangular pyramidal planes of the as-grown Lely seed crystal. Therefore, before the start of the growth, the top surface first converts to the dome like shape drawn by dots line of L in the

schematic figure, and then the crystal became thicker with the further growth. Fig. 3 is its x-ray topographs obtained with $g=11\bar{2}0$. The high density of dislocation is only observed between the unetched surface of the seed crystal and the grown crystal (Region β). Moreover, many line defects are propagated from there. However, the grown crystal on the etched top of the seed crystal shows no high density of dislocation and low line defects (Region α). It seems that the pre-growth etched surface of the seed crystal is effective to restrain of defect propagation in the SiC crystal growth.

When the pre-growth etch back process was performed for the seed crystals prepared from modified Lely crystals, we succeeded to constrain not only the high density of dislocation but also micropipes. This interesting phenomenon could be found in the interface between the seed crystal and the grown crystal from the observation using optical microscope as shown in Fig.4. We observed that many micropipes terminate just below the interface, which is the first observation in the SiC crystal growth by the modified Lely method. The density of the micropipes in the grown crystal decreases to about 1/10 comparing with the seed crystal.

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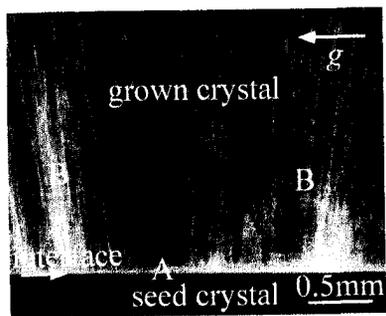


Fig. 1 X-ray topograph of the SiC crystal grown in the (0001) Lely plate crystal.

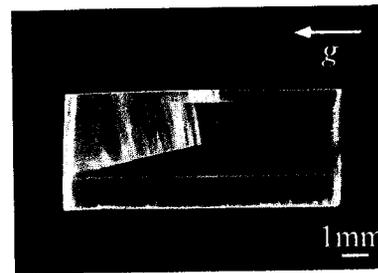


Fig. 3 X-ray topograph obtained with $g=11\bar{2}0$ from the same specimen observed in Fig. 2.

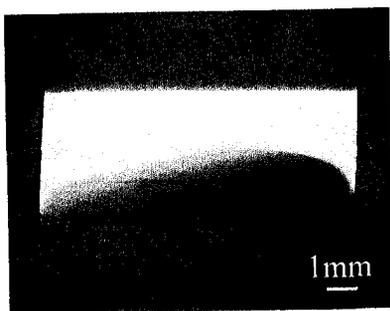


Fig. 2 Optical micrograph obtained of the SiC crystal grown on the as-grown Lely seed crystal.

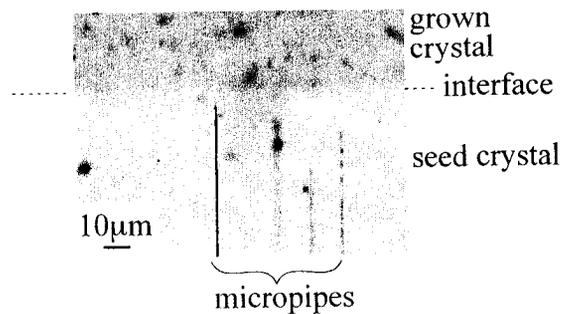


Fig. 4 Optical micrograph showing several terminated micropipes in the interface region between the seed crystal and the grown crystal.

The Nucleation of Polytype Inclusions During the Sublimation Growth of 6H and 4H Silicon Carbide

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Silicon carbide (SiC) possesses a host of electrical and physical properties that make it ideally suited for use in high temperature, high frequency, and high power devices. One of the most interesting properties of SiC is that it can take the form of over 200 different polytypes, a one-dimensional version of polymorphism. Each polytype has a set of electrical and physical properties that is unique. Therefore, controlling the formation of different polytypes is a key ingredient in controlling the properties of SiC devices. Recent progress in the physical vapor transport (PVT) growth of silicon carbide crystals has resulted in single crystal wafers of the two most common polytypes, 4H and 6H, up to 100 mm in diameter [1]. However, the nucleation, or switching of different polytypes during PVT growth is still not understood and has been shown to result in the formation of micropipes and dislocations in SiC crystals. [2].

In this study, polytype nucleation during the growth of both 6H and 4H single crystal SiC was investigated. The polytype inclusion's morphologies were examined and related to growth conditions. It was observed that polytype inclusions nucleate at the outer edge of the central growth facet. They then propagate along the a-direction toward the edge of the wafer in a fan like band. Cross-sectional investigation showed that these polytype inclusions were arranged in bands of c-planes, which originate at a single point on one c-plane, see figure 1. The inclusions were observed to then grow outward along the c-plane and upward along the c-direction. Investigation of the nucleation point revealed the existence of voids or inclusions of an as yet unknown origin. The existence of these voids and their possible relevance to polytype inclusions will be discussed, along with an explanation of what may be occurring at the growth surface during polytype switching.

It was also observed that the polytype inclusions have a devastating effect on the crystal quality. In particular, the nucleation of polytype inclusions was linked to the nucleation of micropipes. The boundaries between different polytypes are aligned with micropipes, suggesting that the inclusions were a nucleation point for these micropipes. In cross-section, the micropipes were indeed observed to originate on the c-plane where the polytype changed, see figure 1. The micropipes were also seen to bend at different angles when propagating through different polytypes. An explanation of this observation is presented and its possible relevance to the polytype nucleation discussed.

A detailed investigation of the PVT growth of both 4H and 6H SiC will be presented to explain the formation mechanisms involved in polytype inclusion nucleation, based on the morphologies, growth conditions and experimental evidence obtained during PVT growth.

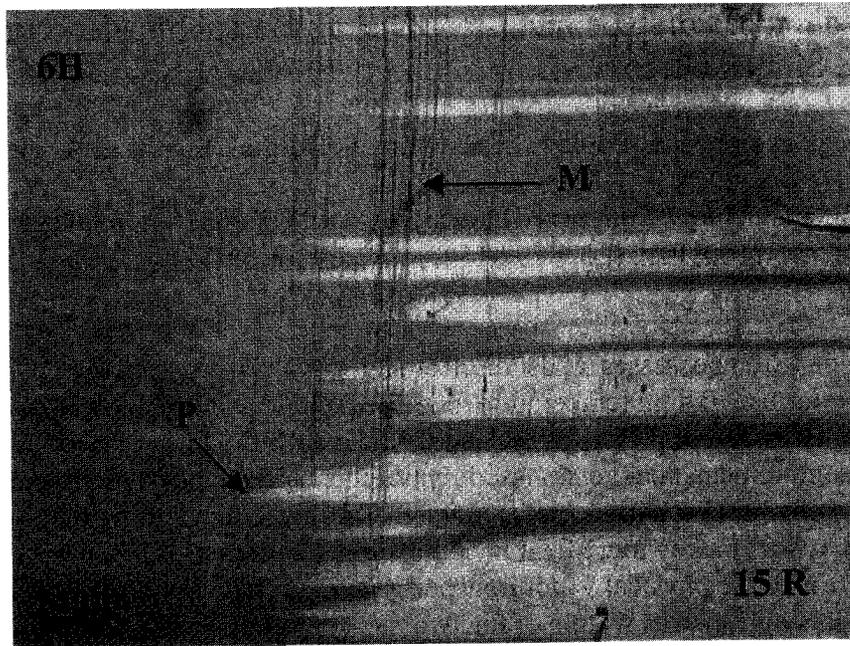


Figure 1 - Optical transmission image of a 6H SiC boule with 15R inclusions. The polytype inclusions all start at a point (such as the one labeled P) at the edge of the central growth facet. Micropipes (labeled M) can be seen originating at the polytype nucleation point and propagating into the growth.

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Aluminum Doping of 6H and 4H SiC with a modified PVT Growth Method

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Aluminum doping of SiC single crystals with powder source results in an exponential axial decrease in charge carrier concentration caused by aluminum source depletion and defect generation through high initial aluminum concentrations [1]. Therefore we applied an additional gas flow to the PVT-Growth-Setup leading directly into the growth cell [2]. Thus a continuous supply of aluminum atoms out of an external reservoir was possible. The concept will be discussed.

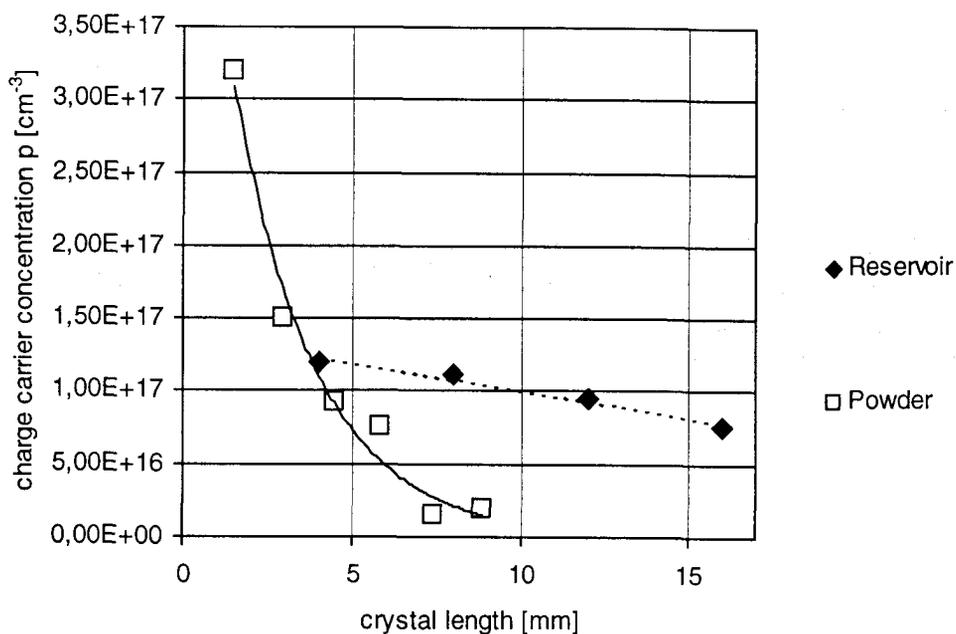


Fig.1: Axial charge carrier distribution (Hall measurement) in 6H-SiC-crystals grown on the Si-side with aluminum in the powder (white squares) and with external source (black rhombuses).

With the Modified-PVT-Method high quality crystals with improved axial (4H: $2 \cdot 10^{16} \text{ cm}^{-3} < p < 4 \cdot 10^{16} \text{ cm}^{-3}$; 6H: $8 \cdot 10^{16} \text{ cm}^{-3} < p < 1,2 \cdot 10^{17} \text{ cm}^{-3}$, Fig. 1) and lateral (4H: $\Delta p/p < 10\%$; 6H: $\Delta p/p < 25\%$, Fig. 2) charge carrier homogeneity were grown.

The Dependence of the remaining doping variations on compensation with residual nitrogen and growth mechanisms and measures for further improvement will be discussed.

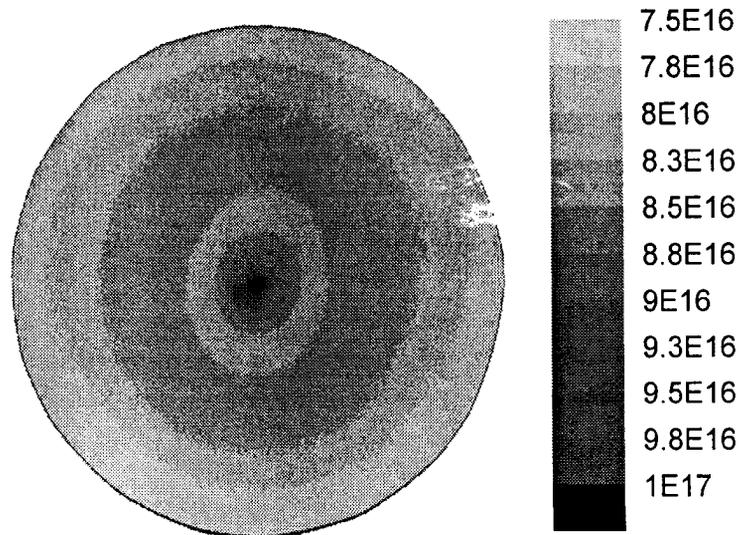


Fig.2: Absorption mapping of a 6H wafer with monochromatic light of 570 nm [3]. The bright parts indicate areas with low charge carrier concentration. Units: cm^{-3} .

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Macro Defect Generation in SiC Single Crystals Caused by Polytype Changes

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The generation of macroscopic defects like radial cracks [1] was discussed in terms of stress induced micropipe formation and agglomeration. Low angle grain boundaries (frequently referred to as domains up to some millimetres in length are visible as linear features extending radial inward from the wafer edge and generally following low-index crystal planes. They may sometimes extend through the entire wafer thickness [2]. Recently, the domain structure was attributed to the polygonization of threading edge dislocations, resulting in a low angle tilt boundary array [3].

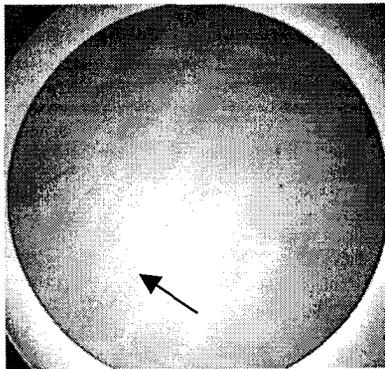


Fig.1
Extended slits perpendicular to
the basal plane
(wafer diameter 32mm)

Another category of grown-in type macro defects will be discussed in this paper. They can be described as slits bordered by two walls with a linear extension up to some millimetres and a distance between them in the micrometer range (Fig.1). The slits are extended in the basal plane, preferentially in $\langle 1\bar{1}00 \rangle$ respectively $\langle 11\bar{2}0 \rangle$ direction, and are running in a plane parallel to the growth direction. They are often bordered by micropipes [4]. In dependence on the growth conditions the slits are stabilised and may penetrate the whole crystal or disappear.

Single crystals of the 4H- and 6H-polytype with diameters up to 35mm and micropipe densities between 50 and 200 cm^{-2} were grown in a temperature range from 2100°C to 2250°C. Seeds with 3.5° (6H) respectively 8° (4H) off-orientation to $\langle 11\bar{2}0 \rangle$ were used. For 4H-crystals only the C-terminated surface was considered. Crystals were nitrogen doped with concentrations from 7×10^{16} - 10^{19} cm^{-3} . The defect evolution within the crystals was investigated using Optical Microscopy, Scanning Electron Microscopy (SEM), Electron Beam Induced Current (EBIC) and KOH-etching methods.

EBIC images revealed that bundles of preferentially basal dislocations are located between isolated slits (Fig 2) and are assumed to be responsible for the slit generation across a long distance in the basal plane as well as in regions below the starting point of the slits (Fig.3). Under certain conditions the induced dislocation bundles may prevent the growth of material above it resulting in a slit. Their existence itself is strongly correlated to the presence of polytype changes. Therefore, the deterioration of the crystal perfection at the polytype borders seems to be the origin of the slit generation, which is especially observed during the growth of 4H-crystals. Polytype stabilising parameters, useful to suppress the generation of the described defects, will be discussed.

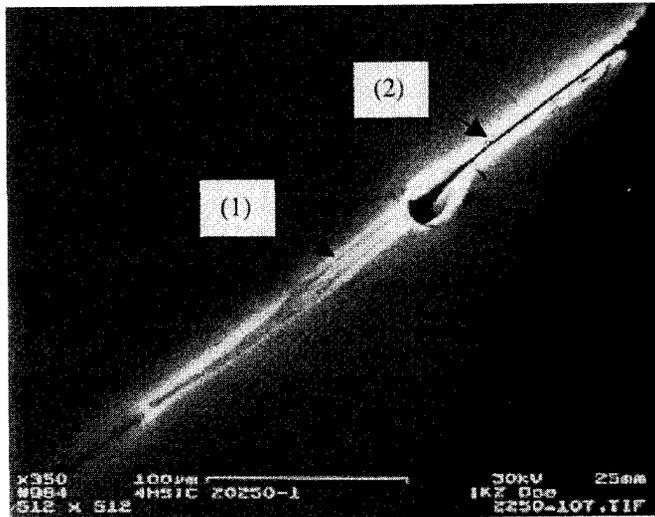


Fig. 2 Dislocation bundle (1) associated with a slit (2) (basal plane), EBIC

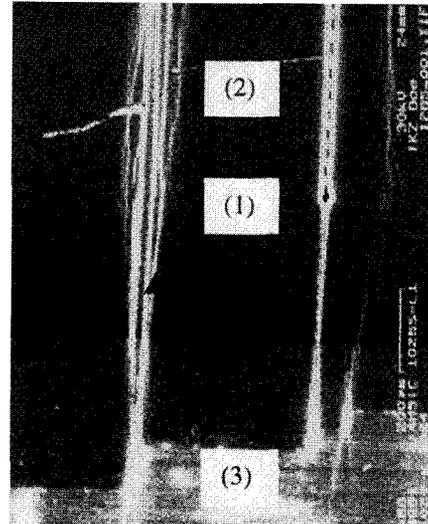


Fig.3 Dislocation bundles (1) below the slit (2) starting at steps of polytype lamellas (3), (EBIC) (growth direction upwards)

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Chemical vapor deposition growth and characterization of shape memory SiC nanorods

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Nano-sized SiC structures are useful for the improvement of mechanical and thermal properties of nanocomposite materials due to their high strength, high elastic modulus, low density, high thermal and chemical stability. The large bandgap property of SiC also enables SiC nanostructures to be potentially applicable for nanoelectronic and nanophotonic devices designed to operate at high temperature, high frequency, etc [1-3].

In this work, we report a shape memory synthesis of SiC nanoscale structures at lower temperature. Our technique consists of the growth of carbon nanotube over Fe-Co catalyst loaded SiC wafer and the subsequent growth of SiC nanorods by a chemical reaction of CNT with TMS in a rapid thermal chemical vapor deposition (RTCVD). The Fe-Co catalyst was supported on an ultrasonic cleaned Si(100) wafer by dipping into aqueous solution (10^{-3} M) of corresponding metal salts ($\text{Fe}(\text{NO}_3)_3 \cdot 9\text{H}_2\text{O} : \text{Co}(\text{NO}_3)_2 \cdot 6\text{H}_2\text{O} = 1 : 1$). After Fe-Co supported Si wafer was washed with DI water, it was dried in an oven at 100°C for 1 h. For the growth of CNT, the metal loaded substrate was placed in the base area of a quartz plate and fixed in the central hot region of a RTCVD reactor [4]. The grown CNTs was insitu etched for 5 min by 200 sccm H_2 gas at 900°C and the growth of SiC was performed for 30 min over the CNT at 1100°C with 1.0/200 sccm TMS/ H_2 . The structural and optical properties were investigated using various analytic techniques.

Figure 1 shows SEM images of the grown SiC nanostructures. The figure reveals the growth of large quantities of straight and curved nanorods across the whole substrate surface. The nanorods with approximately $1 \mu\text{m}$ length are randomly oriented over CNT grown for 1 min (Fig. 1(a)). However, the length of SiC nanorods significantly increases as the growth time of CNTs increases (Fig. 1(b)). IR spectra for both the samples showed a strong C-Si stretching vibration absorption peak at 805cm^{-1} , which confirms the growth of SiC. The appearance of a XRD peak at $2\theta = 17.5^\circ$ also indicates the growth of the zinc blend β -SiC nanorodes [1,5]. The intensity of the SiC peak at

$2\theta = 17.5^\circ$ increased with the growth time.

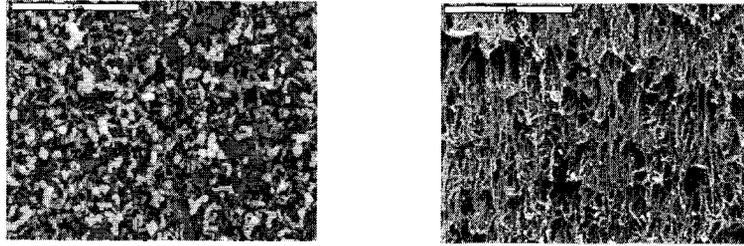


Fig. 1: SEM images for SiC nanorodes; (a) CNTs grown for 1 min. (b) CNTs grown for 10 min.

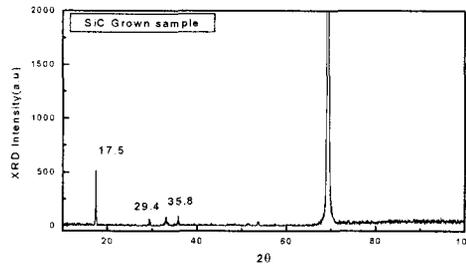


Fig.2: XRD spectrum for SiC.

We have also investigated the temperature effect on SiC growth. No evidence of the growth of the SiC nanorodes was found from the samples grown at 900 and 1000⁰C, respectively. The presence of a sharp peak at 950cm⁻¹ in the Raman spectrum recognized the LO mode of the SiC lattice [6]. The intensity of the Raman peak at 950cm⁻¹ increases as the relative growth time of SiC increases, indicating that SiC nanorods are formed by the conversion of CNTs into SiC. EDX was also showed the stoichiometric growth of SiC nanorods. PL peak was observed at an emission energy of 2.3 eV, indicating the growth of the SiC nanorods [6].

Acknowledgements

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OPTIMIZATION OF INTERFACE AND INTER-PHASE SYSTEMS : THE CASE OF SiC AND III-V NITRIDES

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Modern crystal-growth techniques can now afford a wide panoply of heterosystems for applied physics purposes. A comprehensive understanding of the problems involved in growth experiments implies the macroscopic and microscopic aspects of interface physics. Although the latter aspect is relevant to the very first stages of the growth process, the first aspect (of heteroepitaxy) must be taken into account because not only local features but also periodic and long-range features can influence the process. This is for example the case of Lomer dislocations which may be created at the interface between two host materials with mismatched lattice parameters when the overlayer thickness exceeds a critical value. An energy balance between strain-associated elastic energy and dislocation formation energy determines the overlayer critical thickness beyond which misfit dislocations (MD's) are energetically more favored than strains.

The lattice misfit between two materials A and B is related to the difference between their lattice parameters $\Delta = |a_A - a_B|$. The dislocations which are created when the conditions of strain relief are fulfilled are characterized by a geometric feature, namely the associated Burgers vector. At a nanometric scale, the elementary quantity which we may define is a "small" Burgers vector $b_e = a_B - a_A$, with $a_B > a_A$: b_e represents a rather small fraction of the lattice parameters. In the case of perfect epitaxy, b_e corresponds to small epitaxial dislocations. By a vernier effect, we end up with a network of epitaxial MD's which are fairly parallel with a lattice spacing equal to L . Their density is low when Δ is small: if $b_e \rightarrow 0$, one may expect that $L \rightarrow \infty$, ensuring a very small dislocation density. The appearance of the MD's corresponds to a negative free energy associated with these defects, as they aim at relaxing interface strains. The lattice spacing L is usually obtained by applying the following geometric conditions:

$$(n_1 + 1)a_A = n_1 a_B; \quad n_1 = a_A(a_B - a_A)^{-1}, \quad \text{if } a_A < a_B \quad (1)$$

$$(n_1 + 1)a_B = n_1 a_A; \quad n_1 = a_B(a_A - a_B)^{-1}, \quad \text{if } a_A > a_B \quad (2)$$

If we consider, e.g., Eq. 1, it states that after n_1 jumps on the lattice B and $(n_1 + 1)$ jumps on the lattice A, we may find in coincidence two interface sites belonging respectively to A and B. In the framework of the geometric approach L is then calculated by using the value of n_1 and the expression of the corresponding Burgers vector. Within this approach, we can learn that the best host materials for heteroepitaxy are those providing the highest value of L , i.e., eventually the lowest MD density.

In what follows, we will show that not only the geometric features of host materials are relevant to heteroepitaxy but also those features related to their elastic properties, through which the temperature effects are also involved as these elastic features are temperature dependent. The idea of taking account of these elastic features can be derived by analyzing the elasticity theory equations. These equations relate strain to lattice dynamics features

through relationships involving the $S=f(C_{ij})/\rho$ factor, where ρ is the density. For each interface configuration, i.e., for a specific growth plane, the dynamics equations involve effective elastic constants $f(C_{ij})$ which correspond to elastic waves propagating along the principal symmetry directions in cubic crystals. The expressions of $f(C_{ij})$ for the longitudinal and transverse modes are given below respectively for the [100], [110] and [111] directions:

- For longitudinal modes:

$$f(C_{ij})=C_{11} \text{ (a)}, f(C_{ij})=C_{11}+C_{12}+2C_{44} \text{ (b)}, f(C_{ij})=C_{11}+2C_{12}+4C_{44} \text{ (c)} \quad (3)$$

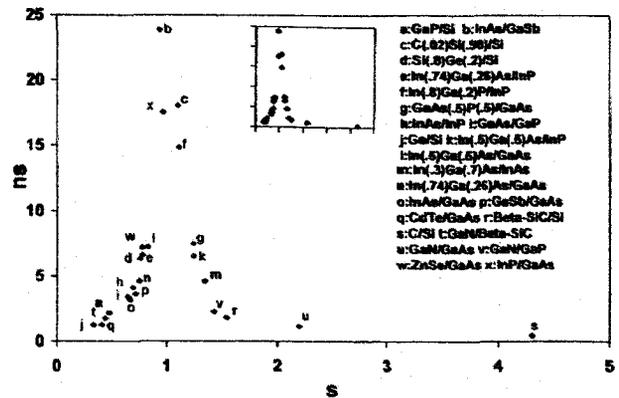
- For transverse modes:

$$f(C_{ij})=C_{44} \text{ (a)}, f(C_{ij})=0.5(C_{11}-C_{12}) \text{ (b)}, f(C_{ij})=(C_{11}-C_{12}+C_{44})/3 \text{ (c)} \quad (4)$$

The relevance of these elasticity-related features for a number of effects characteristics of coherent epitaxial solids and for epitaxy-induced structural phase transformations has been discussed in refs. In our approach, we derive renormalized expressions n_s of the geometric factor n_1 showing the effect of the ratio S of the $S_{A,B}$ factors (effective elastic constants) of the substrate and the epilayer in the case of B/A heterostructure involving one interface. The relevance of S is depicted on the following figure for several heterostructures including nitrides-based systems. One can see that the highest values of n_s , i.e., the smallest MD's densities are obtained for $S \approx 1$ and that n_s decreases when the mismatch of the S_A and S_B factors increases.

For systems where a large lattice mismatch exists between the host materials, the strategy of growing buffer layers before the elaboration of the final overlayer is currently widely used. These transitional layers are aimed at ensuring a continuous matching of the relevant features of the host materials (substrate and overlayer) selected for the growth experiment. It is then important to develop reliable and well-based criteria in order to make an optimized choice of the buffer layer. These criteria are formulated by the continuity conditions for geometric (n_s) and elastic factors (S).

The epitaxial growth of GaN by modern growth techniques as metalorganic chemical vapor deposition is usually made by using sapphire as substrate. Despite the large lattice mismatch between these two materials ($> 12\%$), which implies, in principle, that a high density of dislocations may be present in the epilayer, it has been demonstrated that devices showing surprisingly high performance may be obtained. Defects which could damage the interface quality of the heterostructure are related to the existence of interface defects between misoriented domains in the GaN overlayer, consisting in low-angle grain boundaries. An alternative to the use of sapphire substrates can be provided by SiC because of a better lattice matching and closer thermal expansion. This is expected to give improved crystalline characteristics. One possible strategy to increase this crystalline quality is to introduce a AlN buffer layer. Thus we demonstrate that the matching at the AlN/SiC interface of the dynamics-strain related factors is improved. These previsions show that the SiC-substrate alternative with the use of AlN buffer layer is a valuable approach for GaN heteroepitaxy.



Theoretical investigation of an intrinsic defect in SiC

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Many unidentified intrinsic defects have been measured in the photoluminescence (PL) and Raman spectra of irradiated SiC. The best known ones are the so-called D_I and D_{II} PL centers [1,2] found in H⁺, He⁺ and C⁺ bombarded SiC samples. These are stable up to 1700 °C. The D_{II} center shows five localized modes above the phonon continuum from 1031 cm⁻¹ up to 1328 cm⁻¹. Since the D_{II} center is formed after carbon implantation, local a carbon excess is expected to give rise to these bands. Dramatic changes occurred in the Raman spectrum as the implant concentration was varied from 10²⁰ H⁺ ions/cm³ to 10²² H⁺ ions/cm³. New peaks appeared at 1080 and 1435 cm⁻¹ and at 1400 and 1600 cm⁻¹ [3]. We call these centers R1 and R2, respectively. The first two peaks disappeared simultaneously at 800 °C, while the last two at 600 °C. Based on the higher dose of implants it is expected that more Si vacancies are created while the annealing behavior shows that these centers contain mobile ingredients, most probably carbon interstitials. These centers have been known since decades but very little additional information is available about them.

The conditions of the creation of these centers imply that carbon interstitials play a crucial role in them. We have investigated the carbon di-interstitial defect in a silicon vacancy in 3C- and 4H-SiC. *Ab initio* calculations using the local density approximation of the density functional theory and norm-conserving pseudopotentials have been carried out on supercells in both polytypes. The LVMs and the occupation levels have been determined.

The calculated LVMs of this complex are at 1413 cm⁻¹ and 1155 cm⁻¹ (double degenerate) in 3C-SiC. Both modes are Raman active. The calculated frequencies are reasonably close to the measured ones (at 1435 and 1080 cm⁻¹) in the Raman spectrum, thus we suggest this defect as the microscopic model for the R1 center. The carbon isotope shifts in the vibration modes are predicted as a means to confirm our model experimentally. It is found that the defect complex can act both as a double electron and as a hole trap. The predicted occupation levels should be measurable by deep level transient spectroscopy (DLTS).

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Modification of SiC Properties by Insertion of Ge and Si Nanocrystallites — Description by *ab initio* Supercell Calculations

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The use of SiC for optical applications is limited by its indirect character. According to the k-conservation rule, at the fundamental gap direct transitions cannot contribute to luminescence or absorption. However, defects or nanostructures destroy the translational symmetry and thus make it possible to circumvent this problem. Hence we study Ge and Si nanocrystallites embedded in SiC. These structures are expected to be suitable for luminescence in the visible spectral range even including the blue [1]. Nanostructures of this kind have been produced by ion implantation in amorphous SiO₂ matrices, by electrochemical etching, or by Stranski-Krastanov growth in molecular beam epitaxy [2,3]. In order to achieve electroluminescence, a host material which can be doped, and which has an appropriate band gap is needed. The wide-gap material SiC will be a convenient matrix material. In fact, recent results of ion implantation with subsequent annealing of Ge nanocrystallites in SiC provide the experimental background and the incentive of our work. An example of such a Ge dot is shown in Fig. a) [4]. The questions to be answered by experimentalists and theorists include those of composition and structure of the embedded dots as well as the influence of the embedment on the structure of the inclusions. Indications have been found of hexagonal Ge as well as of GeC phases embedded in hexagonal SiC.

Our main goal is the parameter-free description of the optical properties of these systems. The qualitative description of the different influences allows recommendations to experimental groups in order to achieve luminescence from embedded nanocrystallites. The spectral properties of the nanocrystallites are described within Density Functional Theory (DFT) in Local Density Approximation (LDA) and by means of the Projector-Augmented Wave (PAW) Method. The dielectric function is calculated from transition matrix elements and band energies using a quadratically extrapolative tetrahedron method [5]. We study spherical Ge and Si nanocrystallites of 5 to 239 atoms embedded in cubic SiC as well as free, hydrogenated nanocrystallites to simulate embedment in a wide-gap semiconductor. Finally, we also show results for nanocrystals in hexagonal SiC.

We use the supercell method which starts from one large cell of host material with one nanocrystallite. This building block is now repeated infinitely in all space directions. Thus our material is a composite made of the nanocrystals surrounded by SiC. We show that by means of an effective medium theory it is possible to extract the optical properties of the nanocrystals and to calculate the behavior of a new composite material with other filling factors. The dot-related quantities are size dependent due to quantum confinement effects. They depend on the type of dot material, the dot-host interface, and the shape of

the nanocrystals as well as on strain. Furthermore, the insertion of the quantum dots also alters the behavior of the host. Along with the interaction of neighboring nanocrystals, this is one limitation to the applicability of effective medium theories for systems with low barrier heights for electrons and holes or even for type-II heterostructures, e.g., Ge nanocrystals in cubic SiC. For systems with high barriers, the extraction of $\varepsilon_{\text{dot}}(\omega)$ is simple and precise. We compare the results to absorption spectra of embedded Ge crystallites.

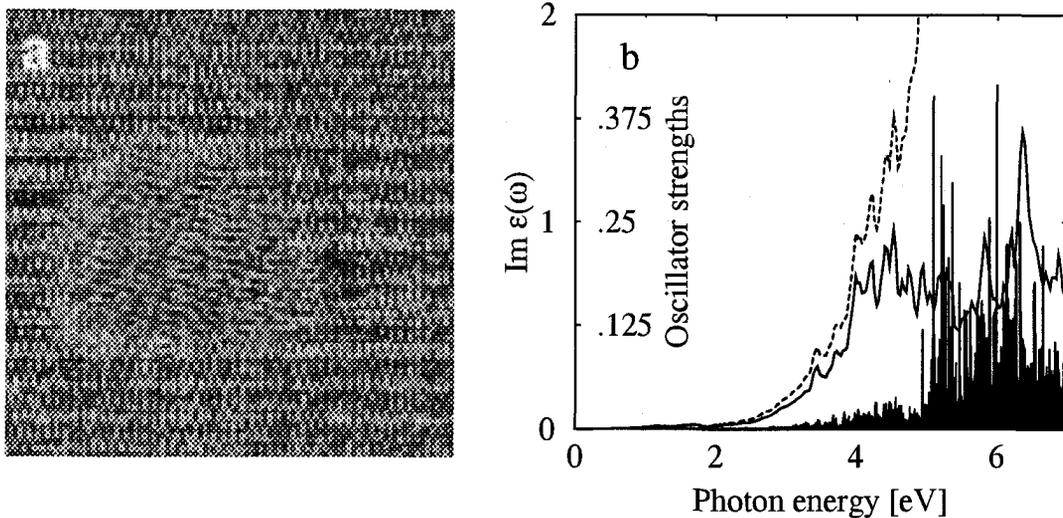


Fig. a) Example of a Ge dot in SiC, TEM picture [4], and b) Contribution of the gap states (solid line) to the total $\varepsilon(\omega)$ (dashed) and oscillator strengths (bars) of 41-atom Ge dot in 512-atom SiC cell.

The luminescence properties of any material are governed by the lowest few transitions. An example of oscillator strengths and the contribution of the gap states to the spectrum are shown in Fig. b). We have identified the origin of the important transitions, i.e., we have allocated them to the respective electronic states. It has been shown that the oscillator strengths and energies depend strongly on the shape and the strain of the crystals as well as on the dot-host interfaces. After all, a consistent picture encompasses the densities of states, the bandstructures, and the optical spectra.

In order to obtain results which represent real systems it is necessary to include the excitation aspect and to go beyond the LDA approximation in the electronic structure calculation. First results of self-energy calculations within the GW approximation are presented. Furthermore, excitation energies are calculated within the Δ SCF method.

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Theoretical calculation of stacking fault energies in silicon carbideHisaoami Iwata^{a)}, Ulf Lindefelt^{a,b)}, and Sven Öberg^{c)}^{a)}Department of Physics and Measurement Technology, Linköping University, SE-58183 Linköping, Sweden^{b)}ABB Corporate Research, SE-72178 Västerås, Sweden

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We report on a first-principles calculation of stacking fault (SF) energies in 3C-, 4H-, and 6H-SiC based on density-functional theory within the local-density approximation. All the structurally different SF in 3C-, 4H-, and 6H-SiC, which can be introduced by glide along the (0001) basal plane, are considered: 3C-, 4H-, and 6H-SiC have one, two, and three geometrically distinguishable SF, respectively, as shown in Fig.1. The SF energies are calculated using both a supercell method and the generalized axial next-nearest-neighbor Ising (ANNNI) model [1,2]. To confirm the accuracy of our calculation, the SF energies of Si and diamond are also calculated using the supercell method since the corresponding experimental values are known and relatively well established. Our theoretical calculations show very good agreement with available experimental results. Our calculation confirms that the SF energy of 3C-SiC is negative [3], and we also find that one of the three types of SF in 6H-SiC has considerably higher SF energy than the other two types (see Table I) [4].

The ANNNI model allows a simple, but still rather accurate, calculation of the SF energy in SiC from the results of several total energy calculations for perfect crystals (in this case from 2H-, 3C-, 4H-, and 6H-SiC). In order to model SF with the supercell approach, a very large number of atoms in the supercell is required (in the present study 96 atoms), and it is therefore very time-consuming. Our calculated inter-layer interaction parameters for the ANNNI model, from which one can determine approximately the SF energy for other SiC polytypes, give values which are very close to the available experimental data in the literature [2,4].

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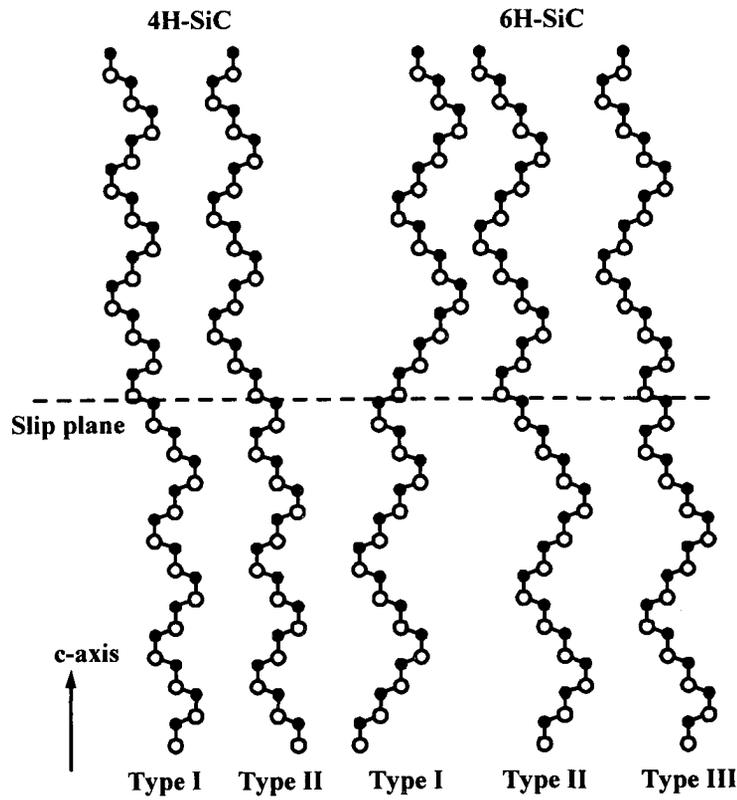


Fig.1. Geometrically distinguishable SFs in 4H- and 6H-SiC

Table I. Theoretical and experimental SF energies in 3C-, 4H-, and 6H-SiC (in mJ/m^2). Note that the ANNNI model does not distinguish between type I and type II SF in 4H- and 6H-SiC. To the authors' knowledge, structural differences between SFs have not been considered in the literature.

	3C-SiC	4H-SiC	6H-SiC
Supercell method			
Type I	-1.80	17.7	3.35
Type II	—	18.1	3.10
Type III	—	—	40.1
ANNNI model			
Type I	-6.27	18.3	3.14
Type II	—	18.3	3.14
Type III	—	—	36.6
Experiment			
Ref.2	—	14.7 ± 2.5	2.9 ± 0.6
Ref.5	—	—	2.5 ± 0.9

Stacking fault interactions and cubic polytype inclusions in 4H-SiCHisaoami Iwata^{a)}, Ulf Lindefelt^{a,b)}, and Sven Öberg^{c)}^{a)}Department of Physics and Measurement Technology, Linköping University, SE-58183 Linköping, Sweden^{b)}ABB Corporate Research, SE-72178 Västerås, Sweden

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A first-principles study of interacting stacking faults (SF) and polytype inclusions in silicon carbide, based on density-functional theory within the local-density approximation will be reported [1]. Polytype inclusions, i.e., the presence of different polytypes in a host crystal, have often been observed in hexagonal SiC polytypes. Although the mechanism for the creation of polytype inclusions is not known with certainty, one possibility is the motion of partial dislocations [2], each leaving behind an imperfect crystal containing a SF. If two partial dislocations having the same Burgers vector appear in neighboring (0001) planes, then a 3C-like inclusion can be created in the hexagonal crystal as shown in Fig.1. If still more partial dislocations are introduced, the thickness of the 3C-inclusion can increase (see Fig.1).

In another paper at this conference [3,4], we studied the effect of a single SF in SiC. In the present paper we introduce additional SFs in neighboring (0001) planes (note that SFs can not be present in all neighboring planes without violating the close-packing stacking sequence) and study the effect on the band structure. The calculations are performed using a supercell technique with 96 atoms per supercell (corresponding to 12 primitive unit cells for 4H-SiC). Figure 2 shows how the band structure changes as 1, 2, and 4 SFs in neighboring planes are introduced so as to convert a part of the 4H-SiC crystal to a 3C-like region. In the case of 4 SFs, the thickness of the 3C-like region is around 2.5 nm. We can see that, and as reported earlier [3,4], 1 SF splits off a band from the continuum of conduction band states, and that on increasing the number of neighboring SFs, this split-off band moves down in energy. This situation is of course consistent with a quantum well (QW) picture (the depth of the QW being equal to the conduction band offset between 3C- and 4H-SiC), where the ground state goes down in energy when the QW thickness increases.

The method has allowed us to study the effect of further SFs, SF-SF interactions and to analyze the wave functions, and will be discussed in the presentation.

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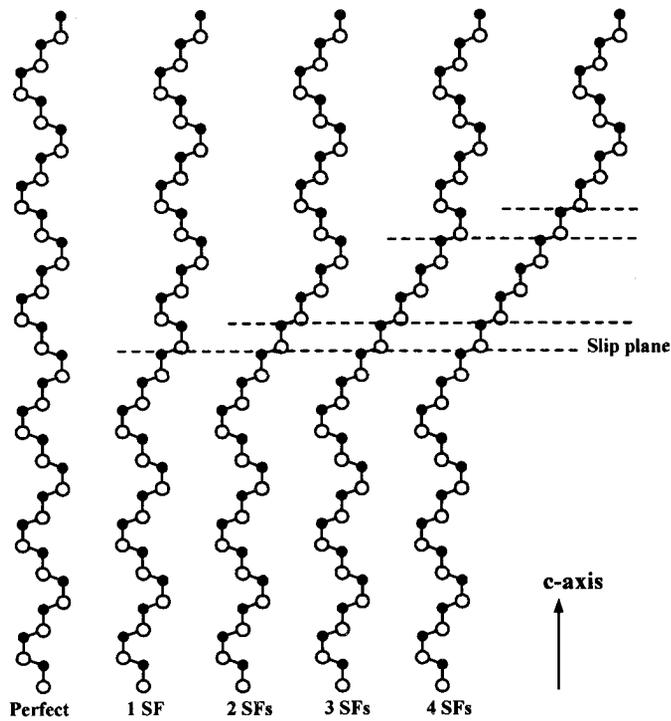


Fig.1. The creation of 3C-inclusions of various thicknesses in 4H-SiC by the stacking of SFs.

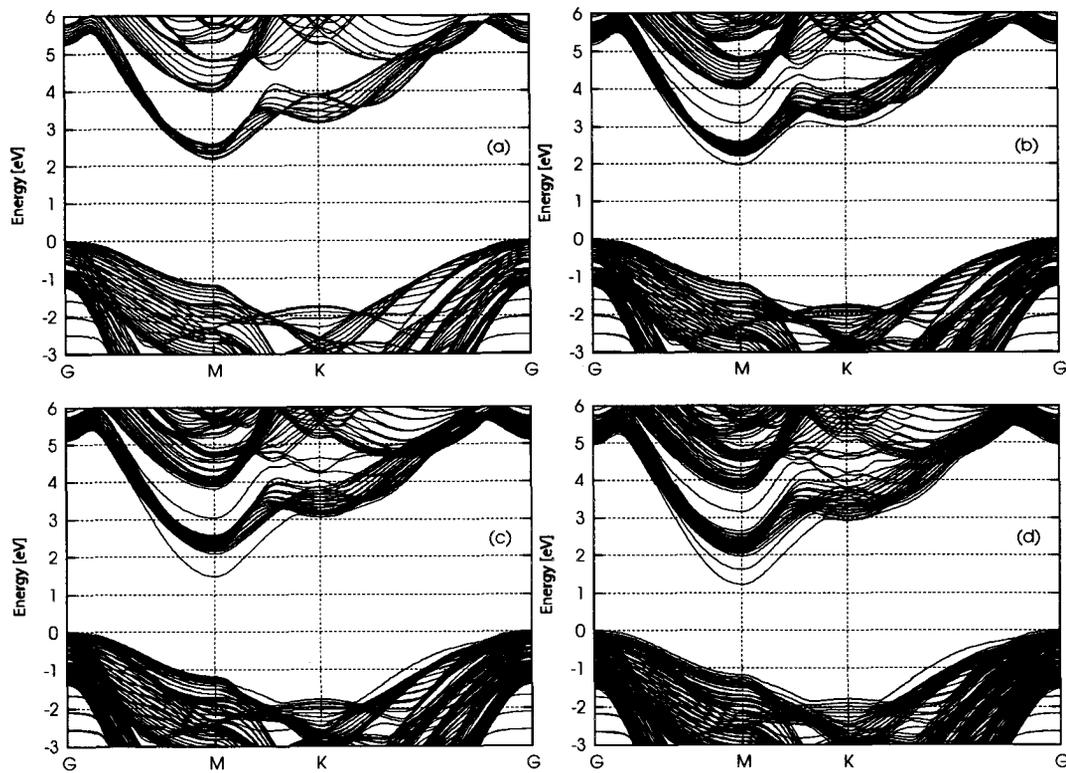


Fig.2. Band structures of (a) perfect 4H-SiC, (b) 4H-SiC with one SF, (c) 4H-SiC with two SFs, and (d) 4H-SiC with four SFs.

***Ab initio* calculation of B diffusion in SiC**

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Abstract

Boron diffusion in silicon has always been a high interest topic, experimentally and theoretically, due to the key role it plays in semiconductor doping processes. In silicon carbide, another material of growing interest in microelectronics, there are to date no theoretical studies on this topic.

Spin polarised *ab initio* calculations at DFT - LDA level were performed with a reasonable cell size (64 atoms) and a well-converged *k-point* sampling of the Brillouin zone. This combination of methods can be considered the *state of the art* in computational material science.

First the main defect configurations and their energy stability were analysed, both for the self interstitials (Si and C) and for B interstitial, in order to probe possible diffusion mechanisms, like Si kick-out [fig.1]. Then a path between two energy minima of a B interstitial was sampled, performing structural relaxations, but constraining the B atom to lay on a plane orthogonal to the selected path. This approach gave us valuable insight as to the diffusion path along the intermediate positions through which the B atom must go through, which normally are not taken into account in conventional studies, and how high the barrier to the diffusion is there.

B diffusion appears to be feasible, as the energy barrier to overcome is not very high (~ 0.6 eV). Moreover, another main feature of our calculations is that the diffusion mechanism that is conventionally postulated, consisting of a hopping process between a tetragonal position and a hexagonal position, appears to be too simplified and may give rise to lower barriers than the real ones. An unexpected result was that more than one, non-equivalent path between two minimum energy positions do exist [fig.2].

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Figures

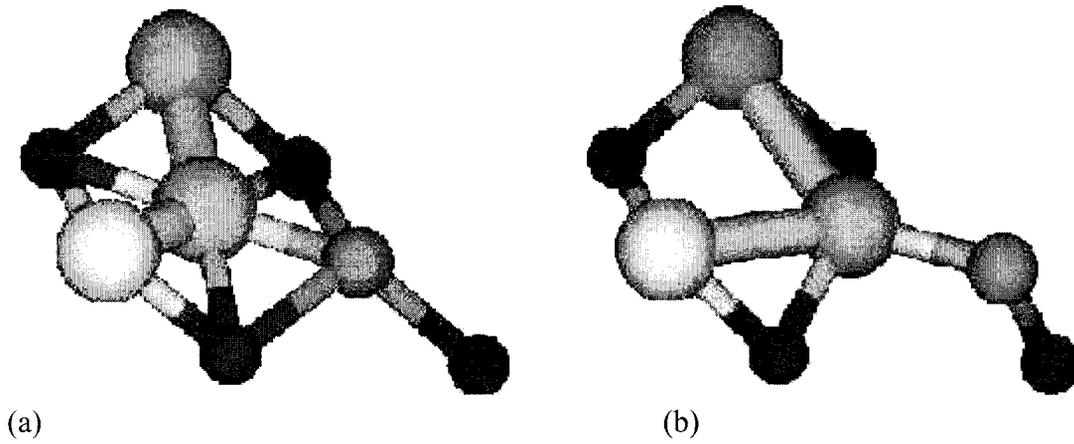


Figure 1 –B kick out. The configuration with a substitutional B in a Si site is made unstable in presence of an interstitial Si gets closer (a). The relaxed configuration (b) shows that to achieve equilibrium B is displaced and Si almost takes its own site back.

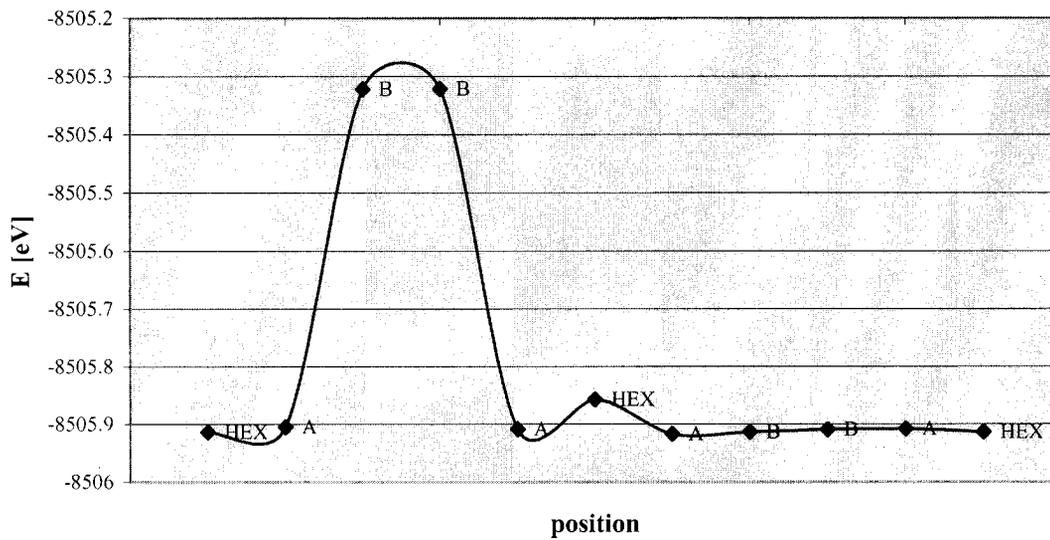


Figure 2 – Diffusion barrier. B diffusion along two different hexagonal-hexagonal paths. One presents a diffusion barrier around 0.6 eV, the other has no barrier.

Theory of Boron-Defects in SiC

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Boron as an acceptor-center in SiC has attracted much attention. Experiments have been focused on the electronic structure of boron-related centers [1,2], the electrical activation of the acceptor [3] and the properties of boron diffusion [4]. Though progress has been made in the understanding of the boron diffusion [5,6], the origin of experimentally observed boron centers is still unclear. While theory predicts substitutional boron acceptors on the carbon and silicon sublattice [5,7], in experiments only the shallow boron acceptor at a silicon site (B_{Si}) has been identified [1]. On the other hand, a recently proposed model [2] for the deep boron acceptor is at variance with theoretical predictions [5]. To obtain a microscopic picture of the properties of boron in 3C-SiC we have investigated by an *ab initio* method boron related defects and the boron diffusion. Our results show that substitutional boron may react with intrinsic point defects to form deep defect complexes or boron interstitials. Under p-type conditions, boron-carbon-vacancy complexes ($B_{Si}-V_C$ and B_C-V_C) and the tetrahedral carbon coordinated boron interstitial (B_{TC}) occur in comparable concentration as substitutional centers. Similarly we have found that boron pairs form. While the second nearest neighbor pair on the silicon sublattice ($B_{Si}-B_{Si}$) is only weakly bound, the nearest neighbor pair ($B_{Si}-B_C$) and the second nearest neighbor pair on the carbon sublattice (B_C-B_C) have a binding energy of about 1 eV. The latter two boron pairs have acceptor levels at 1.0 eV and 0.7 eV, respectively. This indicates that these pairs, besides substitutional boron on the carbon sublattice, may be responsible for the experimentally observed deep acceptor level. Yet, the spin density of the boron pairs cannot explain the EPR-data, that originally has been attributed to the deep acceptor. The electrical activation of boron is determined by three effects: (1) the binding of implanted boron in pairs, the formation of boron-carbon-vacancy complexes and boron interstitials, (2) the compensation of shallow boron by positively charged boron-carbon-vacancy complexes, the boron interstitial B_{TC} or other defects and (3) the out-diffusion of implanted boron during the anneal. According to our findings all these effects are operative. However, the electrical activation rises with the C/Si-ratio as the concentration of shallow boron increases and at the same time the compensation by the boron-related deep centers decreases. Our results indicate that boron migration in p-type material is governed by an interstitial mechanism preceded by a kick-out reaction with a silicon interstitial. This result supports the findings of recent experiments [6].

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THEORETICAL STUDIES ON VANADIUM IMPURITY IN β -SiC

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The studies of a vanadium impurity in silicon carbide are especially actual, as being an amphoteric impurity and forming deep levels near to the middle of the bandgap it allows to receive a semi-insulating material.

The vanadium impurity atom in silicon carbide crystal lattice can be localized in several structural nonequivalent interstitial (i) or substitutional (Si) positions. Besides in view of differences of atoms radiuses of silicon and vanadium in doped silicon carbide it is necessary to expect the effects of local structural relaxation. Till now the problems of shaping thin features of electronic allocations and nature of interatomic bonds in the system SiC:V in view of the marked circumstances remained practically uninvestigated.

In the present study *ab initio* X_{α} - discrete variation method (X_{α} - DVM) calculations of electronic structure and chemical bond parameters has been carried out for the clusters, which simulate possible versions of the isolated vanadium atom impurity intrusion into the β -SiC lattice.

The lattice structural and chemical distortions as a result of vanadium doping has been taken into account within the framework of the tight-binding theory in Harrison's bonding orbitals approach. It was supposed, that the perturbations introduced by the impurity atom, spread not further than next nearest neighbor and, accordingly, the interaction between vanadium impurity atoms was not under consideration.

The following main preliminary results should be marked:

1) for tetrahedrally coordinated substitutional impurity (V_{Si}) there is a considerable split of $V3d$ -orbitals by a crystalline field; at C-octahedrally coordinated interstitial position of vanadium (V_i) the impurity states forms an isolated level of $V3d$ -states inside the bandgap;

2) the external orbitals of V_{Si} form hybrid bonds with carbon atoms, for V_i the atom orbits overlap of vanadium and proximate silicon atoms is observed,

3) there is the local magnet moment (LMM) on vanadium atom for all of the surveyed positions; the LMM makes $\sim (1.4$ and $2.0)$ and $(0.0$ and $1.1) \mu_B$ for each of two variants V_{Si} and V_i . The results regarding the electronic structure, the formation energies, the ionization levels and the geometry of the relaxed structures of the defects caused by vanadium impurity intrusion into structurally nonequivalent SiC lattice positions will be reported and discussed.

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Evaluation of 6H-SiC(0001) surface after high-temperature hydrogen annealing by reflection high-energy positron diffraction and atomic force microscopy

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1. Introduction

To use SiC as the high performance device materials, it is necessary to make flat, oxide free and inactive surfaces. For this purpose, high-temperature hydrogen annealing is proposed. It is known that damages on SiC surfaces are removed and dangling bonds of SiC surfaces are terminated with atomic hydrogen after hydrogen annealing above 1100 °C [Ref.1]. We observed the dependence of 6H-SiC surface morphology on hydrogen annealing temperature using reflect high-energy positron diffraction (RHEPD) and atomic force microscopy (AFM). Using the total reflection mode, RHEPD can convey information about the topmost surface.

2. Experimental and results

Commercial 6H-SiC(0001) specimens were dipped in 5%-HF to remove surface oxides after boiling in acetone, H₂SO₄ and aqua regia to remove the organic substances and metal contaminants. Hydrogen annealing was conducted from 1000 to 1400 °C for 8 hours with H₂ gas pressure and flow rate of 100 Torr and 2 sl/m, respectively. Figures 1 and 2 show the AFM images after H₂ annealing at 1000 °C and 1400 °C, respectively [Ref.2]. In both annealing conditions, flat terraces and step structure are observed. The specimen which was

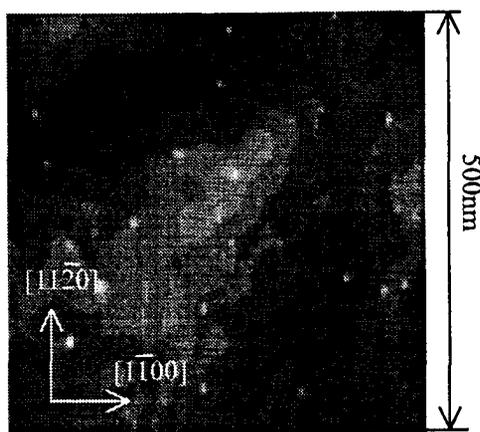


Fig. 1 AFM image for 6H-SiC (0001) after H₂ annealing at 1000 °C for 8 hours.

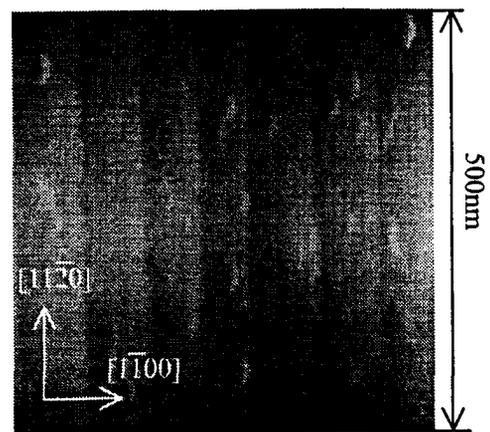


Fig. 2 AFM image for 6H-SiC (0001) after H₂ annealing at 1400 °C for 8 hours.

simply boiled in ultra pure water after dipping in 5%-HF, any terraces were not observed and root mean square roughness (Rq) was several tenths of Å. Thus, terraces appear due to hydrogen annealing. Typical step height between each terrace and Rq in terraces were several Å and less than 1 Å, respectively, after hydrogen annealing at 1000 °C. Nevertheless, the peripheries of terraces are not straight. Much more wider terraces and well-ordered step structure are observed after hydrogen annealing at 1400 °C. The step height between each terrace and Rq of terraces were approximately 1~2 Å, which are comparable to the Si-C bond length (1.87 Å). The step height and Rq are similar to the case of H₂ annealing at 1000 °C.

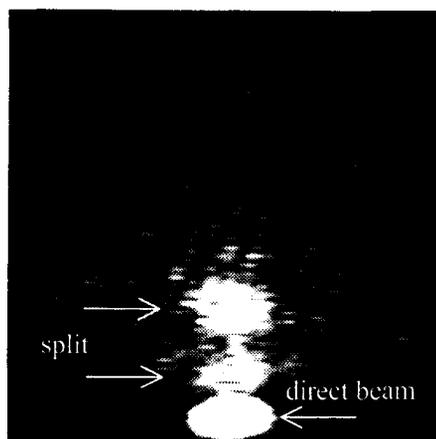


Fig. 3 RHEPD specular pattern for 6H-SiC(0001) after 5%-HF dipping and H₂O boiling.

RHEPD total reflection (at glancing angle of 1.1°) patterns are shown in Figs. 3 through 5 at $[1\bar{1}00]$ incidence. The lowest spot indicates the direct beam. Figure 3 was obtained from the specimen simply boiled in ultra pure water after dipped in 5%-HF. The pattern is heavily splitted. This suggests that the as received 6H-SiC surface was rather rough. From Figs. 4 and 5, it is seen that the specular patterns are spot like. This suggests that H₂ annealing at over 1000 °C make 6H-SiC surface atomically flat. These results are consistent with AFM observations.

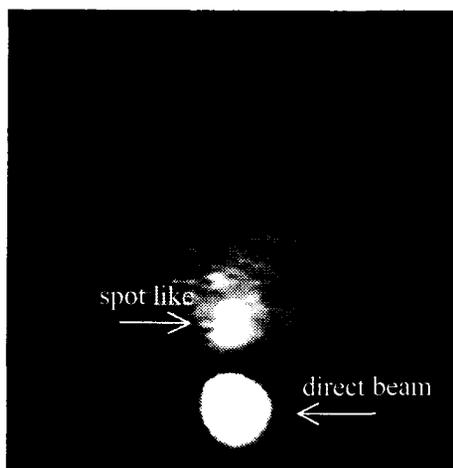


Fig. 4 RHEPD specular pattern for 6H-SiC(0001) after H₂ annealing at 1000 °C for 8 hours.

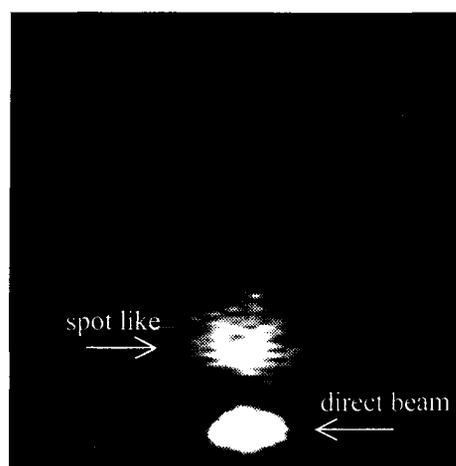


Fig. 5 RHEPD specular pattern for 6H-SiC(0001) after H₂ annealing at 1400 °C for 8 hours.

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Ion-implantation induced deep levels in SiC studied by Isothermal Capacitance Transient Spectroscopy (ICTS)

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Ion implantation is well known as one of the most potential selective doping technology to produce planar SiC devices, applicable for vertical types devices such as MOSFET and JFET. During the implantation, however, generally followed with generation of damage, destroying the crystalline structure of SiC. Although post-implantation annealing can recover the crystallinity, in contrast it causes new-secondary defect. In SiC, 3 types of implantation and successive post-implantation annealing induced defects have been reported¹⁾. These defects might work as origin of deep levels, act as trapping or recombination center and greatly limit device performances.

Concerning deep levels associated with these defects, recently, Dalibor et al have overviewed some intrinsic deep defect centers induced by ion-implantation together with the subsequent annealing in several SiC polytypes²⁾. Their results, however, have insufficient clarifications of which process and which region mostly involved with these defects. Moreover, there seem to be a lack for discussion the behaviors of these defects especially for elucidating the defect origins and the information of deep levels in as implanted sample as well as in post-annealed implanted one. In this contribution, we will give valuable data of deep levels related these defects particularly in as implanted 4H-SiC schottky device, their depth profile and the effect of post-implantation annealing, analyzed by isothermal capacitance transient spectroscopy (ICTS)³⁾. In this study we used n-type 4H-SiC(0001) substrate with 8° off-angle and n-type epitaxial layer purchased from CREE. The effective carrier density (Nd-Na) in epitaxial layer was $5 \times 10^{15} \text{ cm}^{-3}$. Multiple implantations of N were carried out at room temperature in order to form box-shape profiles with a depth of 0.3 μm . The total dose was $1 \times 10^{13} \text{ cm}^{-2}$. The subsequent annealing was carried out in Ar-ambient at 1500°C for 5 minutes. Ni electrodes were formed on SiC back surface by electron beam evaporation and annealed at 1000 C for 2 min, which leads to ohmic contact. To form the Schottky contact Ni was deposited on the ion implanted SiC-surface. The

ICTS measurements were performed in 10^{-2} Torr vacuum, at various temperatures, using sensitive-capacitance measurement apparatus (1MHz) with typical measurement condition of; reverse voltage $V_r = -2$ V, forward pulse voltage $V_p = 1$ V, and pulse width $W_p = 1$ ms.

In as-implanted SiC device, we found three typical deep levels i.e., E1, E2 and E3 with energy levels located at 0.375, 0.76 and 0.86 eV below conduction band, respectively. Since our measurement was limited at temperature range of $\pm 190^\circ\text{C}$, we suggest that deeper energy level might be detectable at higher temperature. Figure 1a and 1b show representative ICTS signals and Arrhenius plot of E1 taken at around ambience temperatures. From the depth profile results, interestingly, E1 and E2 were detected at depth region up to $0.8 \mu\text{m}$ from metal/ion-implanted SiC interface. On the other hand, ICTS signal of E3 appeared at deeper position. Two suggestions might be applicable here; one is that E1 and E2 are probably of deep levels associated with ion-implantation induced defects, where the densities decrease toward to deeper position. Second is that E3 may be due to a defect originally existing in the epitaxial layer, but as the defect concentration is much less than that of E1 and E2, it was undetectable at shallower region. Although further investigation to clarify the origin of these defect is required, these results prove that ICTS method is powerful for characterization such kind of these defects.

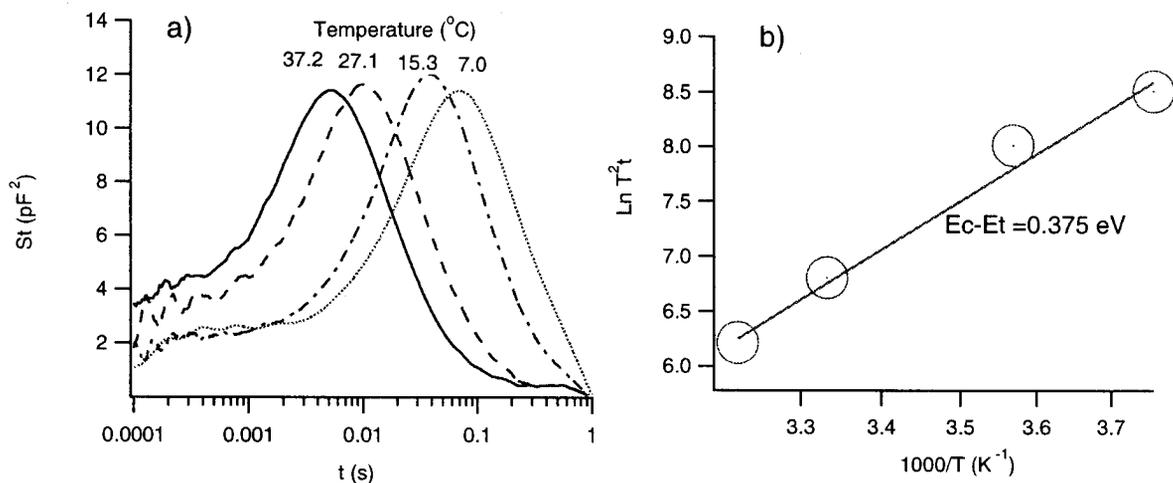


Fig.1 ICTS signals in as-implanted SiC schottky device (a) and Arrhenius plot of corresponding data (b) determined at around room temperature. This is identified as E1 with energy level located at 0.375 eV below the conduction band.

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Wafer-scale Defect Characterization of SiC Wafers Based on an Optical Technique

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Recent investigations have shown the large potential of SiC for high-power, high-temperature and high frequency electronics. Different wafer types (6H and 4H) grown by the modified Lely method are available at relatively low prices. However, silicon carbide wafers are far from being free of micropipes and other structure defects, which are deleterious to high quality epilayer growth for SiC device applications.

Characterization of structural and crystallographic defects in SiC single crystals is mainly established by X-ray topography, SEM/TEM, AFM, and etching methods. These methods are time-consuming, expensive, and sometimes destructive due to the necessary special techniques for sample preparation. Moreover, the most commonly used etching methods for defect delineation are destructive. It is very difficult to realize wafer-scale defect characterization of SiC wafers using the above methods. Therefore, it is essential to develop an economic, rapid, and nondestructive characterization technique for SiC wafer-scale evaluation of structural and crystallographic defects.

In this work, an optical technique has been developed successfully to characterize the structural and crystallographic defects in SiC wafers. A rapid, nondestructive and low-cost visualization technique is demonstrated. The technique allows revealing of micro- and nano-pipes as well as dislocations in basal-cut hexagonal SiC wafers. A comparison between the results from this technique and X-ray topography, AFM, and KOH etching is also presented.

Figure 1 shows typical dislocation distribution of a 6H-SiC wafer. The presented surface area is about $0.7 \times 0.7 \text{ mm}^2$.

This technique offers a method of observation of macro defects, such as micropipes on a wafer-scale, but also enables us to study micro scale defects, such as dislocations, and thus offers a wide range of possibility for material characterization in a completely non-destructive manner. It is especially effective for investigations of defect distribution and density influence on the device performance.

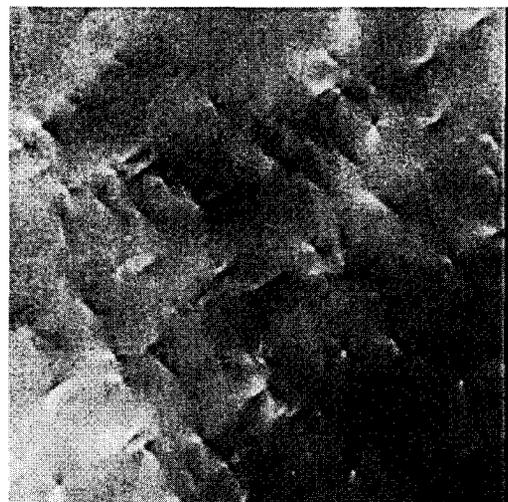


Figure 1. Dislocation distribution in 6H-SiC wafer

Luminescence and Electron Paramagnetic Resonance in AlN Layers Implanted with Er and O Ions

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The interest in the study of the luminescence of Er ions in semiconductors is due to the prospects of employing them in optoelectronics. To obtain a better understanding of the defect-formation processes and the luminescence of Er³⁺ ions, various semiconductors have been investigated. According to the results, the thermal quenching of the photoluminescence (PL) intensity of Er ions decreases significantly as the gap width of the semiconductor increases. For example, in Si:Er the PL intensity of Er ions decreases by several orders of magnitude as the measurement temperature is raised from 77 K to 300 K [1], whereas in GaN:Er a severalfold decrease in the intensity is observed [2]. The purpose of the present work was to study the optical and magnetic properties of Er-doped aluminum nitride layers.

Erbium ions with an energy $E = 1$ MeV and dose $D = 5 \times 10^{14}$ cm⁻² and oxygen ions with $E = 0.115$ MeV and $D = 5 \times 10^{15}$ cm⁻² were implanted at room temperature. The implanted samples were annealed in a furnace for rapid thermal annealing at 1300°C during 30 s in a stream of nitrogen. The PL was excited by the emission of a halogen lamp and recorded by means of a monochromator with 3-nm resolution and an InGaAs photodetector operating at room temperature. The magnetic resonance was measured by an ER-220D electron paramagnetic resonance spectrometer in 3 cm range at temperature from 3.5 K to 120 K.

Figure 1 shows the PL spectra, measured at 80 K and 300 K, for a AlN:Er sample. In addition to the emission peak with a maximum at the wavelength $\lambda = 1.536$ μm due to transitions of Er³⁺ ions from the first excited state $^4I_{13/2}$ to the ground level $^4I_{15/2}$, the spectra also contain a series of small peaks in the vicinity of $\lambda \approx 1$ μm , which can be attributed to the ion transitions from the second excited state $^4I_{11/2}$ to the ground state, and a broad luminescence band in the interval $\lambda \sim 1.02$ -1.12 μm . The Er-related PL intensity at $\lambda = 1.536$ μm increases by a factor of 2 when the measurement temperature is lowered from 300 K to 80 K. The broad emission band is associated with the PL of defects in AlN, since the PL intensity increases after additional implantation of oxygen ions. The Er-related PL intensity at $\lambda = 1.536$ μm in AlN:Er is higher than that in AlN:(Er,O) by several orders of magnitude.

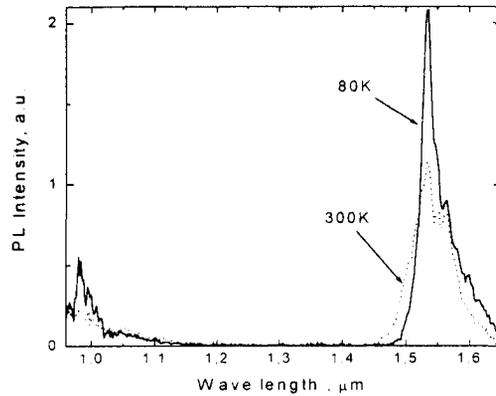


Fig. 1. PL spectra of AlN:Er sample. Spectra were measured at 80 K and 300 K.

The magnetic resonance signals in AlN:Er and AlN:(Er,O) are observed from 60 K to 110K and from 4.1 K to 110 K, respectively. A spectrum contains one isotropic line with parameters strongly dependent on temperature (Fig. 2). The inversion of magnetic field is not followed by the reproducibility of position and intensity of the line in the AlN:(Er,O) sample. Observation of magnetic resonance at high temperatures shows the magnetic centers have zero orbital momentum. We believe that the centers are formed by lattice intrinsic point defects. Temperature dependence of resonance signal parameters can be explained by changes of the internal magnetic field. This field can appear due to exchange interaction between erbium atoms, without exchange interaction with other defects. So, magnetic resonance studies show the presence of lattice defects surrounding the magnetically ordered clusters of erbium ions.

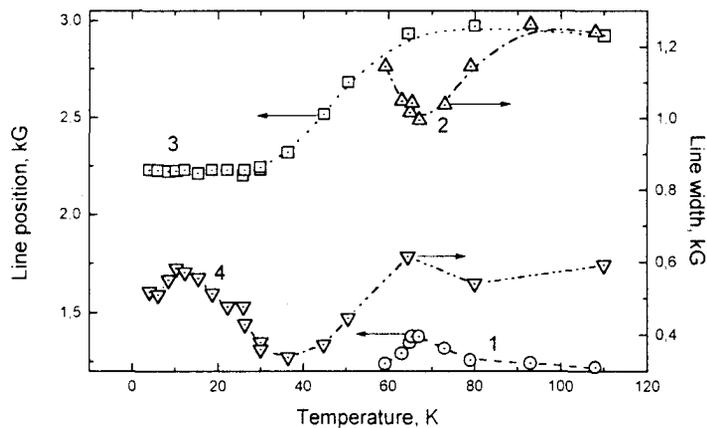


Fig. 2. Temperature dependencies of the line position (1,3) and line width (2,4) for AlN:Er (1,2) and AlN:(Er,O) (3,4) samples.

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Electrical characterization of SiC/Si heterostructures with modified interfacesCh. Förster, J. Pezoldt

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The problems to grow 3C-Bulk crystals has retained over the years the interest to the thin film heteroepitaxy on silicon substrates. Beneath the fundamental question of the heteroepitaxial growth in a material system with large lattice mismatch, the SiC - Si system has certain attractive applications. The first is in the field of robust sensors operating at high temperatures and harsh environments. The second is in the field of substrates for the nitride epitaxy. The common technique to grow SiC on Si is a two step process consisting of a carbonization process followed by epitaxial growth. The grown layers suffer from the high lattice and thermal lattice mismatch between these two materials leading to high residual stresses and lattice defect densities in the grown silicon carbide layer and the heterojunction. The properties of the SiC layer can be improved by using one of the following substrate modification methods: (1) silicon on insulator, (2) porous silicon, (3) modification of the silicon substrate with group IV elements. Only the last method is applicable if the electrical properties of the heterojunction are of interest.

To have an insight in the influence of the surface preparation techniques on the properties of the SiC/Si system the following methods of creating a SiC pseudosubstrate were used: (1) conversion of Si(111) into SiC(111) by RTCVD using propane diluted in hydrogen, (2) conversion of Si(111) into SiC(111) by solid source molecular beam epitaxy, i.e. in a hydrogen poor environment, (3) conversion of Si(111) modified by Ge predeposition into SiC(111) by SSMBE. On these substrates 3C-SiC epitaxial layers were grown at 1000°C with a growth rate of 1nm/min. The growth were carried out at Si rich conditions and continuously operating Si and C sources. The stability of the growth conditions were controlled by using the (3×3)-Si(111)SiC surface reconstruction. The growth process was monitored by *in situ* reflection high energy electron diffraction and *in situ* spectroscopic ellipsometry in real time. The films were investigated *ex situ* by atomic force microscopy, X-ray diffraction. For electrical characterization heterodiodes were prepared.

The results obtained show that the epitaxial layers are characterized by a single domain 3C-SiC structure. The layers grown on RTCVD carbonized material shown a carbon face where as the layers grown on MBE carbonized material exhibit a silicon face [1]. In dependence on the polarity of the deposited layers different built in voltages were observed indicating on a band offset in dependence on the SiC polarity on Si. For both cases it was observed that Ge predeposition lead to an improved electrical properties of the formed heterojunction. This was obtained for the forward direction where the ideality factor was improved from 1.8 to 1.3 as well as for the reverse direction where the reverse currents which decreases with increasing Ge coverage. The obtained current-voltage and capacity-voltage characteristics were analysed in terms of interface state densities and band offsets. Detailed band diagrams in dependence on the interface modification method will be presented.

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Carrier concentrations in implanted and epitaxial 4H-SiC by Scanning Spreading Resistance Microscopy

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Developments in process technology and electrical characteristics of silicon carbide based devices require precise knowledge of the charge carrier distribution in the material. Especially, the activation of implanted species in SiC is crucial for device performance, but can not be determined using the standard dopant profiling techniques of today. Attempts have been made to measure p-type aluminum and boron implantation profiles in 4H-SiC by spreading resistance profiling (SRP), but the hardness and electrical barrier between the probe and sample were found to limit the dynamic range and prevent contact formation for low carrier concentrations [1, 2]. Other types of dopant profiling techniques have also been investigated, none of which have been able to provide sufficiently reproducible and, in particular, quantifiable data [2].

In contrast to the results from conventional SRP however, we report here of the successful application of a novel spreading resistance method for wide range and high gradient free carrier concentration measurements in SiC, namely scanning spreading resistance microscopy (SSRM). SSRM is a recently developed scanning probe microscopy (SPM) based technique, using an atomic force microscope (AFM). It has previously been applied for dopant profiling/imaging in Si [3] as well as three-five materials such as InP [4].

The SSRM set-up consists of a Digital Instruments Dimension 3100 AFM system with a commercially available SSRM add-on module equipped with logarithmic current amplification, which utilizes boron doped diamond coated tips. The arrangement enables penetration of the native oxide by high forces and provides continuous (or single-step) one or two dimensional SR measurements, with spatial resolution of about 30 nm and a dynamic range of up to seven orders of magnitude, typically 10^{14} to 10^{21} cm^{-3} [5].

An example demonstrating the wide dynamic range is depicted in Figure 1 (a), which shows the averaged SSRM current across an Al-doped epitaxial stair-case structure of 4H-SiC together with the corresponding secondary ion mass spectrometry (SIMS) data in (b). The step-heights are in very good agreement with SIMS, except at the highest peak, which may be attributed to the reduced activation and/or mobility observed for Al concentrations $> 10^{20}$ cm^{-3} [6]. It should also be mentioned that conventional SRP measurements of the same structure had difficulties to detect concentrations already below the maximum peak at 2×10^{20} cm^{-3} . In Figure 2 (a) the combination of SSRM and SIMS data has been used to produce a calibration curve, which for the specific tip it is calibrated for, enables quantification of e.g. implantation profiles. As an example, we employ the calibration curve to evaluate an Al and B implantation profile of 4H-SiC in Figure 2 (b) and (c), measured after 10 min annealing at 1700 °C. The SSRM data reveals a much higher resistance in the highly Al doped region than suggested by the chemical concentration of $> 10^{20}$ cm^{-3} . The measured current in this region corresponds in fact to the resistance found at a concentration as low as about 10^{18} cm^{-3} in the epi layer calibration curve. The observation may be explained by the presence of remaining implantation induced defects in the material, even after annealing. Furthermore, the long diffusion tail of B into the material can be detected also electrically by this method, until the concentration reaches the level of the background n-type epi layer doping (2×10^{15} cm^{-3}) at about 3 μm depth.

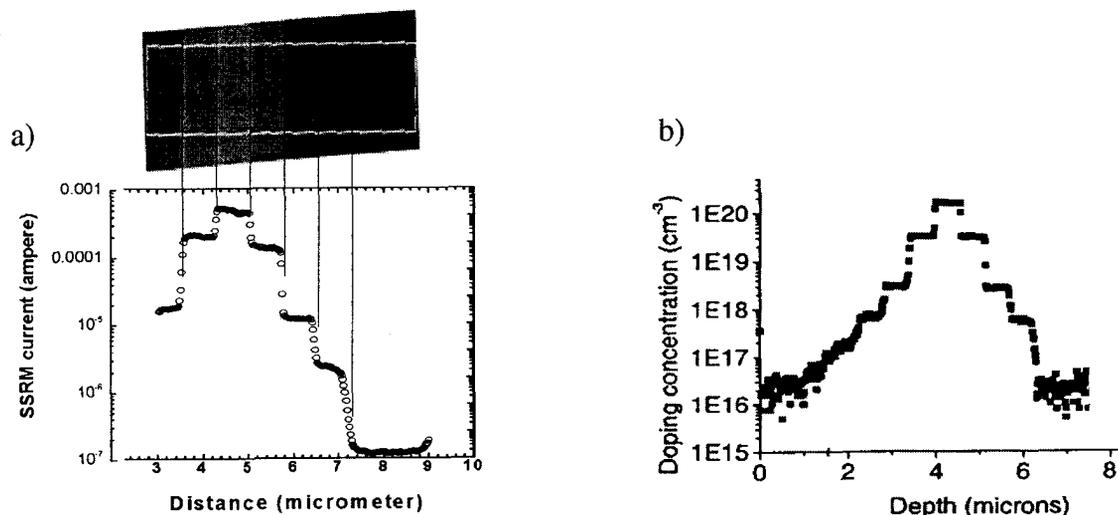


Fig 1. (a) SSRM and (b) SIMS depth profiles of an Al doped epi layer of 4H-SiC. The SSRM signal represents the average of multiple scans (> 50) selected from a surface region free from topographical gradients, which is marked by white lines in the two-dimensional SSRM image shown as inset above (a).

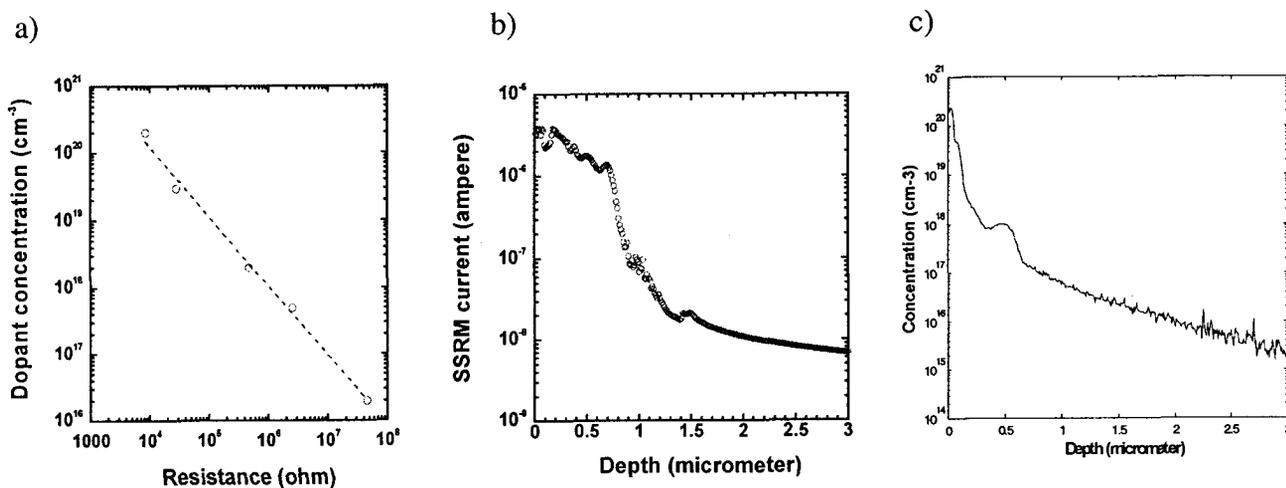


Figure 2. a) Calibration curve for extraction of carrier concentration from measured resistance. The data is tip-specific for each diamond coated SSRM tip. b) SSRM line scan of an Al and B implantation profile using the same tip as in a) at a bias voltage of 5V. c) SIMS measurements the same implantation, for comparison plotted as the sum of both Al and B.

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Thermoelectric properties of β -SiC produced by silicon carbonization

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Introduction

Silicon carbide (SiC) is a wide-band-gap semiconductor with high chemical stability at high temperatures. Therefore, SiC may be an excellent candidate of the materials for devices which can operate at high-temperature, -frequency or -power conditions. However, it is generally considered that SiC is unsuitable for thermoelectric applications due to its rather high thermal conductivity. This is because the thermoelectric figure of merit Z retains lower values for materials with a higher thermal conductivity. Here, Z is defined by the equation, $Z = \alpha^2 \sigma / \kappa$, where α , σ , and κ are the Seebeck coefficient, the electric conductivity, and the thermal conductivity, respectively. To get a large Z value it is required to increase both α and σ , and to decrease κ , simultaneously. We tried to fulfill these requirements by adopting a novel synthesizing method for SiC, in which β -SiC is fabricated by the carbonization of commercial Si wafers doped with different concentrations of impurities.

Experimental Procedure

We used 0.5 mm thick Si-wafers as a silicon source, and graphite powders of 99.98 % purity as a carbon source. The wafers were put into a carbon case filled with graphite powders. The case was evacuated in a chamber down to 1×10^{-3} Pa at 600 °C, and subsequently the chamber was filled with Ar gas of 1 atm. The carbonization of Si-wafers was carried out at 1300 °C for 24 hours. During this process, the surfaces of the wafers were carbonized, and SiC layers were formed. The crystal structure and composition of these samples were studied by X-ray diffraction (XRD) and electron probe microanalysis (EPMA). The microstructures were characterized by using

transmission electron microscopy (TEM) and field emission scanning electron microscopy (FE-SEM). The thermoelectric properties of the samples were evaluated by measuring the DC conductivity and the Seebeck coefficient at elevated temperatures (R.T.~1000 °C).

Experimental Results

Structure and composition

The XRD patterns of the carbonized samples showed the formation of β -SiC on the surfaces of the wafers. The cross sectional SEM observation revealed that the thickness of the SiC layer was about 55 μ m beneath the original surfaces of the wafer. (Fig. 1)

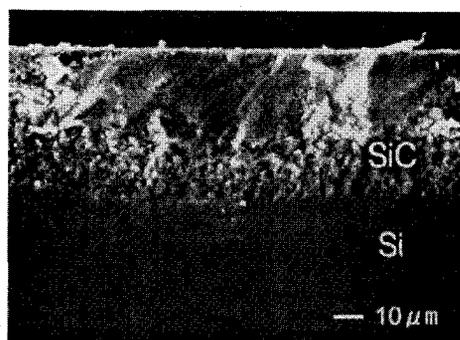


Fig.1 Cross section SEM micrograph of sample

Since the relative density of the β -SiC layer was approximately 60 %, it is expected that the present carbonization process has a role to make the SiC layer porous. The size of SiC crystallites and pores was estimated to be about 10~50 nm and 10~100 nm, respectively, by TEM observations. In addition, HR-TEM indicated the presence of grain boundary amorphous layers. The composition of the β -SiC layer analyzed by EPMA was C-rich (Si/C \approx 0.8) and the amount of oxygen was rather high. The excess Si and oxygen are assumed to be due to the presence of

the grain boundary amorphous phase (SiO_2), since the XRD pattern of the β -SiC phase showed no apparent peak shifts.

Electrical Properties

It is interesting to see the effects of impurities, already doped in the Si-wafers, on the electrical conductivity of the SiC prepared by the carbonization process. Figure 2 shows the Arrhenius plots of σ for two different samples. The sample formed from the high-doped wafer indicates higher conductivity values of the order of $10^4 \sim 10^5 \text{ } \Omega^{-1} \cdot \text{m}^{-1}$, whereas that formed from the low-doped wafer has low conductivity values ranging $10^2 \sim 10^3 \text{ } \Omega^{-1} \cdot \text{m}^{-1}$. With increasing temperature up to 600–1000 °C, however, the conductivity of these samples came to similar values which can be fitted to a straight line.

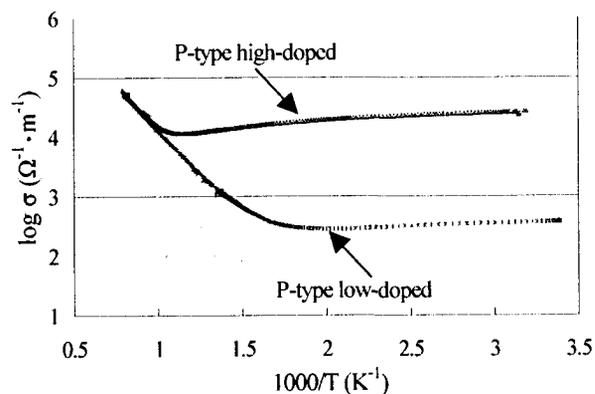


Fig.2 Arrhenius plots of electrical conductivity for samples.

The temperature dependence of the Seebeck coefficient for the SiC samples is shown in Fig.3. The sign of α depended on the conduction type of the wafer used. A negative sign was observed for the samples prepared from the n-type wafers, and a positive sign was found for those prepared from the p-type wafers, though the sign changed to negative at high temperatures $> 850 \text{ } ^\circ\text{C}$. It is also found that the samples formed from the high-doped wafers gave very high values of the Seebeck coefficient $\approx 600 \text{ } \mu\text{V/K}$ at a temperature range 400–500 °C.

An example of the power factor $P (= \alpha^2 \sigma)$ for the SiC sample is given in Fig.4. It is clear that β

-SiC obtained by the present carbonization process exhibits very large power factor values greater than 10^{-3} W/mK^2 at 300–600 °C, which is quite attractive from a practical view point of thermoelectrical applications.

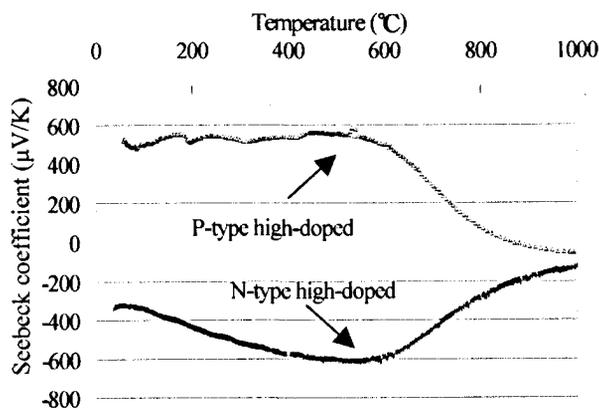


Fig.3 Temperature dependence of Seebeck coefficient.

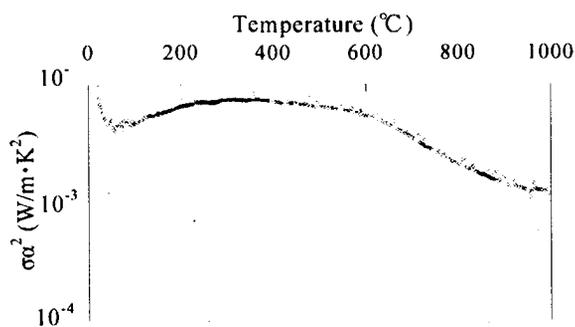


Fig.4 Temperature dependence of power factor.

Conclusions

We successfully produced porous β -SiC on Si-wafers by a silicon carbonization process. The results of thermoelectric characterizations showed that the SiC samples prepared from the high-doped wafer have high electrical conductivities and high Seebeck coefficients, which may be suitable for high temperature thermoelectric applications. It could also be expected that the thermal conductivity of the SiC samples must be reduced extremely because of its porous structure.

Distribution profile of deep levels in SiC observed by isothermal capacitance transient spectroscopy

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Silicon carbide (SiC) has been attracting much attention as a material for high-power, high-frequency, and high-temperature devices. To realize the SiC devices, it is quite important to obtain information about deep levels in SiC, since deep levels in semiconductors, which are due to impurities or point defects, can be trapping or recombination centers and influence device performance. Attempts to evaluate deep levels in SiC have been done and several deep levels have been found in SiC.¹⁾ In the present work, we have tried to observe the distribution of deep levels in SiC by use of isothermal capacitance transient spectroscopy (ICTS).²⁾

Samples used were n-type 4H-SiC (0001) substrate with effective carrier density ($N_d - N_a$) of 2.6×10^{17} having 8° off-angle purchased from CREE. A part of the substrate was cut into 12×12 mm squares, and a 4H-SiC epitaxial layer was deposited on the Si face of the substrate by the low-pressure, hot wall type, horizontal chemical vapor deposition method. The epitaxial layer was n-type with effective carrier density of $2 \times 10^{15} \text{ cm}^{-3}$. Nickel Schottky contact and Mg ohmic contact were formed on the Si face and on the C face of the samples, respectively. The ICTS measurements were performed in 10^{-2} Torr vacuum at the temperature range from 80 to 470 K. The applied forward pulse voltage and the pulse width were 1 V and 10 ms, respectively. Depth profiles of the deep levels were obtained by changing the applied reverse voltage.

Figure 1 shows the ICTS spectra observed in the substrate sample. The energy level of the deep level showing the ICTS signal was calculated to be $E_c - 0.94 \text{ eV}$ from the shift of the peak with temperature, where E_c indicates the energy level of the

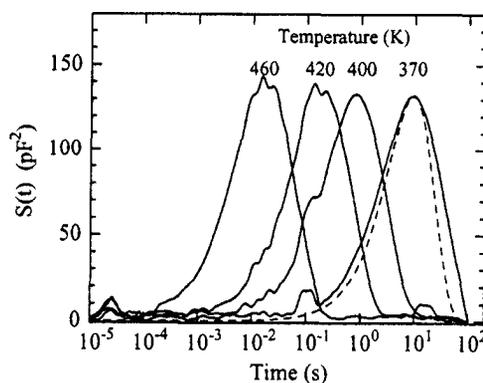


Fig. 1. ICTS spectra observed in the substrate sample at the temperature range from 370 to 460K.

conduction band. Figure 2 shows the depth profile of the concentration of the deep level from the sample surface. This result indicates that the deep level was uniformly distributed in the substrate.

Figure 3 shows the ICTS spectrum observed in the epitaxial layer at 290 K. The calculated energy level of the deep level was $E_c - 0.6$ eV. This deep level is considered to be due to the Z_1 center reported in Ref. 1. The distribution of the Z_1 center in the sample is shown in Fig. 4. The concentration of the Z_1 center in the epitaxial layer close to the substrate is in the order of 10^{14} cm^{-3} , while it is about 1×10^{13} cm^{-3} at the sample surface. This result indicates that the Z_1 center was mainly introduced at the initial phase of the epitaxial growth.

The Z_1 center is not always observed in the epitaxial layers grown by the CVD apparatus. It has been observed that there is no correlation between the generation of Z_1 center and bulk substrate conditions. These facts indicate that the introduction of Z_1 center strongly depends on the epitaxial conditions.

This work was performed under the management of FED as a part of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

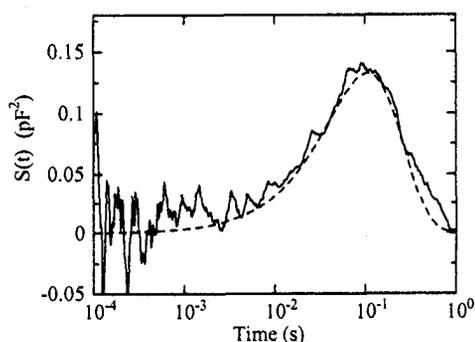


Fig. 3. ICTS spectrum observed in the epitaxial layer at 290 K.

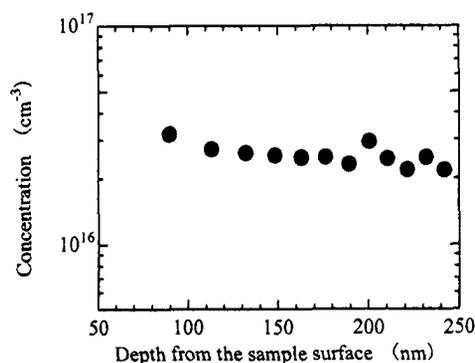


Fig. 2. Depth profile of the concentration of the deep level observed in the substrate sample.

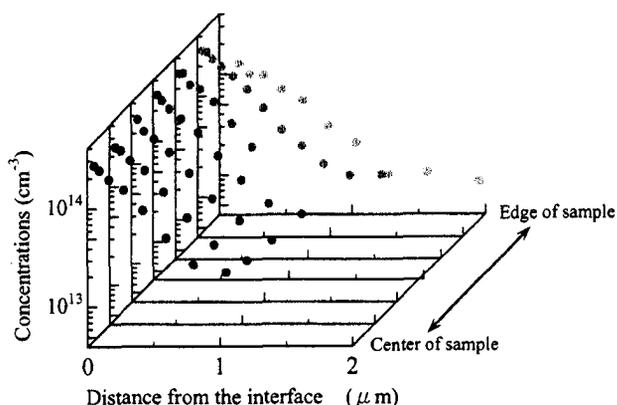


Fig. 4. Distribution of the Z_1 center in the epitaxial layer.

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Oxidation of porous 4H-SiC substrates

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Porous silicon carbide (por-SiC) has been investigated recently because of its potentially attractive properties for light emitting diodes¹, efficient photodetectors², and as templates for nano-structure epitaxial nucleation, and surface layer modification. Commonly, in device technology, the silicon dioxide formation plays a significant role. Moreover, the oxidation of a porous surface might modify the morphology of the surface that would result in changing of the optical and electrical characteristics of the modified surface. For these reasons, it is necessary to understand the kinetics of the oxide growth on a por-SiC substrate.

In this research we have been studying the influence of SiC crystal orientation (carbon vs. silicon terminated faces) on the kinetics of porous 4H-SiC substrate oxidation.

Anodization of n-4H-SiC samples purchased from CREE Research and Bandgap Technologies was carried out in dark mode at current densities from 10 to 60 mA/cm² in 2.5% HF solution for 2-10 min. After RCA cleaning, oxidation of the porous samples was performed in wet oxygen at 1000°C for 60-180 min.

The thicknesses of the grown oxide layers both on the porous and non-porous regions were measured by Dektak profilometer and by Rudolph ellipsometer as well. Also, the steps between porous and non-porous regions before and after the oxide removal were measured on each face to obtain data about the oxide propagation into por-SiC. Surface morphology of porous silicon and carbon faces before and after oxidation was analyzed by means of AFM.

It was found that the interface between the oxide layer and a porous substrate is always below that for non-porous substrate in both Si- and C-faces. However, the oxidation rate of porous substrate on the both faces is less than the plain carbon face but higher than the plain silicon face. This difference in the oxidation rates results in a thicker oxide layer grown on a non-porous C-face than on porous carbon and silicon faces, and thinner oxide layer grown on a non-porous Si-face than on porous carbon and silicon faces. The kinetics of oxidation of the porous layer is discussed in detail in this presentation.

The AFM images shown in Fig.1 have been taken from porous C-face before oxidation (Fig.1a) and after oxidation and subsequent removal of the oxide layer (Fig.1b). It is seen clearly that after oxidation of the porous c-face the surface peaks become more sharp. This surface modification will be discussed in terms of the anisotropy character of the silicon carbide oxidation.

Acknowledgments

The authors are grateful to Dr. X. Ma for AFM measurements.

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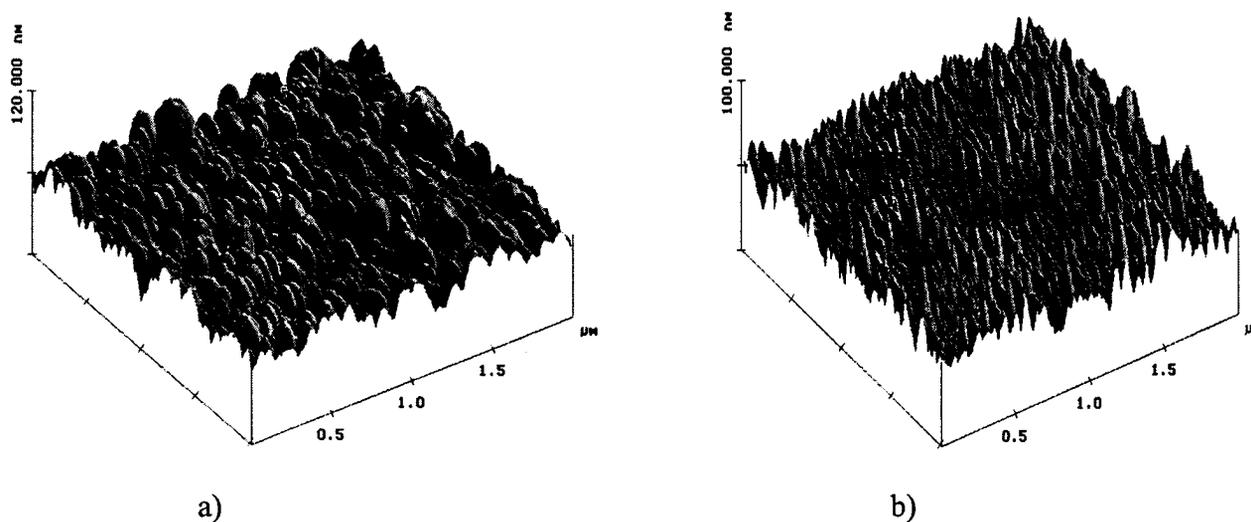


Fig.1. AFM images of (a) porous C-face before oxidation and (b) after oxidation and subsequent oxide removal.

Plasma Oxidation of SiC at Low Temperature below 300 °C

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The thermal oxidation of SiC is of important for the fabrication of metal-oxide-semiconductor structure and the insulating layer on SiC devices. The growth rate of SiO₂ layer on SiC due to the thermal oxidation is much slower than that of Si even at temperature of 1150 °C. On the other hand, it has been reported that Si can be oxidized by the plasma oxidation at extremely low temperature as low as 400 °C[1]. It is expected also that the plasma oxidation of SiC is useful to form the SiO₂ layer on SiC at low temperature. In this study, we report the plasma oxidation of SiC at temperature below 300 °C.

Samples used in this study were (0001)-oriented n-type 6H-SiC epitaxial layer (net donor concentration: $1 \times 10^{16} \text{ cm}^{-3}$) grown on n-type substrate, which were provided from Cree Research. Figure 1 schematically illustrates a microwave-equipment used in this study, in which the introduced gas is discharged by microwave from 2.45 GHz magnetron at a power of 500 W. After a sacrificial oxidation and HF treatment of sample, the O₂-plasma oxidation was carried out with a O₂ flow of 0.4 sccm and Ar flow of 5.6 sccm at a pressure of 100 mTorr. In order to estimate the temperature dependence of oxidation rate, the temperature of samples were ranged from 100 to 300 °C. The composition of the growth layer was evaluated by using X-ray photoemission electron spectroscopy (XPS) with Mg K α X-ray. The thickness of grown layer was evaluated by means of ellipsometry.

Figure 2 shows XPS spectra of Si2*p*, C1*s*, and O1*s* electrons taken from the Si-face sample, which was processed for 20 min at the temperature of 200 °C. The binding energies of Si 2*p* and O 1*s* in the growth layer were evaluated to be 103 and 532 eV, respectively. The obtained binding energies of Si 2*p* and O 1*s* in the grown layer are identical to those of the thermally oxidized layer of SiC. It is concluded that the growth of SiO₂ layer on SiC can be achieved by O₂ plasma processing at 200 °C. Also, it should be noted that there are no singles attributed to C atoms in the plasma-grown SiO₂ layer. At the surface, the binding energies of Si and O may be influenced by C contaminations. At the interface, the binding energies of Si 2*p* and C 1*s* are lower than those in SiC. Since the binding energies of Si 2*p* and C 1*s* correspond to those of Si crystal and graphite, respectively, it is suggested that the dissociation of SiC at the interface between SiO₂ and SiC is caused during the plasma oxidation.

Figure 3 shows the oxide thickness as function of the oxidation time. The oxidation rate for the dry thermal oxidation at 1150 °C for Si-face of 6H-SiC is also shown. For the Si-face sample, SiO₂ layer with a thickness of 74 nm was obtained after the plasma oxidation for 20 min, while that for the thermal oxidation was evaluated to be 2 nm for Si-face of 6H-SiC. Furthermore, the oxide thickness for C-face is thicker than that of the case of Si-face. The larger oxidation rate of C face than Si-face in O₂ plasma oxidation is similar to the case of the thermal oxidation of (0001)-oriented SiC. The oxidation time dependences of the oxide thickness for Si- and C-face show the slope of 1.5 and 0.72 below 30 min and 0.4 and 0.2 above 30 min, respectively, while the slope of thermal oxidation is estimated to be 1.0. For the plasma oxidation of C-face SiC sample, the obtained slopes are in good agreement with

those in the case of Si. The initial growth with a slope of 0.72 is connected to both Si-SiO₂ interface reaction controlled and diffusion controlled in the SiO₂ layer, while the growth with a slope of 0.2 has been correlated to the Cabrera-Mott model [1]. The plasma oxidation of Si-face SiC sample shows 2 times larger slopes than the case of C-face. It is suggested that the unknown phenomena are involved in the plasma oxidation of Si-face. The activation energy of the plasma oxidation of 6H-SiC was estimated to be about 0.04 eV for both Si- and C-face in the temperature range from 100 to 300 °C. The low activation energy indicates that the plasma oxidation is dominantly activated by O₂ plasma processing of SiC.

In summary, the low-temperature oxide growth on 6H-SiC was observed at extremely low temperature of 200 °C with the much faster growth rate, as compared to the case of the thermal oxidation at 1150 °C, which is useful to the rapid oxidation of SiC at low temperature. [1] Y. Kawai, N. Konishi, J. Watanabe, and T. Ohmi, Appl. Phys. Lett. 64, 2223(1994).

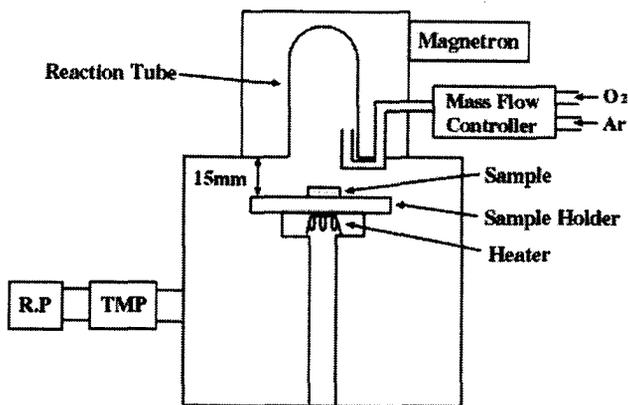


Fig. 1

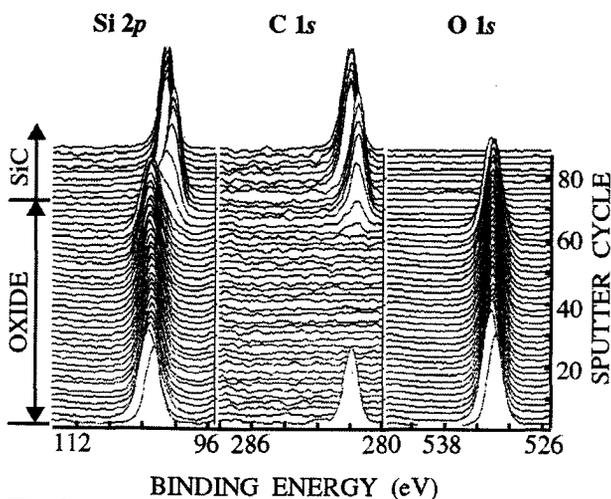


Fig. 2

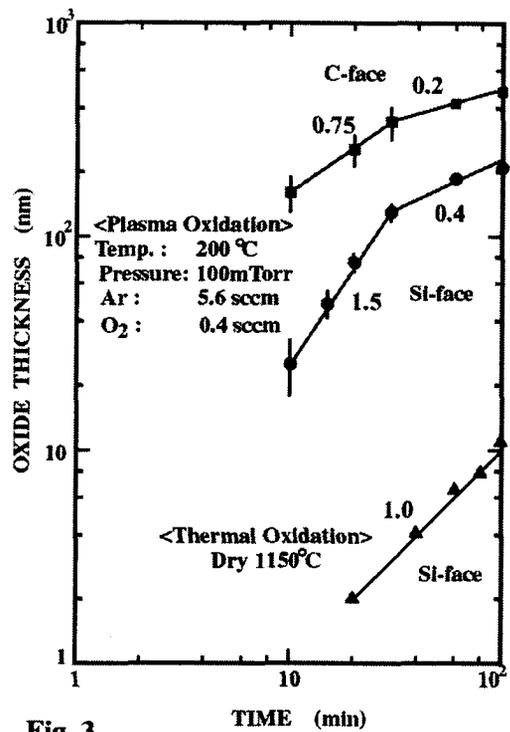


Fig. 3

4H-SiC ACCUEFT with stacked gate oxide consisting of two layers

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Channel mobility in 4H-SiC MOSFETs is rather low regardless of the high bulk mobility. One cause of low channel mobility is attributed to the capturing of carrier electrons by the many interface traps that are present in 4H-SiC MOS structures [1]. This paper describes an effective way to reduce interface state density, D_{it} , using a stacked gate oxide having two layers. Improved channel mobility has been achieved with this stacked gate oxide.

Figure 1 shows a dependence of D_{it} on the thickness of thermally grown oxide. The D_{it} distribution as a function of energy from the conduction band was measured with the high-low CV method. A 4H-SiC (0001) n-type epi-wafer ($N_d = 3 \times 10^{16} \text{ cm}^{-3}$) was used and the thermal oxide was grown at 1100 °C. It is seen that D_{it} in the SiO₂/4H-SiC interface increased as the thermal oxide became thicker. Figure 2 shows a comparison of D_{it} between samples using either the thermal oxide or the stacked gate oxide. The stacked gate oxide was created in a three-step process. First, a high quality thermally grown oxide was formed to a thickness of about 20 nm. Then an additional 30 nm of non-doped silicate glass (NSG) was deposited by CVD. The stacked oxide was then annealed at 1000°C for 30 minutes in a H₂ or N₂ atmosphere. The highest D_{it} value was observed near the conduction band edge of the sample with the 50-nm-thick thermal oxide. N₂ annealing was more effective for reducing D_{it} of the stacked oxide than H₂ annealing and the lowest D_{it} value was obtained from the stacked oxide that was N₂ annealed at 1000 °C for 30 minutes.

Planar 4H-SiC accumulation-mode MOSFETs (ACCUFET) with a thermally grown oxide or a stacked oxide were fabricated on p-type epi-layers ($N_a = 3 \times 10^{16} \text{ cm}^{-3}$) grown on n-type (0001) Si-face substrates. Figure 3 shows a cross sectional view of the ACCUFET. The channel length and width were 3 and 100 μm , respectively. Source and drain regions were formed by phosphorous ion implantation and nitrogen was implanted in the channel region at 800 °C with a total dose of $2.2 \times 10^{12} \text{ cm}^{-2}$. The regions were activated at 1600 °C for 20 minutes in Ar. The thermally grown oxide was formed at 1100 °C to a thickness of 50 nm. The stacked gate oxide consisted of a 20-nm-thick thermal oxide and 30-nm-thick NSG. The sample with the stacked oxide was then annealed at 1000 °C for 30 minutes in N₂. The ohmic contacts for the source and drain were Ti/Al and the gate electrode was poly-Si.

Figure 4 shows the $I_D - V_D$ characteristics of the ACCUFET with the stacked gate oxide. The accumulation layer channel mobilities (μ_{FE}) of the samples were calculated with Eq. (1) and plotted with the gate voltage in Figure 5.

$$\mu_{FE} = G_m \cdot Lg / (W \cdot C_{ox} \cdot V_d) \quad \text{at } V_d = 0.1 \text{ V} \quad (1)$$

Higher channel mobility of 35 cm²/Vs was obtained using the stacked gate oxide compared with 21cm²/Vs for the thermal oxide only. V_{th} of the stacked oxide ACCUFET was 0.3 V, while that of the thermal oxide ACCUFET was 1.0 V. This indicates that more negative charges existed in the MOS structure with the thermal oxide only than with the stacked oxide. These negative charges may have been electrons captured by acceptor-like interface traps. Since 4H-SiC ACCUFETs with a stacked gate oxide have lower density of electron traps, they can achieve higher channel mobility than ACCUFETs with a thermal oxide only.

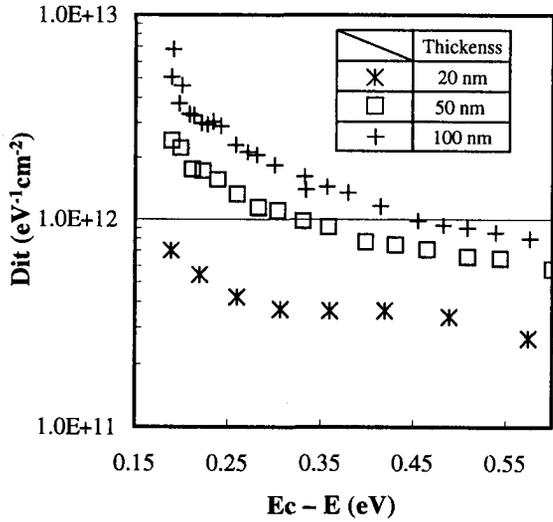


Fig. 1. Dependence of D_{it} on the thickness of thermally grown oxide

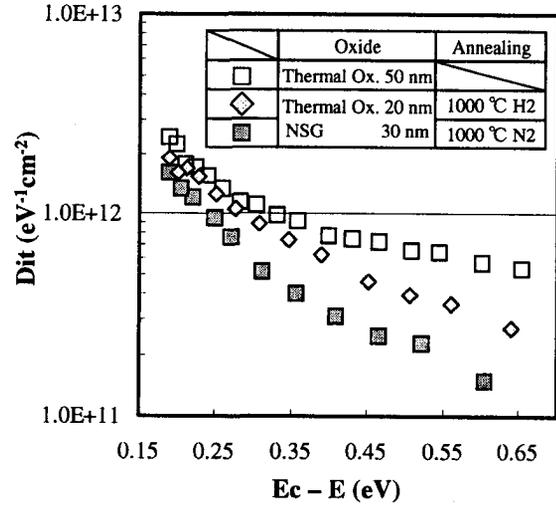


Fig. 2. D_{it} for samples with thermally grown oxide or stacked gate oxide

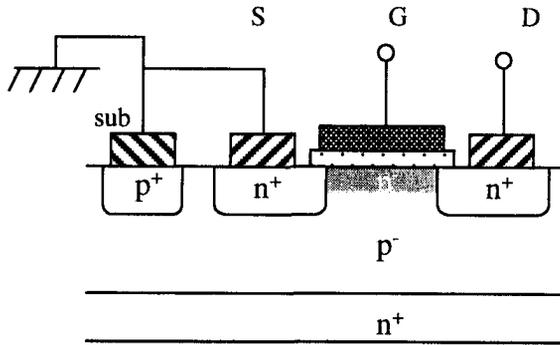


Fig. 3. Cross section of 4H-SiC ACCUFET

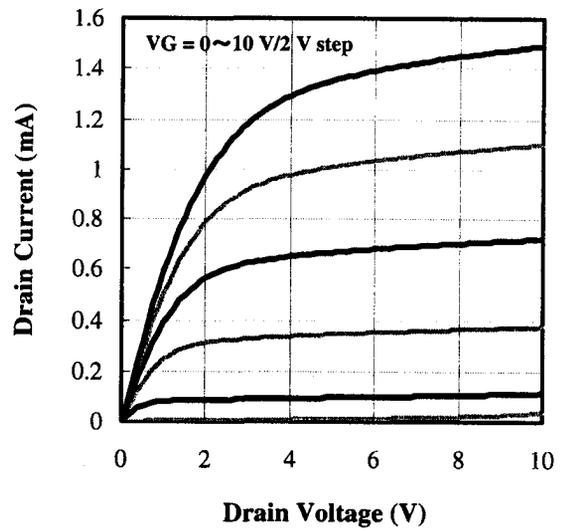


Fig. 4. I_D - V_D characteristics of 4H-SiC ACCUFET with stacked gate oxide

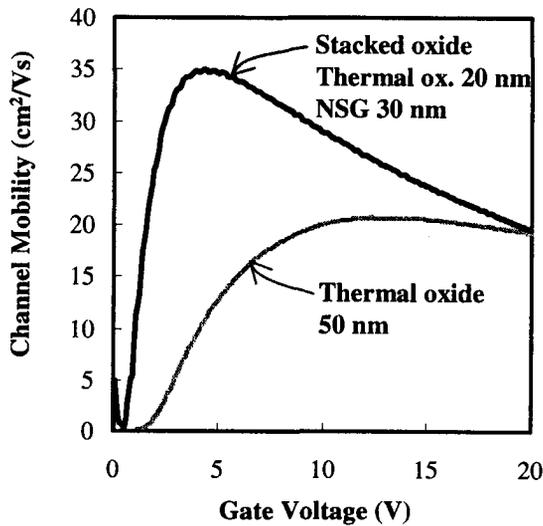


Fig. 5. μ_{FE} of 4H-SiC ACCUFET with thermal oxide or stacked oxide

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Correlation between inversion channel mobility and interface traps near the conduction band in SiC MOSFETs

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SiC MOSFETs are attractive switching devices in high-power and high-temperature electronic field. However, poor inversion mobility in the n -channel SiC MOSFETs is a serious problem especially in the 4H polytype. Several groups have reported that channel mobility is affected by an anomalously high interface trap density (D_{it}) near the conduction band edge (E_c). In this work, we evaluated the D_{it} near E_c by making capacitance-voltage (C - V) measurements for gate-controlled diodes (GCDs)[1]. Measurements of GCDs can be performed with MOSFETs, it makes possible a direct characterization between the interface traps and MOSFET channel mobility.

N -channel MOSFETs were fabricated on p^+ substrates with either a p -type 4H- or 6H-SiC homo-epitaxial layer (Si-face, $N_A-N_D \sim 5 \times 10^{15}/\text{cm}^3$), purchased from CREE Research. Source and drain regions were formed by phosphorous ion implantation. A gate oxide 40 ± 2 nm thick was grown at 1200°C in dry or wet O_2 . Post-oxidation annealing was performed for some samples in pure hydrogen at 800°C for 30 min (H_2 POA) [2] or in wet oxidation ambient at 950°C for 180 min (wet re-oxidation annealing; wet ROA) [3]. The μ_{fe} values for the MOSFETs prepared using various gate-oxidation procedures are summarized in Table I. The data listed there are the average values for 30 MOSFETs prepared on the same wafer. The wet ROA treatment improved the μ_{fe} much more than H_2 POA.

The C - V measurement of the GCDs was performed with a frequency of 20 Hz at room temperature. N^+ source and drain regions were tied to the p -type substrates during the measurements. As in the operation of n -channel SiC MOSFETs, the minority carriers were available from the adjacent n^+ regions. Typical C - V property for the 4H-SiC GCD with the dry-oxidized gate oxide is shown in Fig.1. This curve show a clear accumulation and inversion property with some peculiar structures similar to those in the curves reported in Ref.4, where the "hook and ledge" feature of the curves was attributed to the charge trapping in the interface states. Occurrence of the strong inversion at the SiC surface is shifted from point B to C due to the existence of the deep interface traps, the surface potential $\Psi_S = 2\Psi_B$ at point C (Ψ_B : bulk Fermi potential).

Here we define the difference between the gate voltages at C and D as V_{C-D} , where the capacitance at point D is equal to the flat band capacitance. The surface Fermi level moves toward the conduction band edge as increasing the gate voltage from point C to D. The values of the $E_c - E_F$ at the SiC surface were calculated to be about 0.2 and 0.1 eV at point C and D, respectively. The interface trap density N_{it} within the energy range of $E_c - E - 0.1 - 0.2$ eV can be estimated from $N_{it} = C_{ox} \times \Delta V_{C-D} / q$, where ΔV_{C-D} is the difference of the V_{C-D} between the experimental and theoretical value, C_{ox} is the oxide capacitance per unit area and q is electronic charge.

The values of N_{it} were calculated for all the devices whose μ_{fe} values are listed in Table I, and the normalized channel mobility μ_{fe}/μ_{bulk} of the MOSFETs is plotted in Fig.2 as a function of N_{it} . The values of the μ_{bulk} used for the normalization were $800 \text{ cm}^2/\text{Vs}$ for 4H and $400 \text{ cm}^2/\text{Vs}$ for 6H. A close correlation between the channel mobility and shallow trap

density is clear in this figure. The μ_{fe}/μ_{bulk} of the MOSFETs is rapidly reduced as increasing N_{it} independent on the polytype and the preparation procedures. Therefore, this correlation strongly indicates that the significant cause of the low inversion channel mobility of SiC MOSFETs is the high density of shallow traps between the E_c and the surface Fermi level at strong inversion. Our results are further evidence that the degraded channel mobility is caused by the reduction of the free carrier density due to the charge trapping in the shallow traps and the consequent Coulomb scattering by the negatively charged traps[5].

This work was performed under the management of FED as a part of the METI New Sun Shine Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

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Table I. The field effect mobility μ_{fe} in 4H- and 6H-SiC MOSFETs with different gate-oxide preparation procedures.

Oxidation	Post annealing	μ_{fe} (cm ² /Vs)	
		4H	6H
Dry	None	6.2	38.5
	H ₂ POA	7.4	38.3
	Wet ROA	24.8	76.3
Wet	None	5.6	34.7
	H ₂ POA	6.1	
	Wet ROA	15	52.2

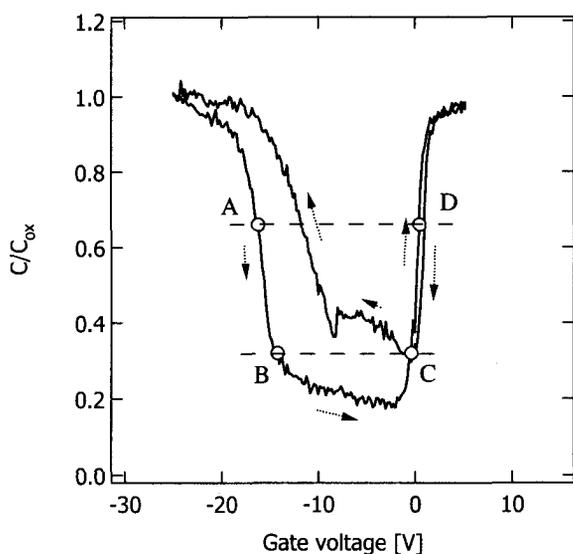


Fig.1. C-V curves obtained at room temperature for a 4H-SiC GCD with a dry-oxidized gate oxide.

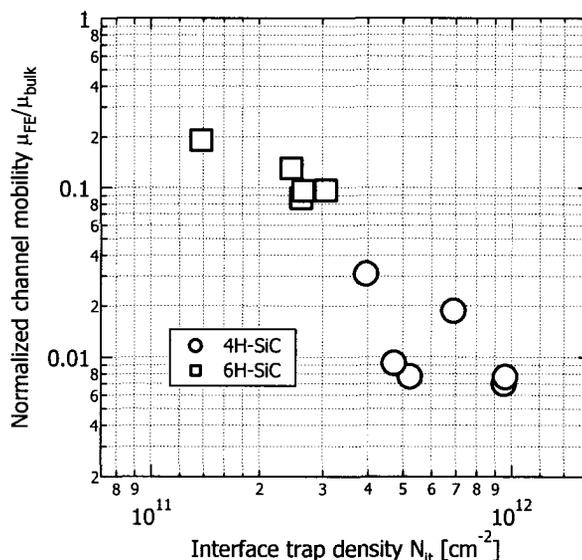


Fig.2. Normalized channel mobility μ_{fe}/μ_{bulk} of the 4H- and 6H-SiC MOSFETs plotted as a function of N_{it} .

LOW TEMPERATURE THERMAL OXIDATION OF ION AMORPHIZED 6H-SiC

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In this work the wet thermal oxidation of ion amorphised 6H-SiC was studied at temperature lower than 1100°C. The Rutherford Back-Scattering technique in the Channeling geometry was used to characterise the as-implanted and thermally treated samples. 6H-SiC on-axis and off-axis, p-type and n-type bulk substrates were ion implanted by Ar⁺ at fluence and energy values such to produce an amorphous surface layer less than 200 nm thick. These samples were thermally oxidised in a wet ambient for different temperatures and time intervals in the ranges 750-1100°C and 15 - 40 min, respectively. Some polycrystalline, mostly 3C-SiC, and crystalline 6H-SiC samples were also processed for comparison. Fig. 1 compares the oxide layer thickness grown for increasing temperature and fixed time (30 min) on samples ion amorphised, ion amorphised and re-crystallised, i.e. mostly polycrystalline 3C-SiC as described in [1], and crystalline 6H-SiC. For the amorphous samples two temperature intervals were identified: below and above 900°C, where the

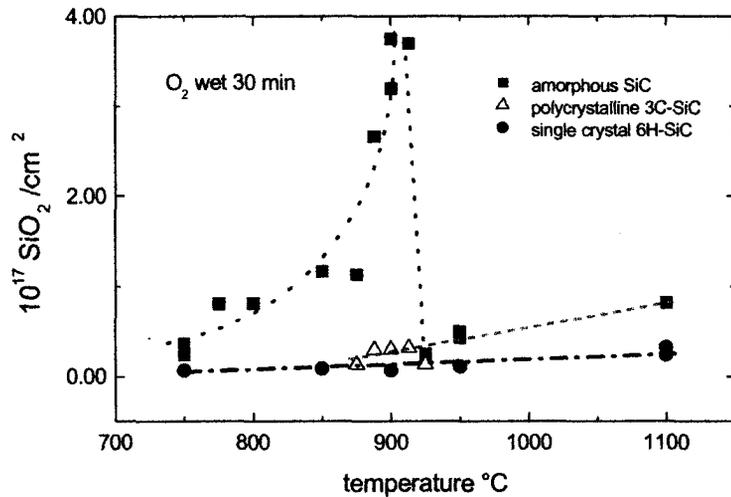


Fig. 1 Comparison among the oxidation of amorphous, polycrystalline and single crystal SiC for different annealing temperatures and constant annealing time. The rich oxygen ambient is wet.

oxidation rate were, respectively, fast and slow. The comparison with the reference samples shows that the trend above 900°C fits that of the polycrystalline samples, while below 900°C it is much higher. Over all the temperature range the 6H-SiC phase showed the lower oxidation rate. The data about the ion amorphised samples were independent on substrate type and orientation.

The hypothesis of an epitaxial regrowth of the ion amorphised 6H-SiC at a temperature as low as 900°C can explain the trend of Fig. 1. In fact, the drop of the oxidation rate at 912°C may be due to the touch between a polycrystalline regrowth front and on oxide one. The analysis of samples oxidised at 900°C for different time confirmed such hypothesis.

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Study of Surface Morphology and Chemistry of 4H- and 6H-SiC After Cyclic Oxidation

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Abstract

In-depth Atomic Force Microscope (AFM) and X-ray Photoelectron Spectroscopy (XPS) studies were performed on the surface morphology and chemistry of heavily doped n-type 6H- and 4H-SiC epilayers after cyclic dry oxidation and oxide removal in 49% HF, and pirhana clean (p-clean). The objective was to determine the fundamental differences and changes on the surface morphology and chemistry between the two polytypes after similar oxidation and oxide stripping processes. The goal of this oxidation study was to identify the optimum surface quality that would support improved homogeneous electrical contact interface characteristics across the wafer. The result shows that the progression toward smoother surface morphology is tracked by the disappearance of C 1s binding energy spectral peaks due to adventitious carbon and related compounds.

AFM scans of 1 cm² samples measured at five locations showed the 6H-SiC roughness to average RMS = 0.58 nm (Fig. 1a), followed by an of average RMS = 0.54 nm (Fig. 1b) after the first four-hour 1150°C dry oxidation/HF strip/p-clean. The second five-hour oxidation/HF strip/p-clean had an average of RMS = 0.4 nm (Fig. 1c). For the 4H-SiC, the as-received sample had an average roughness of RMS= 0.39 nm (Fig. 2a), and after the first oxidation/HF strip/p-clean the average was RMS=0.26 nm (Fig. 2b). The roughness after the second oxidation/HF strip/p-clean was measured as 0.31 nm (Fig. 2c).

The XPS survey spectra of the chemical species on the surface of both polytypes after each process cycle are shown in Figs. 3a and b. The as-received samples show up to 2.5 at. % chlorine (origin unknown) present on the surface. The chlorine concentration dropped below detection limits (0.1%) after the first four-hour oxidation/HF strip/p-clean. In the C 1s spectra of both the as-received 6H- and 4H-SiC shown in Figs. 4a and b, respectively, additional C 1s peaks at higher binding energies can be seen in addition to the primary carbide peak at 282.7 eV. After the first four-hour oxidation/HF strip/p-clean, the XPS C 1s spectrum of the 6H-SiC polytype still shows adventitious carbon as a higher binding energy shoulder while the C 1s spectrum of the 4H-SiC, on the other hand, shows a much cleaner carbide peak with minimal shoulder. The result in 6H-SiC was reproduced in three different sample sets. After the second oxidation/HF strip/p-clean, the three 6H-SiC sample sets looked more like the single carbide peak observed in 4H-SiC after only one oxidation.

It is not clear at the moment why the 6H-SiC samples required two oxidations and 49%HF stripping cycles to stabilize its surface (i.e. eliminate the extra C 1s shoulder) while the 4H-SiC required only one. It is worth noting that after the first oxidation, the 4H-SiC achieved a surface roughness equivalent to a Si-C bilayer step height (0.25 nm) while 6H-SiC has an average roughness equivalent to about a two Si-C bilayer step height. Reaction kinetics are known to be surface area driven¹. In this particular experiment, the 4H-SiC will offer less area for adventitious reactions to take place after the first oxidation cycle. We will discuss these issues in broader terms within the context of relationships between surface morphology, surface chemistry, and the observed orientation dependency of specie concentration.

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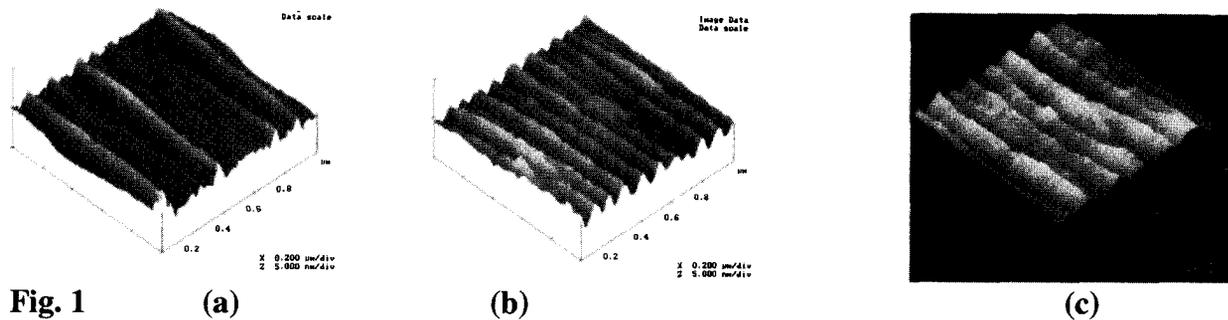


Fig. 1

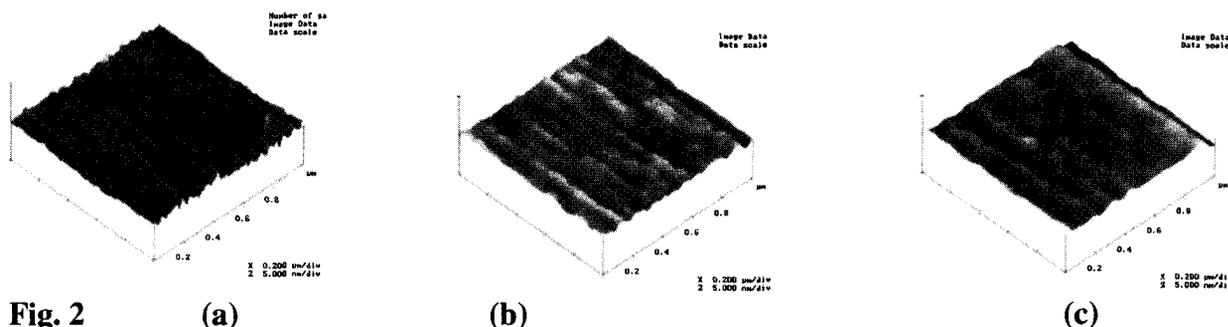


Fig. 2

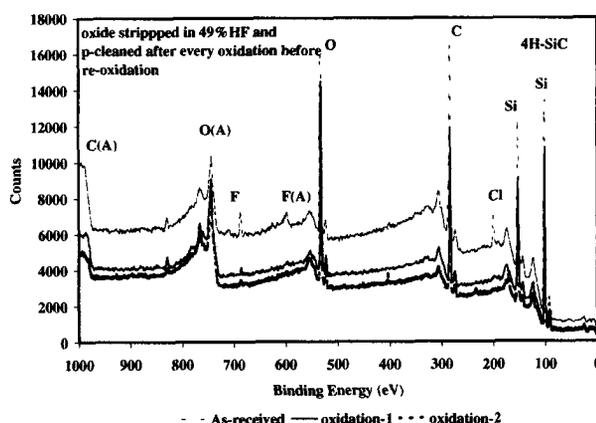
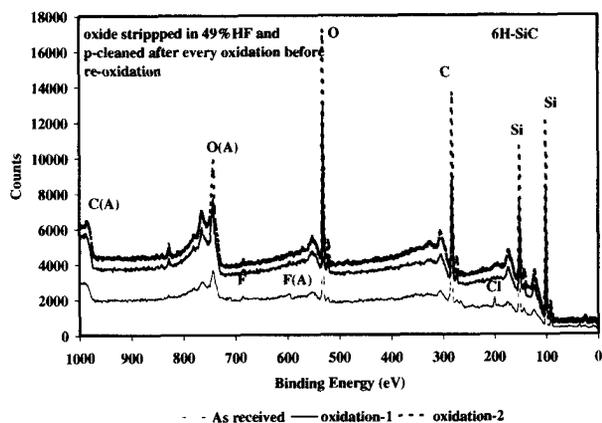


Fig. 3

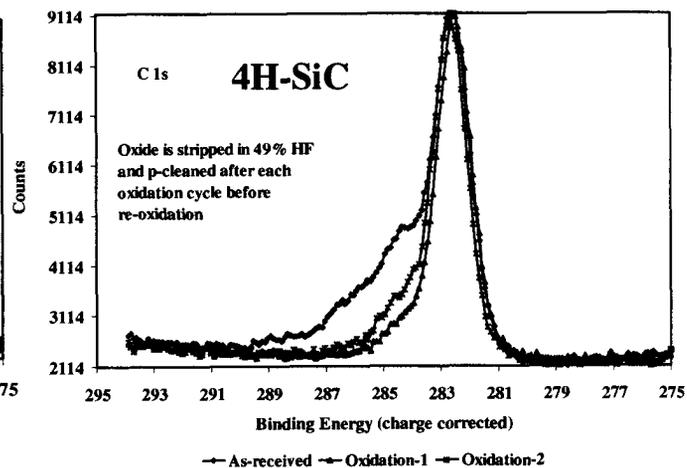
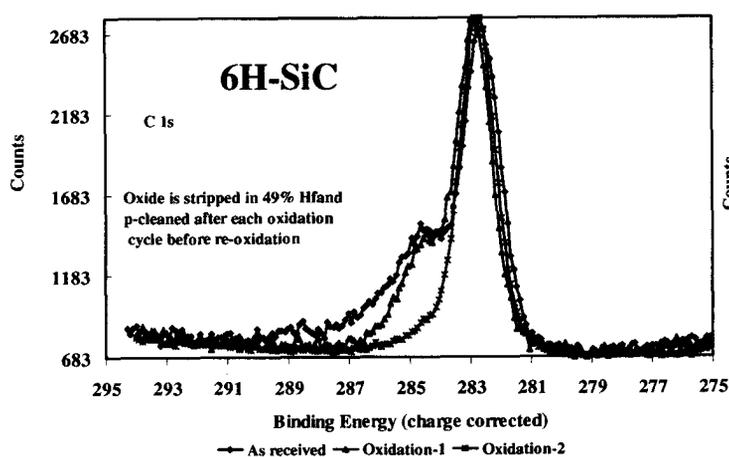


Fig. 4

Effects of successive annealing of oxides on electrical characteristics of SiC MOS structures

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Insulators on SiC are easily made by thermal oxidation process similar to the fabrication process of Si metal-oxide-semiconductor (MOS) technology. This is one of the most important characteristics of SiC for device applications. In order to realize SiC MOS devices with high performance specifications, it is important to fabricate the SiO₂/SiC interface with fine electrical properties. A few years ago, it was reported that the electrical characteristics of SiO₂/SiC interface are improved by the annealing in steam at 950°C for 3 hours (re-oxidation) [1]. However the re-oxidation is not optimized at present. In this conference, we propose the successive annealing of oxides in steam at different temperatures and report the decrease of interface defects in oxide layers of 4H-SiC MOS structures.

The 4H-SiC chips (5-mm in square) with epilayers were made by cutting from 2-in. n-type (0001) wafers purchased from Cree Research Inc. The substrates were boiled with acetone and sulfuric acid to degrease their surfaces, and then sacrifice oxidation was performed twice. Thereafter, pyrogenic oxidation was carried out at 1100°C for 1 hour to form gate oxide layers of approximately 25 nm in thickness. At the final stage of the oxidation, annealing in steam at 950°C for 3 hours was performed and that at 800°C for 3 hours was successively carried out (successive annealing in steam). The successive annealing profile is shown schematically in Fig.1.

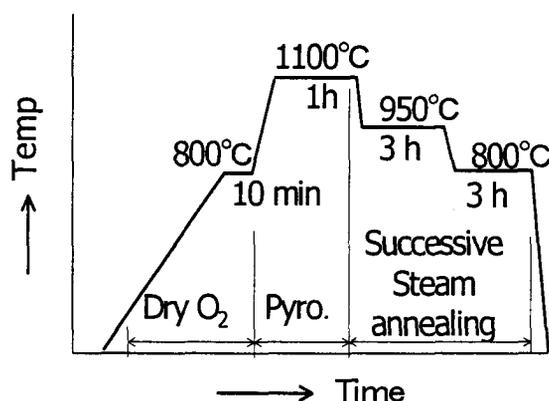


Fig.1 Successive annealing profile.

After the process, gold was deposited thermally on the oxide layers to form gate electrodes of 25 nm in thickness. To make an ohmic electrode, the oxide layers on the backside of substrates were removed and aluminum was evaporated on the bared surface of the substrates. The simultaneous *CV* (*SCV*) characteristics were measured for the 4H-SiC MOS structures to obtain the gate

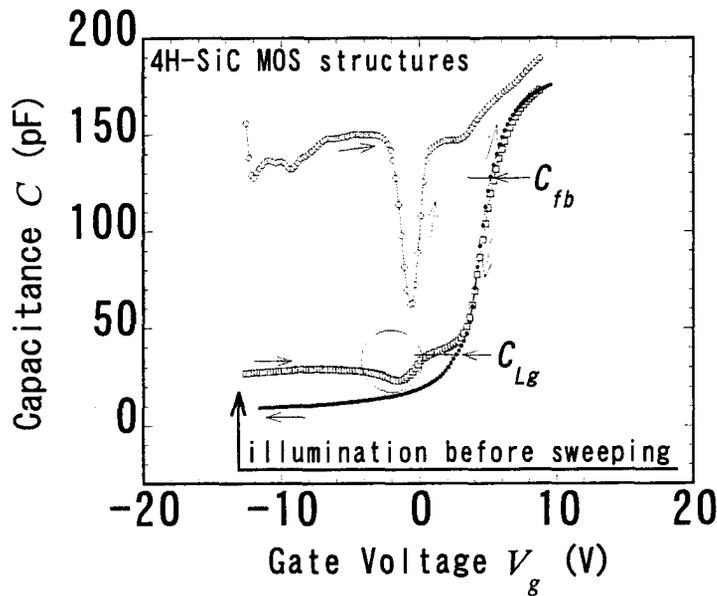


Fig.2 SCV characteristics of MOS structures on the Si face of a 4H-SiC substrate. The oxide layer is annealed in steam at 950°C for 3 hours and subsequently at 800°C for 3 hours. For SCV measurements, MOS structures were illuminated with a low-pressure mercury lamp to induce an inversion layer before sweeping the gate voltage.

The notations C_{fb} and C_{Lg} indicate the capacitance values corresponding to the flat band condition and the ledge of the high-frequency CV curve swept from negative to positive gate voltage side, respectively. There is a split near the depletion region between the high-frequency CV curves. This indicates that the interface traps exist around the mid-gap region. The difference in gate voltages at C_{Lg} level is found to be about 1.8 V. The high-frequency CV curve obtained by illumination winds down near the ledge and the quasi-static CV curve has a narrow valley near the region. The winding curve means the minority carrier redistribution [2]. These suggest that the number of interface traps near the valence band edge is scarce. The narrow valley and the winding for the SCV characteristics were not observed for the sample annealed in steam at 950°C for 3 hours only. On account of the difference, the number of interface traps near the valence band edge can be concluded to decrease by the successive annealing in steam. The successive annealing is effective method for the fabrication of MOS structures with fine electrical property.

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voltage corresponding to flat band condition (V_{fb}) and the energy profile of interface trap density per unit area (D_{it}) near the conduction band edge. The CV curve swept rapidly from positive to negative gate voltage side was also measured for the same sample before and after the SCV measurements to calculate the net number of interface traps per unit area (N_{it}).

Figure 2 shows the SCV characteristics of MOS structures on the Si face of a 4H-SiC substrate, which is fabricated using the successive annealing in steam. The

Gamma-ray irradiation effects on the electrical characteristics of 6H-SiC MOSFETs with annealed gate-oxide

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Since silicon carbide (SiC) has a strong radiation resistance[1], it is expected to be applied to electronic devices used in harsh radiation environments such as space. In the development of radiation resistant devices based on SiC, it is both important to improve their electrical characteristics before irradiation and to understand the degradation of the electrical characteristics of SiC devices due to irradiation. Recently, we have demonstrated that the electrical characteristics of SiC MOSFETs are improved by hydrogen (H₂) or steam annealing of the gate oxide just after the oxidation process[2]. Since the radiation response of MOSFETs strongly depends on the fabrication process of gate oxide, we have studied the influence of γ -ray irradiation on the electrical characteristics of SiC MOSFETs of which gate oxide was formed with different post-oxidation annealing conditions.

The MOSFETs used in this study were fabricated on p-type 10 μm thick epitaxial 6H-SiC films grown on 6H-SiC substrates (3.5° off, Si-face). The net acceptor concentration of the epitaxial films ranges from 5×10^{15} to 1×10^{16} /cm³. The source and drain of the MOSFETs were formed using phosphorous ion implantation at 800 °C and subsequently annealed at 1500 °C for 20 min in an Ar atmosphere. The gate oxide was fabricated by pyrogenic oxidation (H₂:O₂ = 1:1) at 1100 °C for 60 min. Steam annealing for the gate oxide was carried out at 800 °C for 30 min in the same ambient as the pyrogenic oxidation. Hydrogen annealing was carried out at 700 °C for 30 min at a pressure of 20 Torr. The thickness of the gate oxide was determined by *C-V* measurements. The gate length and width of the MOSFETs are 10 μm and 200 μm , respectively. Gamma-ray irradiation was performed up to 530 kGy (SiO₂) at a rate of 8.8 kGy/h at room temperature (RT). During the irradiation, no electrical bias was applied to the gate, the drain and the source of the MOSFETs. The electrical characteristics were measured at RT under dark conditions. The channel mobility (μ) of the MOSFETs was derived based on the following procedures: First, the values of μ were estimated from the linear region of the drain current (I_D) versus drain voltage (V_D) curves in various gate voltage (V_G). Then, the best value obtained from the V_G dependence of μ was used as the value of μ in this study. The threshold voltage (V_T) was determined as the value at the intersection between the V_G axis and the line extrapolated from the curve of the square root of the drain current (I_D). Here, SiC MOSFETs with H₂-annealed gate oxides and steam-annealed gate oxide are referred to as SiC(H₂) MOSFETs and SiC(H₂O) MOSFETs.

Figure 1 shows the absorbed dose dependence of μ for SiC(H₂O) and SiC(H₂) MOSFETs. The value of μ in the un-irradiated SiC MOSFET fabricated without post-

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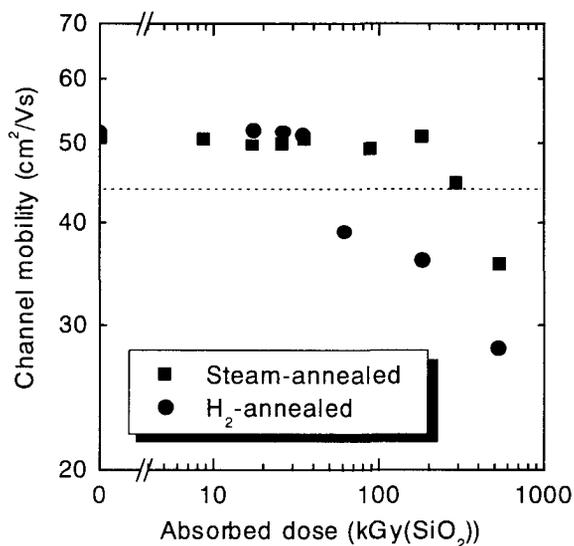


Fig. 1 Absorbed dose dependence of channel mobility for SiC(H₂O) and SiC(H₂) MOSFETs. The value of channel mobility for un-annealed SiC MOSFETs before irradiation is also indicated as the broken line.

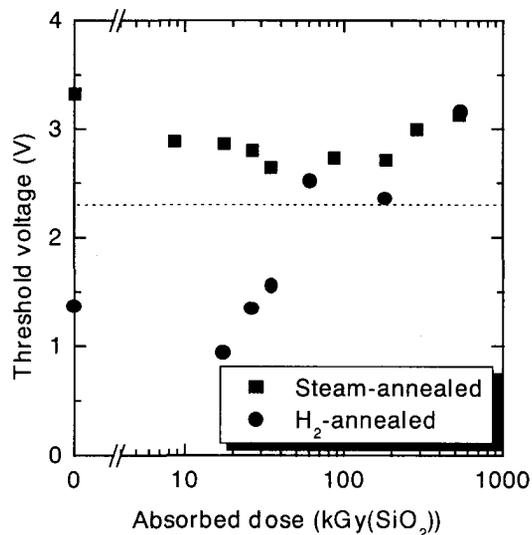


Fig. 2 Absorbed dose dependence of threshold voltage for SiC(H₂O) and SiC(H₂) MOSFETs. The value of threshold voltage for un-annealed SiC MOSFETs before irradiation is also shown as the broken line.

oxidation annealing (un-annealed SiC MOSFETs) is also shown as the broken line. Before irradiation, μ for both SiC(H₂) and SiC(H₂O) MOSFETs was 52 cm²/Vs. As for SiC(H₂) MOSFETs, the value of μ decreases at doses above 60 kGy(SiO₂), and becomes 28 cm²/Vs at 530 kGy(SiO₂). On the other hand, μ for SiC(H₂O) MOSFETs is not changed up to 200 kGy, and at 530 kGy, the value of μ is 35 cm²/Vs.

Figure 2 shows the absorbed dose dependence of V_T for SiC(H₂O) and SiC(H₂) MOSFETs. The value of V_T for SiC(H₂) MOSFETs decreases slightly at 17 kGy, and increases with increasing absorbed dose above 17 kGy. The change of V_T by irradiation up to 530 kGy is 2.2 V (from 0.9 to 3.1 V). With respect to SiC(H₂O) MOSFETs, V_T decreases slightly with increasing absorbed dose below 34 kGy, and slightly increases with increasing absorbed dose once above 87 kGy. The change of V_T by irradiation is only within 0.6 V (2.7 to 3.3 V). For the radiation resistant devices, the stability of their electrical characteristics such as V_T under irradiation is very important. Thus, our results suggested that the radiation resistance of SiC(H₂O) MOSFETs is higher than that of SiC(H₂) MOSFETs.

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A large reduction of interface-state density for MOS capacitor on 4H-SiC (11 $\bar{2}$ 0) face using H₂ and H₂O vapor atmosphere post-oxidation annealing

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SiC MOSFETs are expected as switching devices because of its high-speed ability. The field-effect channel mobility (μ_{FE}) of 4H-SiC MOSFETs is predicted to be higher than that of 6H-SiC because of higher bulk Hall mobility of 4H-SiC. However, actual μ_{FE} of 4H-SiC MOSFETs is much lower than that of 6H-SiC MOSFETs, which is originated from higher interface state density (D_{it}) at SiO₂/4H-SiC interface. Yano et al. reported the effective mobility as high as 30cm²/Vs for 4H-SiC MOSFETs on (11 $\bar{2}$ 0) face [1]. However, this value is not sufficient for the reduction of on-resistance (R_{on}) of 4H-SiC power MOSFETs with the relatively low blocking-voltage below 1kV. In this work, we have researched the effect of oxidation method and post-oxidation annealing (POA) on the D_{it} of MOS capacitor formed on 4H-SiC (11 $\bar{2}$ 0) face.

N-type 4H-SiC (11 $\bar{2}$ 0) bulk substrates were purchased from Cree Research Inc. The three n-type epitaxial layers were grown on bulk substrates. The thickness and effective carrier density ($N_d - N_a$) of bottom layer are 1.5 μ m and 1 \times 10¹⁸ cm⁻³. Those of middle layer are 0.5 μ m and 1 \times 10¹⁷ cm⁻³. Those of top layer are 0.1 μ m and 5 \times 10¹⁵ cm⁻³, respectively. The RCA cleaning was carried out. Next, a sacrificial oxide of 10nm thickness was grown, and then it was removed with 5% HF solution. Oxide films were thermally grown at 1150°C in dry O₂ (dry oxidation, samples (a),(c) and (e)), and in H₂O vapor atmosphere (wet oxidation, samples (b),(d) and (f)). The thickness of the oxide film was 50 \pm 5nm. After both oxidations, all samples were annealed in argon for 30 min at 1150°C. In addition, the samples (c) and (d) were annealed in H₂ at 800°C for 30 min. The samples (e) and (f) were annealed in H₂O vapor atmosphere at 750°C for 3 h. Aluminum on the top of the oxide films and on the back of the samples was evaporated to make gate electrodes and ohmic contacts, respectively. The D_{it} estimations were performed using high-low technique and a KI82 system.

Figures 1 and 2 show the D_{it} distributions of the samples (a)~(f). The D_{it} of the sample on (0001) face with dry or wet oxidation following Ar annealing at 1200°C are also shown for comparison. In the case of samples with the dry oxidation, the D_{it} of sample(a) on (11 $\bar{2}$ 0) face with only Ar annealing is much higher than that of sample on (0001) face. This suggests that the μ_{FE} of 4H-SiC MOSFETs on (11 $\bar{2}$ 0) would be lower than that of 4H-SiC MOSFETs on (0001) face. As shown in sample(c), the H₂ POA decreases the D_{it} in the shallow level from the conduction band edge (E_c). The D_{it} becomes the same value as that of (0001) face

near $E_c - E = 0.2\text{eV}$. However, at the $E_c - E = 0.6\text{eV}$, the D_{it} is one order of magnitude higher than that of sample on the (0001) face. The H_2O POA decreases the D_{it} in the energy level from 0.2eV to 0.6eV (sample(e)), which results in the almost same value as that of (0001) face. Hence, it is considered that the H_2O POA much improves the μ_{FE} of sample with the dry oxidation. On the other hand, in the case of samples(b),(d) and (f) with the wet oxidation, the D_{it} in $E_c - E < 0.3\text{eV}$ is much lower than that sample on the (0001) face. This is the reason why the μ_{FE} of 4H-SiC MOSFETs on (11 $\bar{2}$ 0) face with the wet oxidation is higher than that on (0001) face as reported by Yano et al. The H_2O POA reduces the D_{it} in the energy level from 0.2eV to 0.6eV (sample (f)). Moreover, H_2 POA reduces the D_{it} in the energy level deeper than 0.35eV (sample(d)). This means the H_2 POA much improves the μ_{FE} of MOSFETs on (11 $\bar{2}$ 0) face. Indeed, we found that the μ_{FE} reached $110\text{cm}^2/\text{Vs}$ using the wet oxidation and H_2 POA technique[2]. Therefore, both the wet oxidation and H_2 POA technique is excellent for the gate-oxide formation process of 4H-SiC MOSFETs on (11 $\bar{2}$ 0) face.

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Acknowledgement

This work was performed under the management of FED as a part of the METI NSS Program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

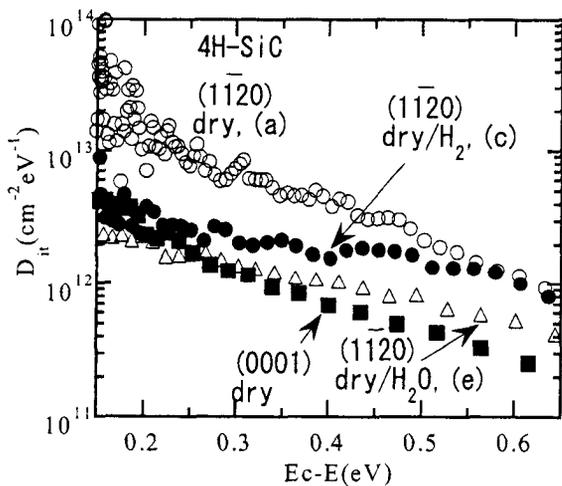


Fig. 1 Effect of POA on D_{it} distribution of samples with the dry oxidation.

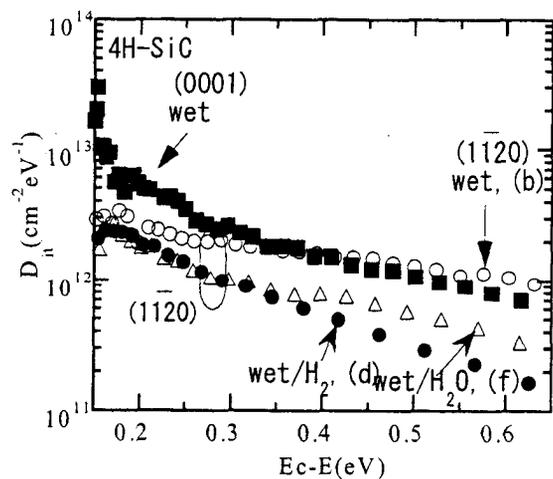


Fig. 2 Effect of POA on D_{it} distribution of samples with the wet oxidation.

Influence of the wet re-oxidation procedure on inversion mobility of 4H-SiC MOSFETsR. Kosugi^{1,2}, M. Okamoto^{1,2}, S. Suzuki^{2,3}, J. Senzaki^{1,2}, S. Harada^{1,2}, K. Fukuda^{1,2}
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SiC-based metal-oxide-semiconductor field effect transistor (MOSFET) is one of the candidates for high power and high frequency electric device applications, because SiC can be thermally oxidized to form a SiO₂/SiC structure. Among many SiC poly-types, recent interesting has shifted to the 4H- from 6H-SiC, because the former has higher electron mobility with its small anisotropy. However, the channel mobility of 4H-SiC(0001) based MOSFETs is far below the predicted value from 4H bulk electron mobility. It has been reported that a wet re-oxidation treatment after gate oxide formation is effective to improve the low channel mobility of 6H-SiC MOSFETs by several researchers¹. In this study, we applied the wet annealing treatment with various conditions to 4H-SiC(0001) MOSFETs and investigated the dependence of the MOSFET characteristics on those conditions.

N-channel MOSFETs were fabricated on the 8° off angled p-type 4H-SiC(0001) substrates with p-type epitaxial layer from Cree Research Inc. Effective doping density ($N_d - N_a$) of the epitaxial layer was about $5 \times 10^{15} \text{ cm}^{-3}$. The channel length and width were 100 and 150 μm , respectively. Source and drain were formed by phosphorous ion implantation and an activation annealing for the implanted layer was conducted at 1500°C for 5min. Gate oxide was formed at 1200°C for 140 min in dry O₂ ambient following a post oxidation annealing (POA) in Ar ambient at the same temperature. Wet re-oxidation annealing (wet ROA) was carried out after the Ar POA on various conditions, (a) at 950°C for 180 min, (b) at 850°C for 180 min, (c) at 1050°C for 180min, (d) at 950°C for 60 min. Al was evaporated as both the gate metal and the contact metal for source and drain. No contact annealing was done after the Al deposition.

Figure 1 shows typical drain current-voltage ($I_d - V_d$) characteristics of FET(a), where the gate voltage (V_g) changed between 0 to 12 V with 3 V steps. The $I_d - V_d$ characteristics exhibit good linear and saturation regime, and positive threshold voltage (V_{th}). This trend was observed for all FETs fabricated in this study (not shown here). A field-effect mobility (μ_{FE}) was calculated from the slop of the I_d versus V_g characteristics. Fig. 2 shows a typical μ_{FE} as a function of V_g at $V_d = 100\text{mV}$ for FET(a)-(d). The peak values of μ_{FE} depend extremely on the wet annealing conditions. That is, the μ_{FE} value increased critically on the FET(a) of 38 cm^2/Vs and no significant improvements were observed on the FETs(b)-(d) of

8-9 cm²/Vs compared with those of standard SiC MOSFETs. This dependence of the μ_{FE} was relevant to the measured effective charge density of the MOS capacitors formed on each test elemental group. The V_{th} was extracted from the intercept on V_g axis made by the tangent line of $I_d^{1/2}$ - V_g plot at $V_d=10V$. The average value of μ_{FE} , V_{th} and μ_{sat} was summarized on the table I. Thus, it was found that the wet ROA improved the channel mobility of 4H-SiC MOSFETs and the effects largely depend on the annealing conditions.

Another interest of this work is why the channel mobility increased by the wet ROA. Recently, it was reported that the wet ROA caused a conformational change in the structure of the SiO₂/SiC and resulted in converting the Si-Si transition layer into SiO₂ thereby shortening the transition region². To examine whether the effects of the wet ROA remain after the following annealing in inert gas ambient, Ar annealing at 1000°C for 30min was conducted after the wet ROA at 950°C for 180min. The peak value of μ_{FE} after the Ar annealing reduced approximately one-third of that for FET(a). This suggests the wet annealing treatment seems not to be irreversible effects such as the structural change as mentioned above and/or the removal of the interfacial carbon rich region³. We believe that the wet annealing causes some sort of inactive effect by -H and/or -OH termination and the effect was diminished by the following Ar annealing. This work was performed under the collaboration of AIST and FED as a part of the METI NSS program (R&D of Ultra-low-Loss Power Device Technologies) conducted by NEDO.

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Table I Summary of μ_{FE} , V_{th} and μ_{sat}

	μ_{FE} [cm ² /Vs]	V_{th} [V]	μ_{sat} [cm ² /Vs]
(a)	33.5	4.6	19.3
(b)	8.9	6.9	3.4
(c)	8.3	8.2	2.4
(d)	8.2	7.9	3.2

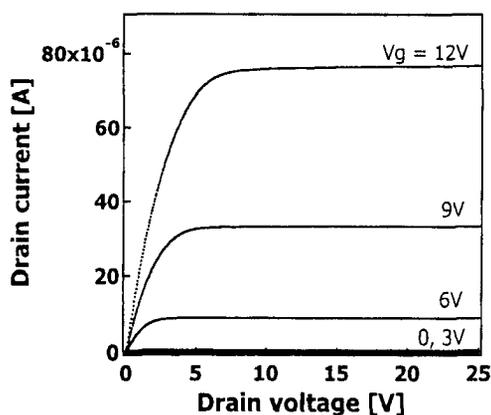


Fig. 1 Output characteristics of FET(a)

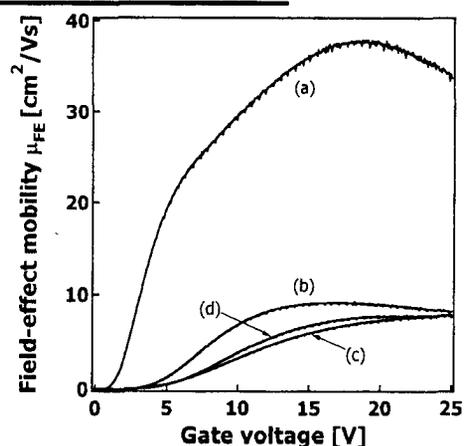


Fig. 2 Field-effect mobility for FETs(a)-(d)

Reduction of Interface Trap Density in 4H-SiC MOS by High-Temperature Oxidation

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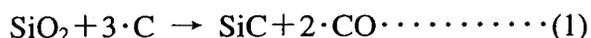
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4H-SiC semiconductor has the excellent physical characteristics for power-application devices. However, 4H-SiC MOSFET have never realized the ideal on-resistance performance because of the very low channel mobility. One of the origin for the low channel mobility is the high interface trap density, especially at the interface energy near the conduction band edge[1]. R.Schorner et al. reported that the residual carbon at MOS interface might make the interface trap density high [2].

In this paper, the reduction of the residual carbon and of the interface trap density have been realized by the thermal oxidation at high temperature (higher than 1200°C).

We reported that a carbonized layer on 4H-SiC Si-face, on which a thermal oxide layer on Si was located as face to face, can be reconstructed to SiC[3]. The carbonized layer was made by the Si sublimation in Ar ambience (50mTorr) at 1600°C. Gibbs free energy of the chemical equation(1) indicates that the carbon and the oxide should be SiC at high temperature(>1200°C) condition.



The reconstructed SiC should be made by the reaction between the carbon layer and the oxide. If the reconstruction velocity from carbon and SiO₂ to SiC is sufficiently larger than the generation velocity of the residual carbon, the generation of the residual carbon during the oxidation process should be vanished and the interface trap density will be reduced. So, we carried out the high temperature (>1200°C) oxidation.

We fabricated the MOS diodes for estimating the residual carbon and the interface trap density. 4H-SiC epitaxial wafers with (0001) Si face were prepared. The gate oxides were thermally grown in wet or dry O₂ ambience at 1080~1250°C. The oxide thickness is about 40nm. The gate electrodes and the back-side ohmic contacts are Al and Ni (annealed at 1000°C), respectively.

The residual carbon at MOS interfaces were analyzed by the low-take-off angle XPS method, after removing the oxides by HF. The low-take-off angle (≤ 15°) XPS method can estimate the binding energy of the atom at only the SiC surface(electrom escape depth ≤ 0.3nm). The residual carbon at the interface of the 1250°C dry oxide is 40% lower than the one of the 1080°C wet oxide.

Figure 1 shows the interface trap density (Dit). Dit was estimated from the Capacitance-Voltage measurements and Hi(100kHz)-Low method at RT. The voltage scanning rate of the C-V measurement was 0.1V/sec. It clearly shows that the Dit is more reduced as higher the oxidation temperature in both ambience, wet and dryO₂. However, the Dit in wet and dryO₂ ambience is different. It is not cleared why the phenomena took place, but we guess that the ratio between the reconstruction velocity and the the oxidation velocity might be different in the oxidation ambience because the oxidation velocity in wet ambience is much lager than the one in dryO₂ ambience.

In conclusion, the oxidation process at higher temperature than 1200°C reduce the residual carbon and the interface trap density(Dit). Especially, the Nit (which is integrated Dit between 1.0~1.4eV) of the oxide thermally grown at 1250°C(in dryO₂ ambience) is 60% reduced as compared to the one at 1080°C(in wet ambience).

[1]M.K.Das, B.S.Um, and Cooper,Jr, Materials Science Forum Vols.338-342, p1069 (2000)

[2]R.Schorner et al.,IEEE Electron Device Let., Vol.20, No.5, p241 (1999)

[3]E.Okuno et al.,Proc. of 9th Meeting on SiC and Related Wide Bandgap Semiconductors, p29 (2001), in Japanese

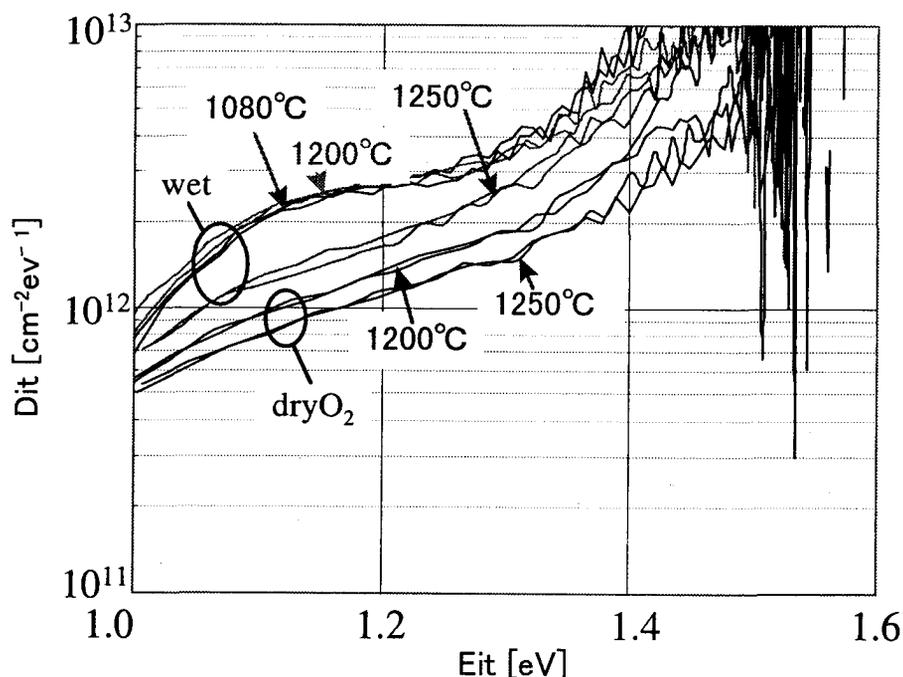


Figure 1 Interface Trap Density(Dit) dependence on Eit (Eit is the energy from Midgap)

INFLUENCE OF DEPOSITION PARAMETERS AND TEMPERATURE ON STRESS AND STRAIN OF IN-SITU DOPED PECVD SILICON CARBIDE

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Abstract

Thin films of silicon carbide (SiC) deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) technique are very attractive for IC-compatible MEMS as structural material and as coating layer. These amorphous films, although deposited at temperature lower than 400°C, maintain most of SiC excellent properties such as high mechanical strength, high thermal conductivity and extreme chemical inertness in several liquid electrolytes.

In this paper we present the influence of deposition parameters such as pressure, temperature, power, gas flow rate on stress and strain of in-situ doped and undoped PECVD SiC films. In fact the mechanical properties of the SiC films that are crucial for its application to MEMS, are affected strongly by the deposition parameters. The thickness of SiC films is measured by using spectroscopic ellipsometry. The density of these films depends on the deposition parameters and is calculated in range of 2mg/mm³ to 2.5mg/mm³. The values of the parameters investigated are varied in the range indicated in Table 1.

Both compressive and tensile stress films can be deposited. Stress values between - 700MPa and + 400MPa can be obtained. A shift from compressive toward the tensile region is observed for increasing SiH₄/CH₄ gas ratio (see Fig.1) and for increasing pressure. This tendency is reversed for increasing total RF power or its LF component. A strong change in stress is measured when doping gas is added or after an annealing cycle up to 650°C (see Fig.2). The influence of two commonly used substrates, thermal silicon oxide and PSG (phosphosilicate glass) on the stress of undoped and in-situ doped SiC is indicated in Fig.3.

The process flow schematically depicted in Fig.4 is used to release the rotating structure that is capable of measuring both compressive and tensile strain. The displacement of the pointer due to the strain is shown in Fig.5 for an undoped and a phosphorous-doped film. The study presented here allows us to establish the proper values for the deposition parameters to obtain as-deposited low-stress films for both undoped and p-or n-type SiC films.

Keyword: Silicon carbide, stress, strain, PECVD, IC compatibility

Table 1: Preparation condition of in-situ doped and undoped silicon carbide layers

Parameter	Value
Temperature	300°C ÷ 400°C
Pressure	1.5 ÷ 3 Torr
SiH ₄ flow	0.05 ÷ 0.25 slm
CH ₄ flow	fixed at 3 slm
PH ₃ flow	4% of total gas
B ₂ H ₆ flow	4% of total gas
Total power	600 ÷ 2500 watts
LF power	25%, 50%, 75%

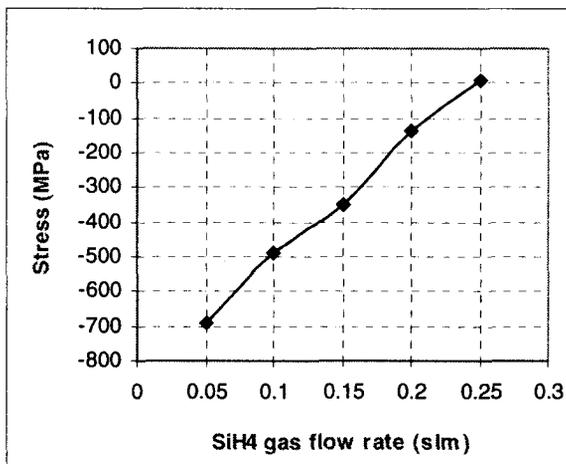


Fig. 1: Stress of silicon carbide as a function of SiH₄ flow rate.

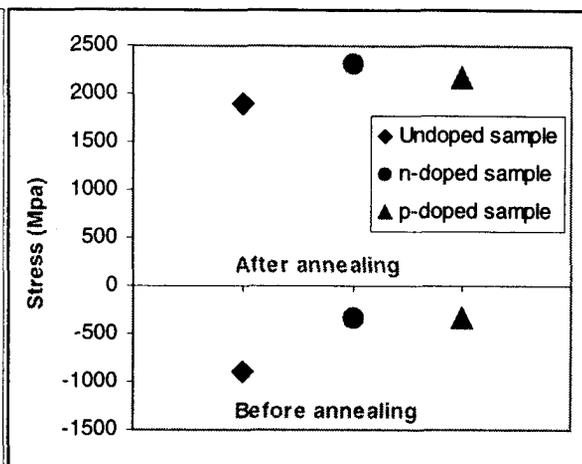


Fig. 2: Stress of undoped and doped silicon carbide before and after annealing

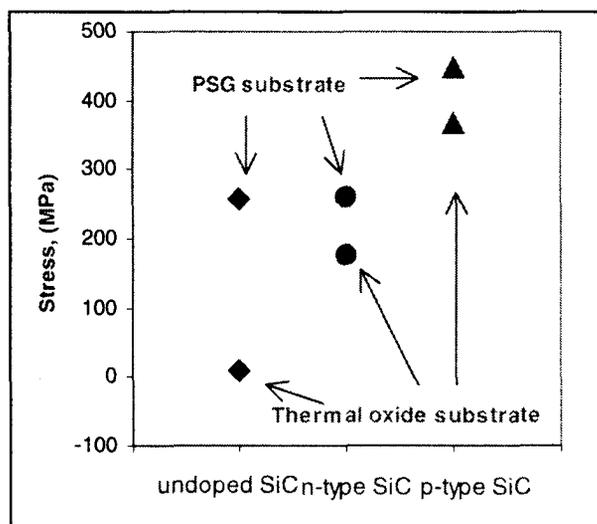


Fig. 3: Stress of undoped and doped silicon carbide film depends on different substrates

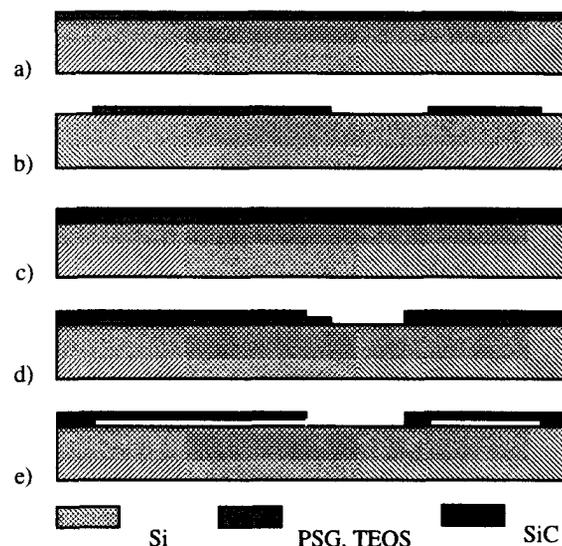


Fig. 4. Schematic view of the process flow to release the strain measurement structure.

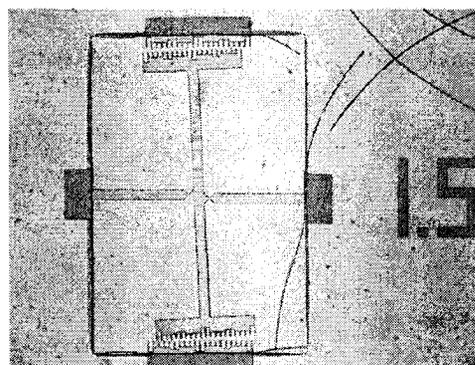
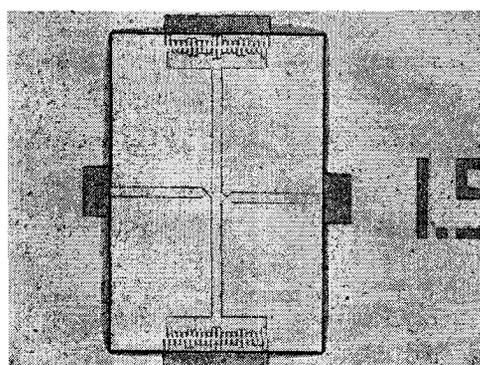


Fig. 5: Optical image of the strain measurement rotating structure after release for an undoped (left) and a Phosphorus-doped (right) silicon carbide layer

Development of a Multilayer SiC Surface Micromachining Process with Capabilities and Design Rules Comparable Conventional Polysilicon Surface Micromachining

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SiC is well known for its excellent mechanical, electrical and chemical properties, making it attractive for microfabricated sensors and actuators operating in harsh environments. Recent advances in SiC patterning techniques have led to the development of surface micromachining processes that are successful in both single and multilevel implementations [1]. To date, however, a multi-user fabrication process with capabilities and design rules comparable to conventional polysilicon processes has not been developed for SiC. This paper details our development of such a process, which we call the Multi-User SiC (MUSiC) process.

The MUSiC process is an eight-mask, four structural layer polycrystalline SiC (poly-SiC) surface micromachining process that generally embodies the Cronos Integrated Microsystems polysilicon MUMPs™ design rules. Due to limitations associated with SiC RIE (e.g., poor selectivity to SiO₂ and polysilicon, micromasking, and low etch rates), the MUSiC process cannot currently be realized by directly implementing the MUMPs fabrication process sequence using poly-SiC. Instead, a micromolding technique that uses SiC film deposition into microfabricated polysilicon and SiO₂ sacrificial molds, followed by mechanical polishing and chemical etching, is used to create patterned poly-SiC structural layers on sacrificial layers (Fig 1). The mechanical polishing steps are used to expose the molds and to create globally planar surfaces at each structural layer. The polysilicon sacrificial molds are dissolved in KOH, and the SiO₂ sacrificial molds in HF to release the devices. The micromolding technique creates featureless field areas, microstructures with smooth and vertical side walls, and top surfaces that are ideal for multilevel processing.

The inaugural MUSiC layout incorporates eight different chip designs replicated 6 times across a 100 mm-diameter wafer. The chip designs include accelerometers, lateral resonators, mechanical characterization structures, micromirrors, capacitive pressure sensors, shear stress sensors, micromotors, and flow sensors. The fabrication process was carried out on 100 mm-diameter Si wafers using poly-SiC films deposited by APCVD in a rf-induction heated reactor designed for epitaxial growth. SEM micrographs of a representative collection of completed SiC devices are shown in Figs. 2, 3, and 4. The first run of the MUSiC process has been successful in terms of pattern generation (~80%). However, issues related to residual stress, stress gradients, polishing selectivity, and deposition uniformity adversely affect fabrication yield and device performance. These issues can be attributed to the APCVD process, leading us to develop a LPCVD furnace to deposit poly-SiC films on large numbers of Si substrates.

The extended paper will detail issues related to the fabrication process, implementation of micromolding on large-area wafers, results from the mechanical and electrical properties test chips, and other issues pertinent to the successful development of the process. Initial results using the LPCVD furnace will also be presented.

[1] M. Mehregany and C.A. Zorman, "SiC MEMS: opportunities and challenges for applications in harsh environments", *Thin Solid Films*, vol. 355 – 356, pp. 518-524, 1999.

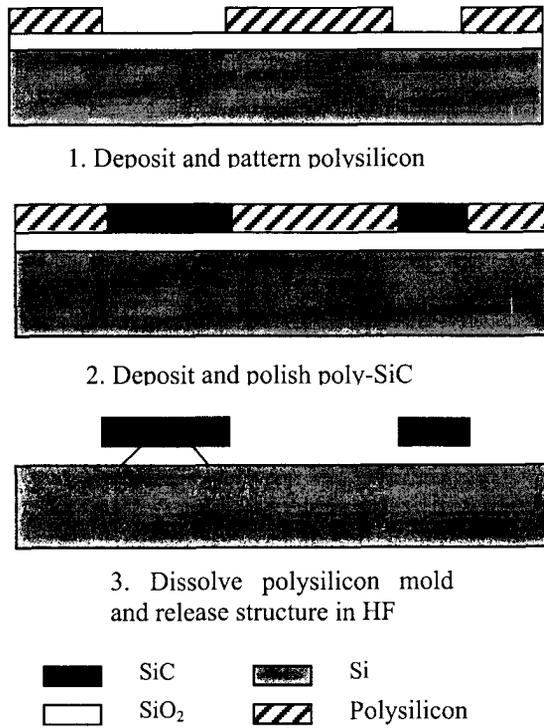


Fig. 1 Cross sectional schematics of the micromolding process.

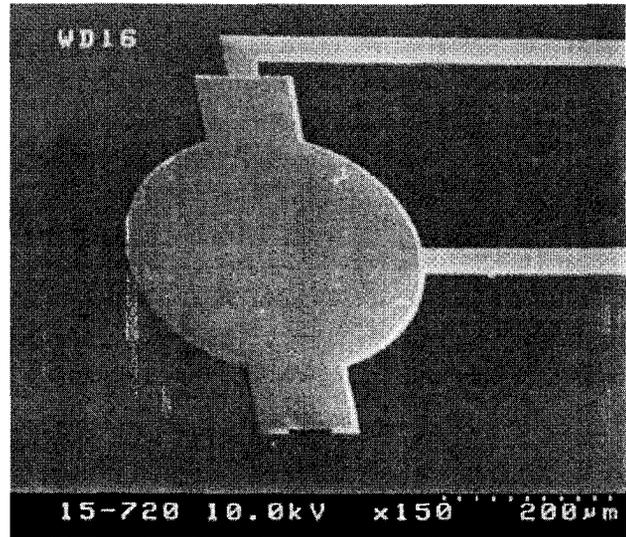


Fig. 2. SEM micrograph of a SiC capacitive pressure sensor.

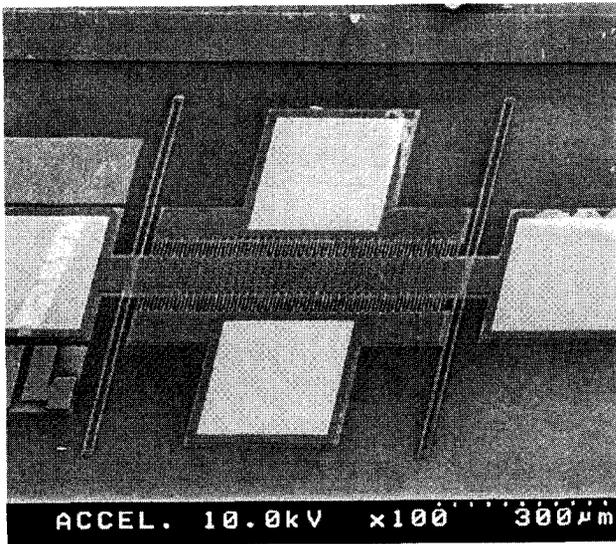


Fig. 3. SEM micrograph of a SiC shear-stress sensor.

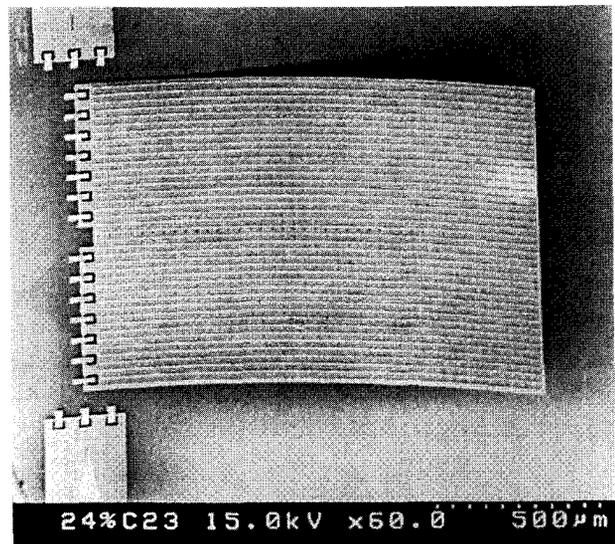


Fig. 4. SEM micrograph of a SiC micromirror showing the effects of residual stress gradient.

Reverse Characteristics of 4H-SiC Schottky Barrier Diode

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The Schottky barrier diode (SBD) on silicon carbide (SiC), a wide-gap semiconductor material, has the outstanding feature of high speed and low loss compared with the conventional SBD on Silicon (Si). A SiC SBD is designed so that the electric field at the Schottky interface is about 10 times as large as that of a Si SBD, when the reverse voltage is applied. Thus, it is necessary to investigate the effect of high electric fields on the reverse leakage current of SBDs. In this work, the reverse characteristics of a 4H-SiC SBD are analyzed using a device simulator, which can consider the tunneling process in addition to the thermionic emission. In the device simulator, the tunneling process is handled by setting up a generation/recombination probability, which takes the tunneling process into consideration, for each node of the mesh in the vicinity of a metal/semiconductor interface [1].

The calculated reverse characteristics of a 4H-SiC SBD are shown in Fig. 1. The solid line shows the leakage current calculated by the tunnel model. The broken line shows the leakage current calculated by the barrier-lowering model, which considers the Schottky barrier lowering by the image force. The dotted line shows the leakage current calculated by the conventional thermionic emission model. Figure 1 shows that the tunneling process dominates the reverse leakage current of a SiC SBD when a high reverse voltage is applied. The reverse characteristics of a Si SBD are also shown in Fig. 2, for comparison. In the reverse characteristic of a Si SBD, the increase in the leakage current induced by the barrier lowering is also important, and the effect of the tunneling process on the leakage current is relatively small compared with a SiC SBD, because the electric field applied to the metal/semiconductor interface is much lower than that of a SiC SBD.

If off-state loss due to the leakage current of a SiC SBD limits the total loss, we have the option of decreasing the electric field at the metal/semiconductor interface, or increasing the Schottky barrier height in order to reduce the off-state loss. However, both of these actions increase the on resistance. We have investigated whether a junction-barrier Schottky diode (JBS) would improve the trade-off between the leakage current and the on resistance by device simulation, considering the tunneling process for the first time. The schematic cross-section of a JBS is shown in Fig. 3, where the electric field at the metal/semiconductor interface is relaxed by the static induction effect from the p well. Figure 4 shows the forward (a) and reverse (b) characteristics of the 4H-SiC JBS. It can be seen from Fig. 4 that the reverse leakage current decreases by order without an increase in the on resistance, as the dimensions of the striped pattern of the p well and Schottky junction decreases.

This work was performed under the management of FED as a part of the METI project (R & D of Ultra-Low Loss Power Device Technologies) supported by NEDO.

[1] M. Jeong et al., IEDM-98, pp. 733-736, 1998

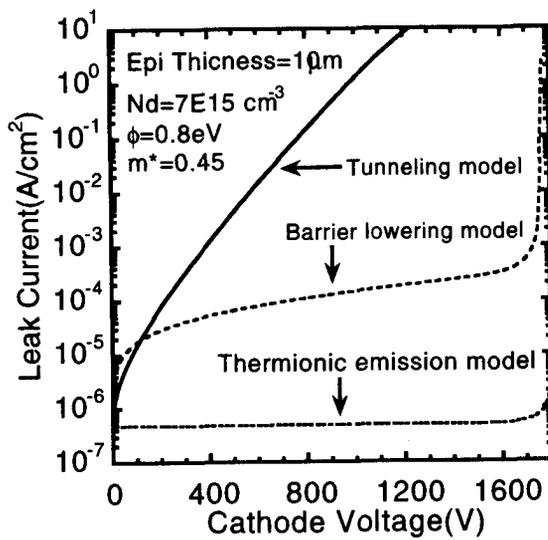


Fig. 1: Calculated reverse characteristics of 4H-SiC SBD.

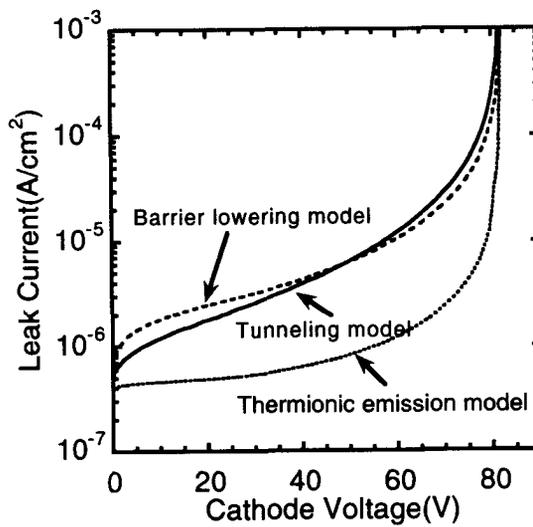


Fig. 2: Calculated reverse characteristics of Si SBD.

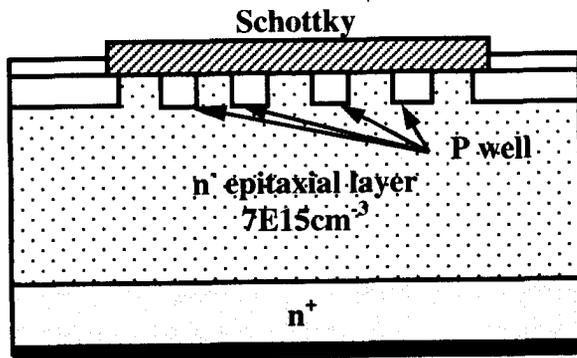


Fig. 3: Schematic cross section of a SiC Junction Schottky Barrier Diode (JBS)

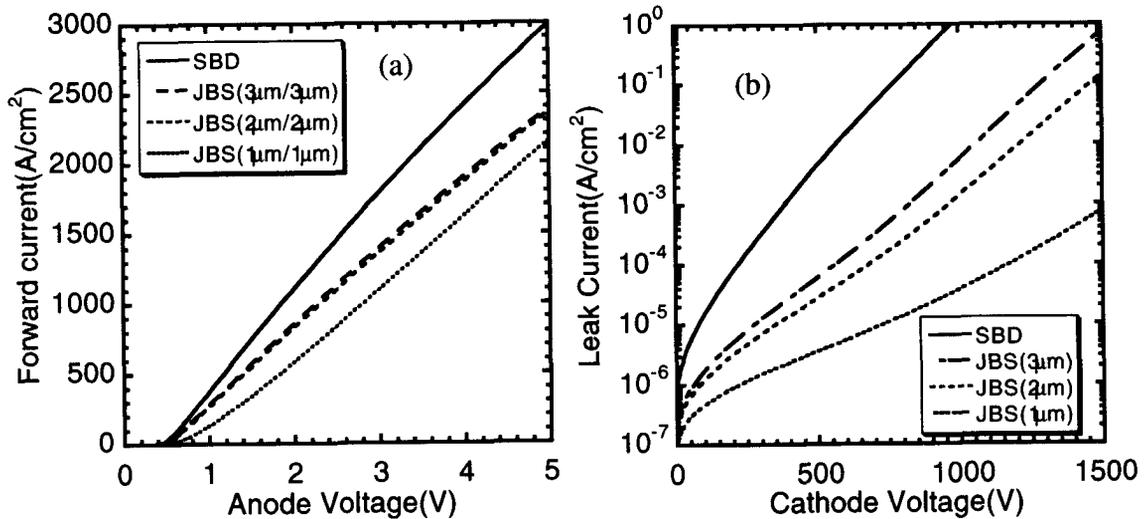


Fig. 4: Current-voltage characteristics of 4H-SiC JBS. (a) Forward characteristics of JBS. (b) Reverse characteristics of JBS. SiC SBD characteristics are shown for comparison.

High Voltage SiC Diode Design—An Experimental Study

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Abstract: High voltage SiC Schottky diode, device and process optimization is presented with experimental demonstration for 2.5KV and 1KV Schottky design. 2.5KV diodes were fabricated with a mean on-voltage of 1.85V at 2.25A (current density of 100A/cm²) and a differential on-resistance of 6mΩ-cm². At 5A, these devices have an on-voltage of 2.6V. These devices were fabricated with a yield of 20%. Smaller sized devices 1mmx1mm in dimension were fabricated with a yield of 40%. Fig. 1 and 2 show the reverse bias characteristics and forward bias characteristics for a typical diode. To our knowledge this is the best result reported thus far for this voltage/current rating. Many process and design parameters control the outcome of the device. The most critical parameters are implant species, implant activation, termination design, Schottky surface preparation, Schottky metal, epitaxial layer doping and thickness. We present the impact of these parameters briefly here, in the paper we will explain the concepts in detail along with experimental data.

Implant activation is essential for the devices to work. The key issues facing implant activation are step bunching, and surface decomposition. There have been many reports on activation placing the wafer in the vicinity of another SiC source. However, even with this technique activation at 1700C causes step bunching. We have addressed this issue by doing the activation very fast, only a few seconds at 1700C, with the wafer enclosed in a SiC container. While this time is insufficient to cause surface damage, it is enough to allow good activation. Fig. 3 shows an SEM picture of the surface after implant activation. It includes three regions: a) unetched/non-implanted, b) etched and implanted and c) etched but non-implanted. From the picture it can be seen that regions b and c which were etched show step bunching while the unetched region is free from such irregularities.

Aluminum and boron are the two practical choices for p-type dopants for SiC. Boron is lighter than aluminum and hence is implanted deeper for the same energy. Further boron diffuses during activation [ref], and hence deeper junctions can be formed using boron. Hence boron is preferred over aluminum for termination design. However for a good termination design we found the difference to be small. To optimize the termination design, we made devices with different termination structures including various field plate designs, floating field rings, and JTE termination. Highest breakdown voltage, 3000V, was obtained using aluminum implant with a floating field ring design. Boron JTE (2600V) performed better than aluminum JTE (2200V). These results will be presented in greater detail in the full paper.

The ideality factor of the Schottky contact plays a principal role in determining the on-state voltage of the diode. Poor ideality factors usually result in lower leakage current at the expense of large increase in the on-voltage. A small change in ideality factor, for example from 1.1 to 2.5, could easily increase the on-state voltage by two volts. Figure 5 compares the forward conduction characteristics for the two cases—ideality factor=1 and 2. Notice that the on-state voltage is increased from 1.4V to 2.4V. The Schottky ideality factor is very sensitive to the surface conditions. We have found that RIE etch of the Schottky surface prior to the implant activation results in poor ideality factors. Further RIE etching using CF₄ or CHF₃ chemistry, after implant activation significantly increases the ideality factor. Hence care needs to be taken to protect the Schottky surface.

We have performed theoretical calculations on the epitaxial layer doping and thickness for device optimization, and obtained a correlation for Epi thickness $W=1.5 \times BV/E_{critical}$ where BV is the desired breakdown voltage and $E_{critical}$ the breakdown electrical field. Detailed analysis will be presented in the paper. High temperature results, including measurements at 250C will also be presented in the paper.

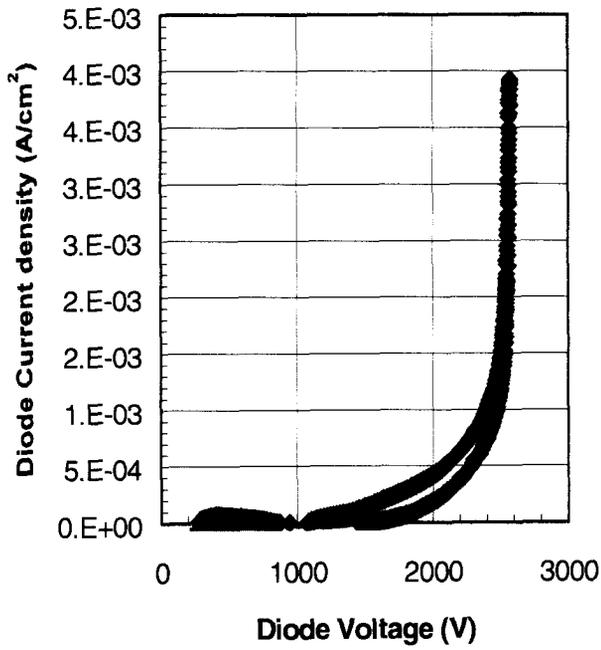


Fig. 1 Shows the reverse blocking characteristics of the diode. Size 2.25mm².

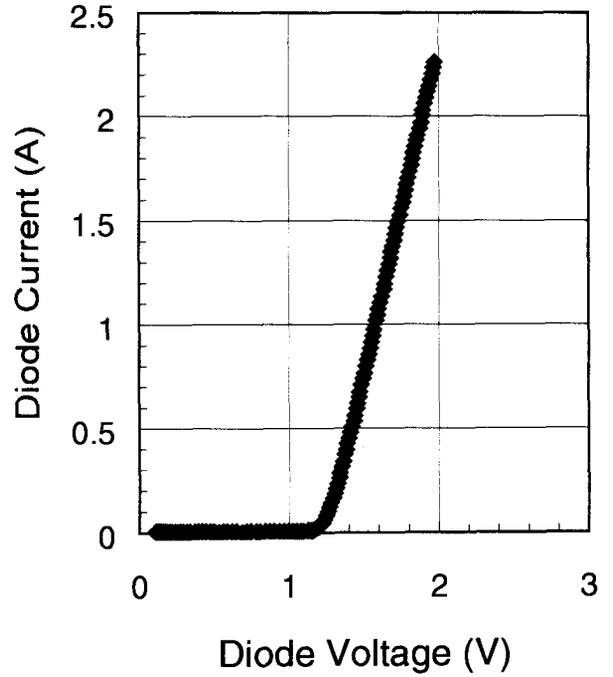


Fig. 2 Shows forward bias characteristics of the diode. Size 2.25mm².

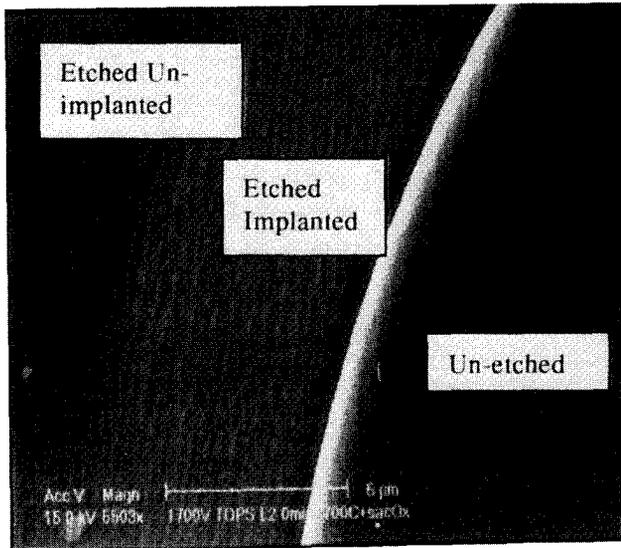


Fig. 3 Shows the SEM picture of a wafer showing three regions, a) Unetched SiC, b) Implanted and etched SiC, and c) Etched and Un-implanted SiC, after 1700C anneal.

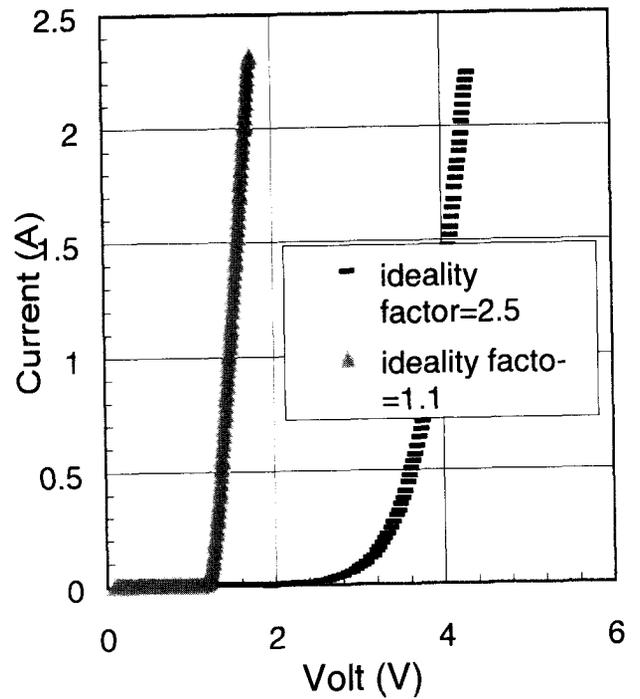


Fig. 4 Shows forward bias characteristics of two diodes with different schottky contact ideality factors.

Optimisation of Implanted Guard Ring Terminations in 4H SiC Schottky Diodes

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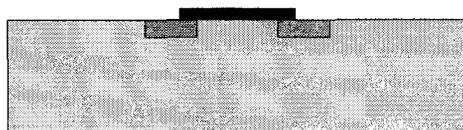
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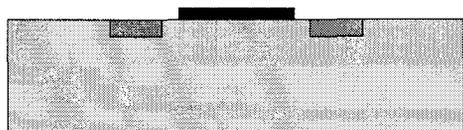
³ Surrey Ion Beam Centre, University of Surrey, Guildford, GU2 5XH, United Kingdom

Junction termination of Ni Schottky contacts on 4H SiC has been performed using floating guard ring structures. These structures are widely used in silicon technology as an effective means of planar edge termination. The major advantage of these structures is in the relative ease of fabrication compared to JTE techniques and the increased reliability over field plate designs.

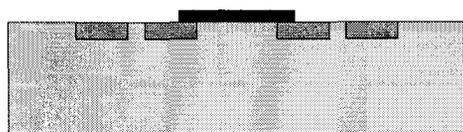
In order to determine the merits of guard ring structures four designs were fabricated. In each case the guard ring width is 20µm. Type 1 has the guard ring overlapping the edge of the Schottky contact by 5µm, whilst type 2 has a 5µm gap. Type 3 is equal to type 1, but with a subsequent 20µm ring, 5µm outside the first. Similarly, type 4 has one guard ring more than type 2. The structures are shown below.



Type 1



Type 2



Type 3



Type 4

Commercial 4H-SiC $n-n^+$ epitaxial wafers from Cree Inc. were used to fabricate the diodes. The n layer had a donor concentration of $3 \times 10^{15} \text{cm}^{-3}$ and a thickness of $10 \mu\text{m}$. The samples were cleaned by degreasing with organic solvents followed by RCA procedure. Photo resist S1828 $2 \mu\text{m}$ in thick was used as a mask for ion implantation. Boron implants of energies up to 200keV and total dose $5 \times 10^{13} \text{cm}^{-2}$ were annealed under Ar flow in a RF furnace at 1600°C for 20 minutes. After annealing the samples were cleaned by an RCA procedure. All metal depositions were made by thermal evaporation at a base pressure of 8×10^{-6} Torr with no sample heating. Immediately prior to placing the samples in the vacuum chamber, they were immersed in 10% HF for 20 s at room temperature followed by blow drying. Nickel 100 nm thick was deposited on the back side of the wafer. Annealing of the back side contact was performed at 1100°C for 180 sec in vacuum chamber pumped down to 8×10^{-6} Torr. Nickel of 100 nm thick with titanium sub-layer ($\sim 5 \text{nm}$) was deposited on epitaxial layer as a Schottky contact. After annealing at 420°C for 20 min, the geometry of the contacts was defined by contact UV lithography.

IV characteristics of the diodes were measured using an HP4155A semiconductor parameter analyser and breakdown tests performed using a Tektronix 371 curve tracer.

The ideality of the fabricated diodes was found to be weakly dependant on the diode type. This can be seen below.

Diode Type	Ideality
Unimplanted	1.04
Type 1	1.07
Type 2	1.10
Type 3	1.10
Type 4	1.07

The low ideality factor for the samples suggests that the surface quality under the Schottky contact is high. This is of importance for diode types 1 and 3 where the Schottky contact overlaps the implanted guard ring, with the associated surface roughness and implantation damage.

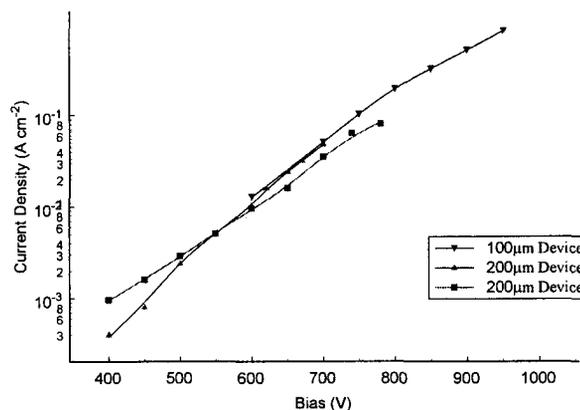
The breakdown voltage of the diodes fabricated on bare epitaxial material with no guard ring structures shows an average breakdown voltage of 451V. The breakdown voltage of diodes on the sample annealed at 1600°C is shown below.

Diode Type	Breakdown Voltage
1	783
2	631
3	912
4	764

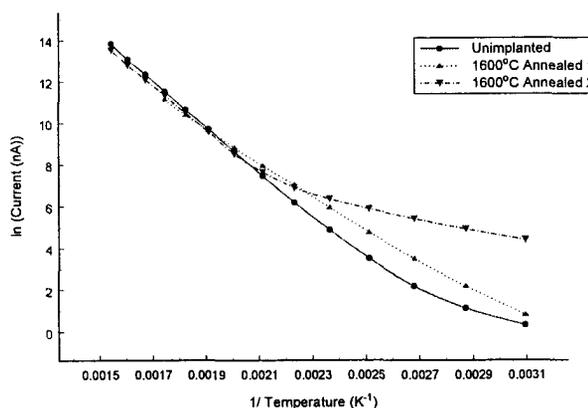
From this it can be seen that the addition of subsequent guard rings increases the average breakdown of the device (Type 3 c.f. Type 1) by approximately 18%. This is consistent with other observations made in both silicon and SiC devices. The change in diode type from gapped structures (Types 2 & 4) to overlapped structures (Types 1 & 3) also sees an increase in breakdown voltage of approximately 22%. From this the double overlapped guard ring structure appears to be the most promising.

For the type 3 diode structures, the leakage current at high reverse bias is dependent on the contact area and not the termination circumference. This would suggest that the current is determined by the behaviour of the contact itself and not the guard ring structure.

The leakage current at -100V bias for a series of 200µm diameter diodes has been



measured as a function of temperature. The unimplanted diode behaviour shows the effect of the intrinsic material properties on the temperature dependence. At low temperatures the guard ring structures dominate the leakage current, but as the temperature rises above 225°C the leakage current is independent of the termination, suggesting a common mechanism. This can be seen by the overlay of the data from both terminated and unterminated devices



Overlapped guard ring structures have been shown to give the greatest increase in breakdown, without adversely affecting forward characteristics or high temperature leakage. Further work will concentrate on establishing the mechanism responsible for the leakage current behaviour at high temperatures.

Minimization of Electric Field Enhancement at Electrode Edge by Surface High Resistive Layer in Ti/4H-SiC Schottky Barrier Diode

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SiC material has attracted much attention for high-power semiconductor devices because of high breakdown electric field. SiC Schottky barrier diode (SBD) is expected to decrease on-resistance and switching loss compared to Si pin diode. Hence, we fabricate Ti/4H-SiC SBD without any intentional edge termination. The measured breakdown voltage is equal to the value expected from breakdown field of SiC, and is evaluated by device simulation.

Wafers with structures of n-epitaxial layer on n-type substrate purchased from Cree were employed. N-type back contact was formed by Ni evaporation and rapid thermal annealing. Schottky electrode was formed by Ti sputtering on n-type 4H-SiC epitaxial layer with carrier concentration of $5 \times 10^{15} \text{ cm}^{-3}$ and thickness of 10 μm . As a pre-treatment before the Schottky electrode formation, HCl+HNO₃ and HF treatment was carried out. Devices with 100 or 500 μm diameter were fabricated by wet etching of Ti. The measured current-voltage (I-V) characteristics are shown in Fig. 1. Low on-resistance of 3 $\text{m}\Omega\text{cm}^2$, low leakage current of 10^{-5} A/cm^2 at 1000 V, and relatively high breakdown voltage of 1500 V are obtained. Schottky barrier height is evaluated to be 1.2 eV, shown in the figure. The barrier height is relatively high compared to the estimated value from workfunction of Ti, and close to the value estimated from hybrid orbital reference energy level for surface pinning [1]. Therefore, influence of thin surface high resistive layer, which brings surface pinning, is investigated.

I-V characteristics are investigated by device simulation with impact ionization coefficients reported by Konstantinov et al [2] and barrier tunneling effective mass of 0.66, which is effective density mass employed. Trap level of high-resistive layer is assumed to be acceptor type with activation energy of 0.5eV. In the same barrier heights, the forward rise-on voltage of devices with thin surface layer is calculated to be larger than that of device without thin surface layer. For devices without thin surface high resistive layer, the barrier height used for the calculation was 1.2 eV, which is equal to the measured value. In order to fit to the measured forward I-V characteristics, the barrier heights of devices with thin surface high resistive layer were set to 0.55-0.85 eV for calculation, depending on thickness and concentration of traps in thin surface high resistive layer.

The calculated results are also shown in the figure. The calculated breakdown voltage of one-dimensional (1D) device without thin surface high resistive layer is 1900 V,

which shows that the breakdown voltage of fabricated devices is 79 % of 1 D estimated value. Though the breakdown voltage of 2D device without thin surface layer is fairly low (below 50V, 1.5 % of 1D device), that of SBD with surface layer is calculated to be 40-85% of 1D devices, as shown in the figure. For higher trap concentration ($1.5\text{-}2\times 10^{19}\text{ cm}^{-3}$), the electric field enhancement is minimized by the effect of thin surface layer and the breakdown is occurred by avalanche above 1200 V. Otherwise, the breakdown is occurred by Schottky barrier tunneling at the electrode edge near 700 V for lower trap concentration ($1\times 10^{19}\text{ cm}^{-3}$). Hence, the breakdown voltage over 1200 V is brought by the minimization of the electric field enhancement at the Schottky electrode edge by the effect of thin surface high resistive layer. The origin of leakage current of SBD is considered to be Schottky barrier tunneling currents.

In summary, Ti/4H-SiC SBD without any intentional edge termination, with low on-resistance of $3\text{ m}\Omega\text{cm}^2$, low leakage current of 10^{-5} A/cm^2 at 1000 V, and relatively high breakdown voltage of 1500 V, is fabricated. The relation between obtained breakdown voltage, Schottky barrier height, and thin surface layer is made clear. Influence of trap parameter on device properties will be also discussed.

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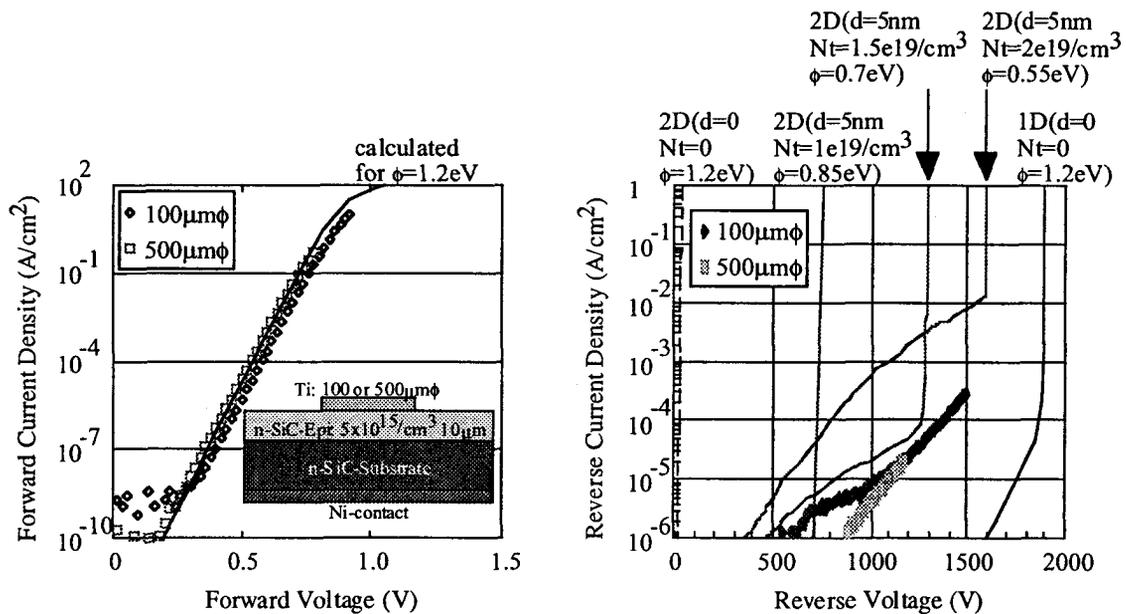


Fig. 1. Measured and simulated I-V characteristics of Ti/4H-SiC SBD.

Influence of epitaxial layer on SiC Schottky diode gas sensors operated in high temperature conditions

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Gas sensor devices operated under high temperature conditions have been investigated using catalytic metal-insulator-silicon carbide, MISiC, structures. The sensors have been tested for several industrial applications [1]. We have studied the influence of CO and O₂ in the ambient in terms of both gas response and device characteristics of the sensor devices [2]. Usually an epitaxial SiC layer grown on a low resistance SiC substrate is used for the sensor device. It is expected that the property of the epitaxial layer strongly affect the electrical characteristics of the diode. In this contribution, experimental results under high temperature conditions are discussed regarding the electrical properties, as well as gas sensing properties, of gas sensor Schottky diodes with different thickness and doping of the epitaxial layer.

The three types of diodes, which were compared, are described in Table 1. These diodes have different thickness and doping of the epitaxial layers, that are grown under different conditions [3-5]. The carrier density of the epitaxial layers was estimated from the capacitance-voltage characteristics. The devices have gate contacts of porous Pt, with an area of about $7.8 \times 10^{-3} \text{ cm}^2$, and ohmic back contacts of TaSi_x + Pt [1]. One Schottky diode was placed on a Pt disc in a quartz tube, and its top electrode was contacted by a Pt wire. The quartz tube chamber was placed in an oven. Forward and reverse current-voltage characteristics were measured in 4000 ppm O₂ in Ar and 8000 ppm CO in Ar, respectively, during steady state conditions at each investigated temperature, 22~600°C.

Figure 1 shows the temperature dependence of the series resistance calculated from the I-V characteristics in the high current region. The thickness and carrier density of the epitaxial layer mainly determines the value of the series resistance. For diodes of type 3, the resistance decreased, with a slope of about -1.5, with increasing temperature in the lower temperature region. This is suggested to be a result of the higher impurity concentration in the epitaxial layer of diodes type 3. The slope of about 1.5 in the higher temperature region suggests that here the resistance increases due to lattice scattering. The series resistance of diodes type 2 monotonously increased with increasing temperature. This means that the resistance is affected by lattice scattering. Further studies are needed to find the reason why the resistance of diodes type 1 has a maximum at about 670K.

In Fig. 2 the ideality factors are plotted versus the temperature. Diodes of type 1 have a higher value of the ideality factor than diodes type 2 and 3 at $T \leq 670\text{K}$. The value of the Schottky barrier height was evaluated for each diode from the temperature dependence of the I-V characteristics and was always about 1.5 eV. The change of the barrier height caused by a change from oxygen to carbon monoxide in the gas ambient was estimated from the forward and reverse current-voltage characteristics. The barrier height change was $\leq 0.3 \text{ eV}$ and had a tendency to increase with increasing temperature for all three types of diodes, that is, the difference in epilayers did not seem to have an influence. The gas response of the devices is

measured as the voltage change at a constant current for a change in the gas ambient. The gas response for a change from oxygen to carbon monoxide in the ambient is higher for the type 1 diodes, above 0.5 V, than for diodes of type 2 and 3. Thus the difference in gas response may be connected to the value of the ideality factor, but not to the change in barrier height, since the latter is similar for the three devices.

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Table 1 Condition of three types diode with different epitaxial-layer.

No.	Thickness (μm)	Condition of epitaxial layer	Carrier concentration estimated by C-V method (cm^{-3})
1	10	Purchased from Cree [3]	3.4×10^{15}
2	24	Hot wall CVD epitaxy [4]	8.1×10^{14}
3	50	Sublimation epitaxy [5], Growth rate= $100 \mu\text{m}/\text{h}$	2.1×10^{16}

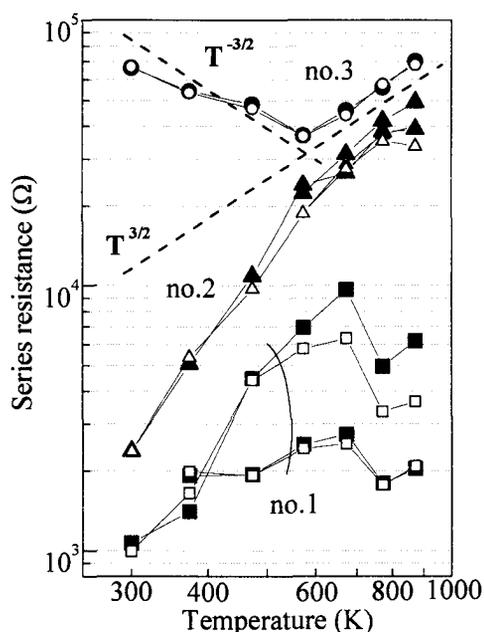


Fig. 1 The temperature dependence of the series resistance of the Schottky diodes in Table 1. A solid and open symbol represents O_2 and CO in the ambient, respectively.

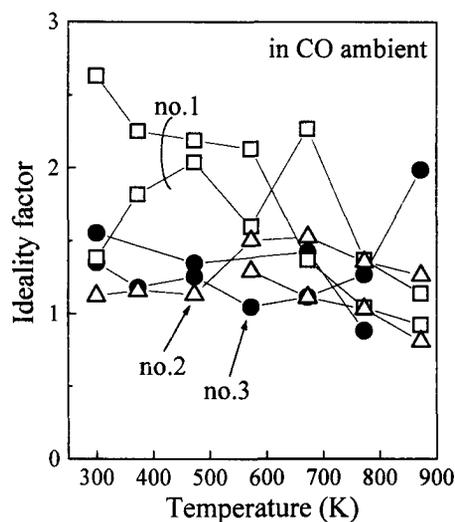


Fig. 2 Temperature dependence of the ideality factor for three types of diodes.

Performance of 4H-SiC Schottky Diodes with Al doped p-Guardring Junction Termination at Reverse Bias

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1 Introduction

In recent years, a large variety of promising SiC devices have been realised in the fields of high power, high temperature, and high frequency applications. In this work we especially concentrate in particular on 4H-SiC Schottky diodes which, due to their physical properties, have proven to show excellent performance for the realisation of fast switching applications with nearly negligible power loss [1]. High power switching implies the requirement of getting very low current at high reverse bias and very high current at low forward bias. SiC, with a critical field 10 times higher than Si, with a band gap of 2.5-3 times larger than that of Si, a thermal conductivity better than copper and large saturation velocities for electrons and holes offers these qualities for high power devices. Using numerical simulation, we investigated the principal mechanisms governing the device operation.

2 Device structure, surface conditions and simulation

Figure 1 shows a schematic view of the Schottky diode, featuring a junction termination to avoid high electrical field peaks at the edges of the contacts, a boundary passivation and a highly doped field stop. In the simulations the Schottky diode was treated as a 2-dimensional structure. Experimental results [3] and [4] suggest, in view of the surface quality of SiC, surface charges may affect the device characteristics and, hence have to be considered in device simulation. As location of such surface charges we assumed the interface of the p-guardring and the boundary passivation and examined the effects on the reverse

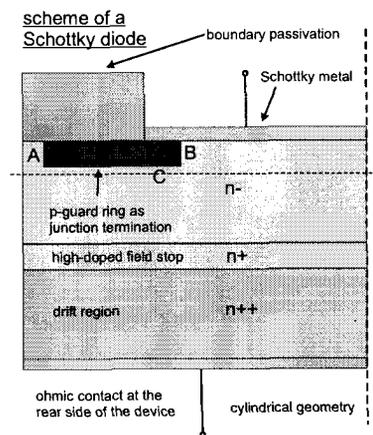


Figure 1: Cross section of the analysed structure

characteristics. The device analysis was performed using the multi-dimensional device simulator *DessisISE* which features a rigorous thermodynamic model of the device behavior based on the solution of the coupled system of Poisson's equation together with the electron continuity and hole continuity equations. The calculations assumed quasistationary conditions in reverse bias.

3 Simulation results

For varying Al doping of the p-guardring and without additional surface charges along the interface of the p-guardring and the boundary passivation our results show, in conformity with former works [2], that different locations can be identified at which avalanche breakdown occurs. Low doping leads to critical field peaks at the outer edge (A) of the p-guardring, whereas at high doping concentration this point moves to the surface underneath the Schottky contact (B). The maximum breakdown voltage is observed if the region with maximum electric field is located at

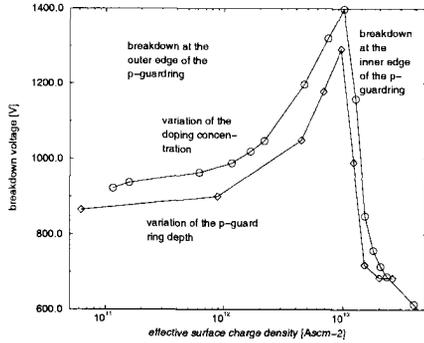


Figure 2: Breakdown voltage versus the surface charge

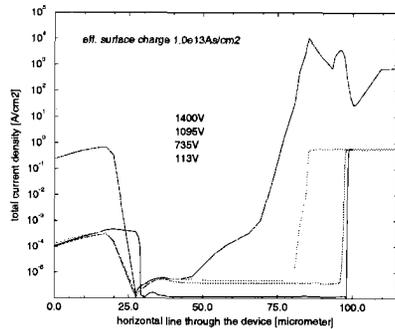


Figure 3: Total current density along a horizontal cut-line through the device

the inner edge of the p-implantation deep in the bulk (C). In this way the doping concentration of the p-guardring controls the breakdown voltage and determines the location where avalanche breakdown takes place (see Figs. 1 and 2). Assuming a surface charge of $6.0 \cdot 10^{12} \text{ As/cm}^2$ along the interface of the p-guardring and the boundary passivation, the breakdown voltage is drastically reduced. As example for a Schottky diode with an effective surface charge at the p-guardring of $1.0 \cdot 10^{13} \text{ As/cm}^2$ and the same structure with an additional surface charge as mentioned above, the breakdown voltage is reduced from 1400V to 1095V. The device behavior under the influence of additional surface charges, was analysed in detail by studying the profile of the space charge, the total current density, the impact ionisation rate and the distribution of the electrical field. Comparing the respective total current densities shows that, for the assumed surface charges, the total current density at the outer edge of the p-guardring rises (see Figs. 3 and 4), while the impact ionisation rate shows equivalent behavior. The maxima of the electric field are located at the same points as they occur without additional surface charges.

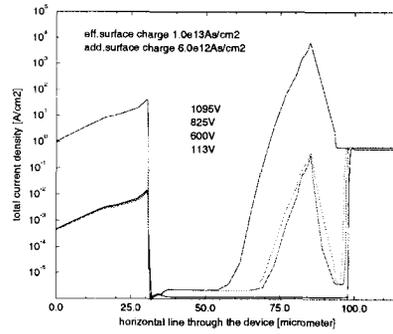


Figure 4: Total current density along a horizontal cut-line through the device

4 Conclusion

The effect of a p-guardring junction termination of Schottky diodes on its breakdown behavior has been discussed. The results of an earlier analysis [2] were corroborated and extended by studying in detail the spatial distribution of the total current density, the electric field and the impact ionisation rate, considering additional charges along the interface of the boundary passivation and the p-guardring.

5 Acknowledgements

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Demonstration of 4H-SiC Avalanche Photodiode Linear Arrays

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Avalanche photodiode (APD) linear array is of great importance for spectroscopic and imaging applications. The demonstration of 4H-SiC APDs¹ makes 4H-SiC APD linear array possible. A high yield of APDs is the prerequisite for APD linear array demonstration. The control of the uniformity of breakdown voltage and the leakage current is also very critical. In this report, we present design, fabrication and characterization of 4H-SiC APD linear arrays.

The present SiC wafers are still very defective. Achieving high enough yield is therefore a very challenging issue. The pixel area has to be sacrificed to achieve a yield high enough for linear array demonstration. As shown in Fig.1, in order to have a substantial yield on an array with pixel number higher than 10, the yield of the pixels has to be higher than 90%. Since the density of the elementary screw dislocation, the major detrimental factor for an 4H-SiC APD, is typically in the range of 10^3 - $10^4/cm^2$,² the pixel area should be smaller than $10^4\mu m^2$ so as to have a yield of pixels higher than 90%.

4H-SiC APD linear arrays containing 40 pixels with the pixel area of $4.3 \times 10^3 \mu m^2$ are designed and fabricated. Figure 2 shows the top view of a pixel. The sizes of 4H-SiC APD mesa, their optical window, and wire-binding pad are 35×122 , 84×19 , and $80 \times 100 \mu m^2$, respectively. A $p^+pn^+nn^-n^+$ reach-through structure is used in our fabrication. The doping concentrations and thicknesses from p^+ to n^- are $3 \times 10^{19}/cm^3$ and $0.2 \mu m$, $1.3 \times 10^{18}/cm^3$ and $0.25 \mu m$, $5 \times 10^{15}/cm^3$ and $0.22 \mu m$, $1 \times 10^{18}/cm^3$ and $0.11 \mu m$, and $4 \times 10^{15}/cm^3$ and $2 \mu m$, respectively. The targeted breakdown voltage is 116V. The substrate is n^+ . Edges of APDs are terminated by $1.5 \mu m$ deep mesa and passivated by SiO_2 .

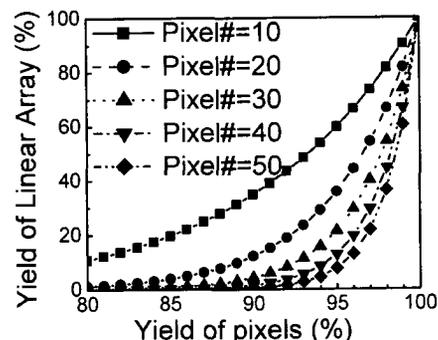


Fig.1: The yield of linear array with different pixel number as a function of the yield of pixels

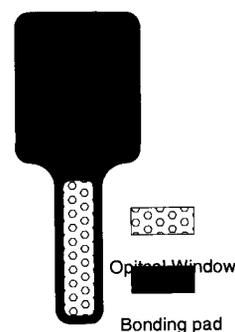


Fig.2: The top view of a pixel of 4H-SiC linear array.

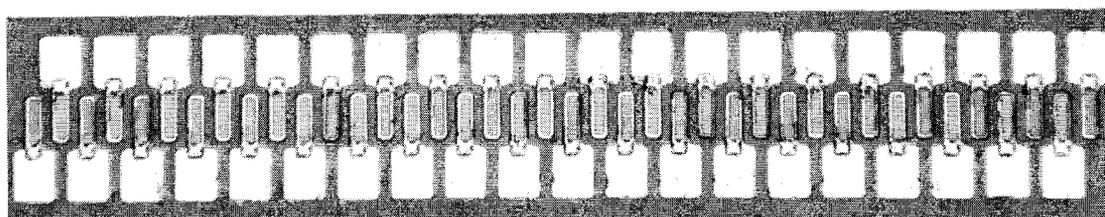


Fig.3: The top view of a fabricated 4H-SiC linear array with 40 pixels

Figure 3 shows a photo of a fabricated 4H-SiC linear array with 40 pixels. The period of pixels is $50\mu\text{m}$ and the total length of an array is 2mm.

The reverse I-V characteristics of pixels are tested and mapped. Fig.4 shows mapping of the breakdown voltage (V_B) and the leakage current at 120V (about 95% of V_B) for one of the best arrays. It can be seen that V_B is very uniform except for the 13th pixel. The average of V_B without the 13th pixel is 126.8V with a standard deviation of 0.9V. Most of pixels show a leakage

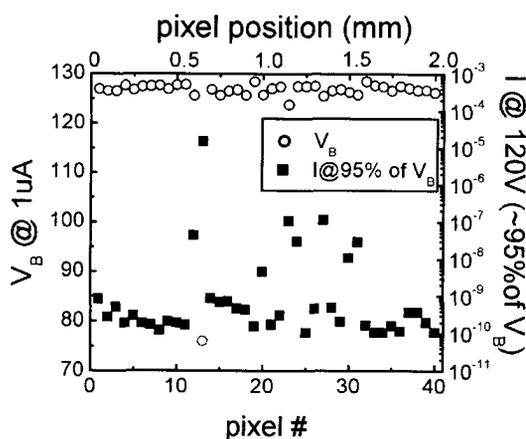


Fig.4: The V_B and the leakage current mapping of a 4H-SiC APD linear array

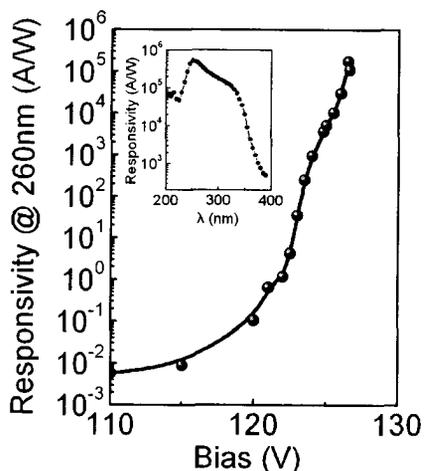


Fig.5: The peak responsivity as the function of reverse bias voltage. The inset is the response spectra at 126.5V.

current lower than 1nA at 95% of V_B . Compared with the high uniformity of V_B , the uniformity of the leakage current is lower. Still, mapping shows that pixels from 1 to 11 and 31 to 40 demonstrate uniform low leakage current at 95% of V_B . They can be packaged for APD linear array applications.

A total of 200 pixels have been tested. The accumulative yield of pixels with breakdown voltages higher than 116V is 91%. The limiting factor is believed to be the elementary screw dislocations. The yield of pixels with the leakage current lower than 1nA at 95% of V_B is 50%. The uniformity of leakage current is much poorer than that of V_B . The poor uniformity of leakage current is, therefore, the major barrier toward achieving 4H-SiC APD linear arrays containing more pixels. Experimental results show that leakage current is dominated by peripheral leakage current.

Figure 5 shows a typical peak responsivity of pixels as a function of the reverse bias. The inset is the response spectra at 126.5V. The peak of the response spectra is located at 260nm and the maximum achievable responsivity is higher than $1 \times 10^5 \text{ A/W}$. Assume unity quantum efficiency, the corresponding optical gain is $4 \times 10^5 \text{ A/W}$. The true optical gain should be higher because the APDs do not have unity quantum efficiency.

In summary, 4H-SiC APD linear arrays have been demonstrated. An array containing up to 11 pixels with a good uniformity of V_B and a low leakage current has been demonstrated for the first time.

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A New Type SiC Gas Sensor with a pn-Junction Structure

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1. Introduction

Silicon Carbide (SiC) devices are expected for use in high temperature environments under the high power and low loss conditions¹⁾. In addition to these power devices, sensor applications such as ultraviolet sensitive diodes²⁾ and gas sensors³⁾ are other fields of targets for SiC devices. Basic device structures of gas sensors utilize catalytic gate Metal/Insulator/SiC substrate structures such as MIS-Schottky contacts, MIS-capacitors, and MISFETs. For the reliable operation of these devices, both metal contacts and intermediate thin insulator films have to stand high temperature gas environments. Present paper reports on a new and simple type gas sensors utilizing 6H-SiC pn-junction and ohmic contacts, which are operable at 500°C in gas ambient such as hydrogen and hydrocarbons. Present device structures are composed of catalytic metal layer/ohmic contact layer/SiC pn-junction/ohmic contact layer. In this device ohmic contact layers play roles for adhesion and barrier layer to the catalytic metal material. Device fabrication, contact stability at the elevated temperature and the device response to the gas components are discussed.

2. Experimental

PN-junctions were made with Al-doping with ion implantation (70~300keV, $2 \times 10^{17} \sim 5 \times 10^{19}$ Al/cm³ in box profiles) or laser doping in n-type epitaxial layers (1.8×10^{16} N/cm³) on n-type bulk 6H-SiC substrates. After ion implantation the substrates were annealed in Ar flowing atmosphere at 1600 to 1650°C for 30 min. PtSi or PtSi/p⁺-Si thin layers for ohmic contacts to p-type doped layer were deposited by laser ablation with a KrF excimer laser, and Ta metal layer were used for the n-type back contacts. Pt metal films 50 nm thick was sputter-deposited on the both ohmic contacts, which function as a catalytic layer and a cap layer to prevent from oxidation. Ohmic contacts on the thin-doped layer were fabricated with the laser processing technique to ensure a steep and shallow contact interface⁴⁾. I-V characteristics of the diodes were tested at 500°C in atmospheres of flowing test gas mixtures. At the constant current in the forward bias condition, test samples show voltage-sensitivity to hydrogen and hydrocarbons (typical example; C₃H₆) in concentration of 2 to 500 ppm contained in N₂ gas.

3. Results and Discussions

Figure 1 shows a device structure under investigation. A PtSi ohmic contact was made by irradiating the deposited PtSi film (~25nm thick) with a KrF excimer laser (energy density; 2.5J/cm², numbers of pulses; 1000). An additional PtSi film 75 nm thick was *in situ* deposited on the contact to ensure the ohmic property, to increase in adhesion of the Pt catalytic electrode, and to allow function as a barrier metal against Pt. A Ta film for the n-type back contact was deposited at 350°C with a DC-sputter method. Al ions were implanted at 100 keV with doses 1×10^{13} cm⁻², which correspond to an Al peak concentration of 1×10^{18} cm⁻³. The projected range R_p of Al ions is estimated to be 120nm. In addition, 1×10^{13} Al/cm² were implanted at 30 keV (3×10^{18} cm⁻³) to decrease in the contact resistance.

Fig.2 shows I-V characteristics at 500°C both in the pure N₂ and the mixture of N₂ and H₂ (100 ppm) gas ambient. As shown in the figure, the voltage drop of the device slightly decreases at a constant forward current, which is dependent on the gas species and their contents. Three kinds of gas mixtures H₂/N₂, C₃H₆/N₂, and CO/N₂ were tested in the gas fraction ranging from 2 to 500 ppm. The sensor response is defined as the measured change in voltage at a constant forward current 20 mA as the gas is switched on from the pure N₂ gas to a test gas mixture. Fig.3 shows an example of the response at 500°C for the H₂/N₂ gas mixture containing 20 and 100 ppm H₂. The sensor response is smaller to C₃H₆ than to H₂, and is very weak to CO.

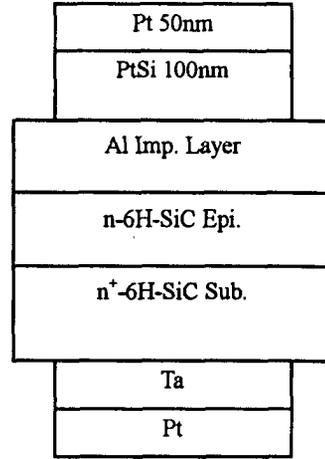


Fig.1 Device structure with a pn-junction and ohmic contacts. A top Pt layer functions as a catalytic electrode.

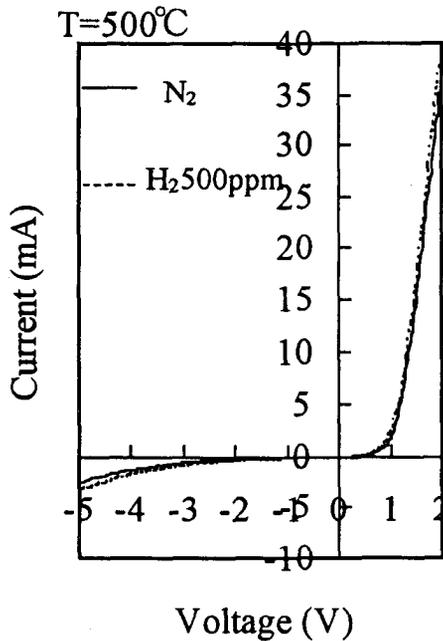


Fig.2 I-V characteristics of an Al-doped pn-junction sensor diode. The device temperature is monitored with a thermocouple attached to the sensor.

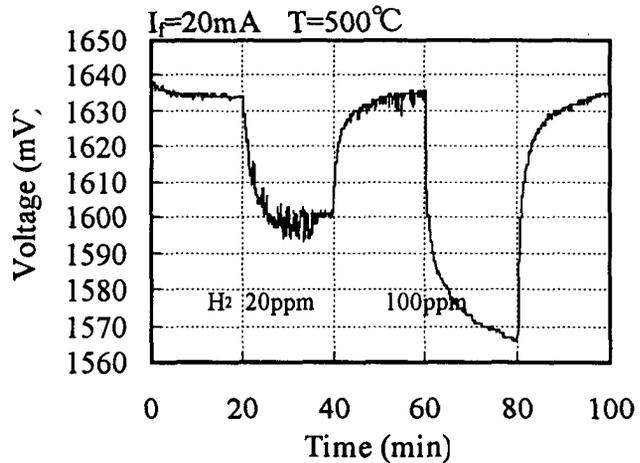


Fig.3 The sensor response to H₂ diluted in N₂ gas. The base voltage for the pure N₂ gas is stable within a few mV during measurements.

In conclusion, the present paper proposes a new gas sensor with a simple device structure. The sensor response time, sensitivity, and thermal stability are discussed in terms of the device structure, impurity profile, and electrode materials.

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N AND P TYPE 6H-SiC FILMS FOR THE CREATION DIODE AND TRIODE STRUCTURE OF NUCLEAR PARTICLE DETECTORS

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Recently, considerable progress has been made in the fabrication of high-quality single-crystal SiC substrates and epitaxial film [1]. The interest of nuclear physicists in SiC is due to the potentially high radiation and chemical hardness of SiC-devices and the possibility of their operation at elevated temperatures [2]. For detectors fabrication were used 6H- SiC films n- and p-type conductivity grown by vacuum sublimation epitaxy [3]. *1. N-type epilayers* (about $d=10\mu\text{m}$ thick, net doping concentration $|N_D^+ - N_A^-| \sim 2 \cdot 10^{15} \text{ cm}^{-3}$) were used for Schottky diodes (barrier were formed by magnetron sputtering of Ni) producing. Diodes were irradiated with a 1 GeV proton beam extracted from the synchrocyclotron. The first dose is $\sim 3 \cdot 10^{14} \text{ cm}^{-2}$. The overall dose of irradiation with relativistic protons was $1.3 \cdot 10^{15} \text{ cm}^{-2}$.

The next detectors parameters were measured: charge collection efficiency (CCE) and energy resolution by alpha-spectrometry; width of the sensitive region (W_{eff}) and capacitance; diffusion length of holes (L_D); deep levels contents by DLTS method. It was shown that dose $(3-5) \cdot 10^{14} \text{ p/cm}^2$ corresponded the initial stage of the detectors degradation. The value L_D decrease up to 20-30%, but W_{eff} -voltage dependence remains unchanged. Under dose $\sim 10^{15} \text{ p/cm}^2$ high R-center concentration causes compensation conductivity of the base [4]. Also conditions of the charge carrier transport deteriorated. For realization CCE=1 3 times larger voltage (U) one must be applied.

2. P-type films ($d \approx 10 \mu\text{m}$, $N_A^- - N_D^+ \sim 2,8 \cdot 10^{15} \text{ cm}^{-3}$) were used for fabrication triode n-p-n⁺ structure. Triode was realizing by grown of p-type epilayers on base of 6H n⁺-SiC substrate.. The triodes were studied in a floating-base mode with alpha particles (5,8 MeV) coming in from the Schottky barrier side. The range of the alpha particles (20 μm) exceeded the film thickness so that the nonequilibrium charge appearing in the base corresponded (with account of the Bragg ionization curve) to absorption of the energy $E=2 \text{ MeV}$

Capacitance measurements demonstrated that the p-n⁺ junctions of the structure are not identical. The Schottky barrier corresponds to an "abrupt" junction, whereas at the n⁺ substrate the transition to the p-type conduction is gradual. Therefore, two connection polarities were tested, with either the p-n⁺ junction of the substrate or the Schottky barrier serving as collector.

In the last regime the E(U) dependence becomes superlinear. The signal corresponds to a value of about 60-80 MeV. The shape of the spectrum is Gaussian. So it was shown possibility of the ≈ 50 times amplification of nonequilibrium charge created by short-range ions.

To describe the effect quantitatively, the first place take into account that the structure under study is equivalent to a phototransistor. It is known that the primary current of the

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phototransistor is amplified in $(1-\alpha_T)^{-1}$ times, where α_T is the base-transport factor for electrons. In accordance with [5] we have for our case $\alpha_T = [(d-W)/L_D] / \text{sh}[(d-W)/L_D]$.

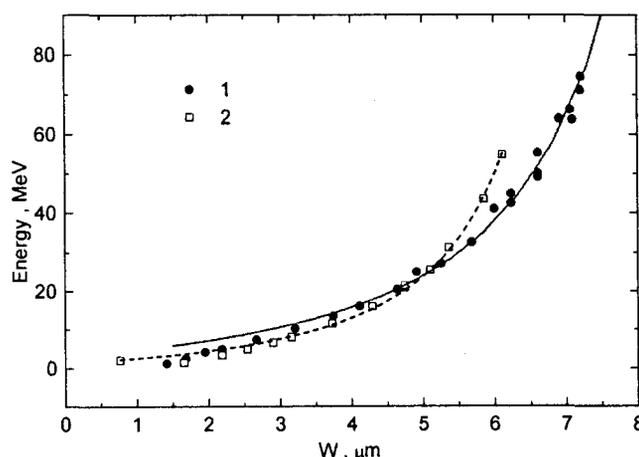


Fig. 1. Signal from alpha particle (in energy units) versus the width of the space charge region at the collector junction (Schottky barrier); fitting data: $L_D = 8.85$ and 5.85 (μm); film thickness $d = 10.75$ and 8.53 (μm) for samples 1 and 2, respectively.

Here W , and L_D are width of the space charge region at the collector junction and diffusion length of electrons, respectively.

Note that the signal as a function of the width region W (see Fig. 1.) is more convenient for approximating experimental data, with d and L_D used as parameters. The accuracy of fitting is characterized by the values $d = 8.53 \pm 0.09$ (μm) and $1/L_D = 0.171 \pm 0.005$ ($1/\mu\text{m}$), obtained for sample 2.

In view of the high radiation hardness [6] and chemical resistance of SiC, structures of the above kind must be, in our opinion, of practical interest, e.g. for recording neutrons after their reactions with light elements, of the type $^{10}\text{B}(n, \alpha)^7\text{Li}$, accompanied by alpha particle escape.

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An Effective High Voltage Termination for SiC Planar pn Junctions for Use in High Voltage Devices and UV Detectors

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We had previously proposed a simple planar edge termination based on a field plate overlapping an oxide ramp at the periphery of the contact. This technique which was successfully tested on SiC Schottky barrier diodes is for the first time extended to *pn* junction barrier diodes (JBDs). Extensive numerical simulations have been carried out to design an optimum SiC oxide ramp termination. We have also fabricated high voltage 6H-SiC *pn* junctions and UV detectors to verify the efficiency of this termination.

From Table 1 one can see that indifferent of the doping/thickness of the *n* epitaxial layer, a near ideal 1D parallel-plane breakdown is obtained as long as the slope of the oxide ramp remains below 5°. A insulating sandwich consisting of an undoped oxide layer and an 8% phosphorus doped oxide layer with a total thickness of 1 µm has been successfully used in the fabrication of planar implanted 6H-SiC *pn* diodes. Experimental measurements indicate that an angle of less than 3° was achieved using two step wet etching, first in a standard oxide etch solution and then an overetching in a P-etch solution. As predicted by numerical simulations this angle results in uniform spreading of the potential lines in the proximity of the junction (see Fig. 1). The oxide ramp termination is not limited to Schottky or *pn* junctions but can be used as a general termination technique in any high voltage SiC devices.

The termination is also highly suitable for photodetectors and charged particle detection. UV detection properties of epitaxial 6H-SiC JBD with oxide ramp termination are illustrated in Figs. 2-4. Similar behaviours have been observed on Schottky barrier structures with the same epilayer and termination. The photocurrent (J_{ph}) is almost flat (Fig. 2a) and responsivity (R) increases linearly (Fig. 2b) over the spectral range from 250 to 350 nm. The highest responsivity (over 200 mA/V) is obtained at 320nm, which corresponds to a quantum efficiency about 75%. The responsivity increases with the increase in the bias voltage up to 10V and also with the decrease in the doping of the *n* epilayer. A weak dependence of R with the epilayer thickness and with the increase in the reverse bias over 10V can be observed. Fig. 3 shows the variation of the total current of JBD ($J(K)$) and the photocurrent (J_{ph}) with temperature. As expected $J(K) = J_{ph}$ up to elevated temperatures where the dark current is two to seven orders of magnitude less than the photocurrent. At temperatures higher than 800K thermal generation is comparable with photogeneration and the contribution of J_{ph} at $J(K)$ decreases. Therefore, one can conclude that the JBD with oxide ramp termination can perform as an effective high performance UV detector up to 800K. Fig.4 shows the transient photoresponse of the JBD with oxide ramp termination. During the pulse light time the photocurrent increases exponentially. It subsequently decays exponentially when the recombination process becomes predominant (Fig. 4a). The transient time within the depletion region and the necessary time of the carriers generated in the neutral region to diffuse to junction result in a considerable time delay between the pulse end and the time at which the current reaches its maximum value. The difference between this maximum value and the photocurrent value which corresponds to the uniform illumination for reverse biases smaller than the punch-through reverse voltage, is due to photogeneration and recombination outside the depletion region (Fig. 4).

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Table 1. Breakdown voltage versus oxide ramp for several n epilayer parameters.

N_d/x_e ($\text{cm}^3/\mu\text{m}$)	Breakdown Voltage(V)			
	Ideal	Ramp 2°	Ramp 5°	Ramp 10°
$2 \times 10^{15} \text{cm}^3/25\mu\text{m}$	3700	3475	3275	2925
$2 \times 10^{15} \text{cm}^3/8\mu\text{m}$	1465	1460	1420	1350
$8.5 \times 10^{15} \text{cm}^3/8\mu\text{m}$	1335	1255	1195	1055

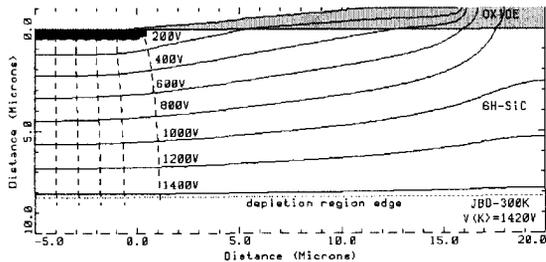
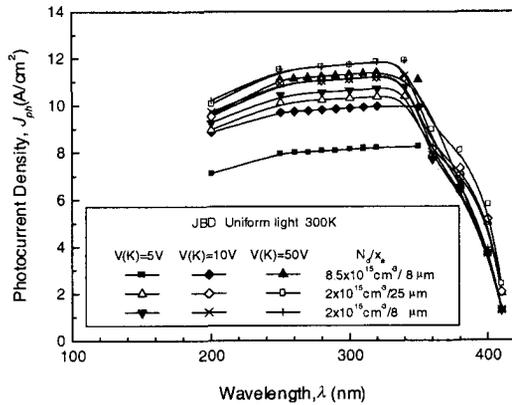
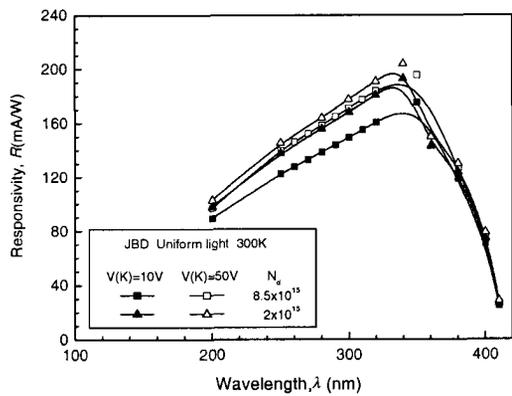


Fig. 1. The potential distribution at breakdown voltage of JBD with $N_d = 2 \times 10^{15} \text{cm}^3$ and $x_e = 8\mu\text{m}$.



(a)



(b)

Fig. 2.(a) Photocurrent density and (b) spectral responsivity versus wavelength for several reverse biases of JBD with different n epilayer parameters. The incident photon flux is $10^{20} \text{cm}^{-2} \cdot \text{s}^{-1}$

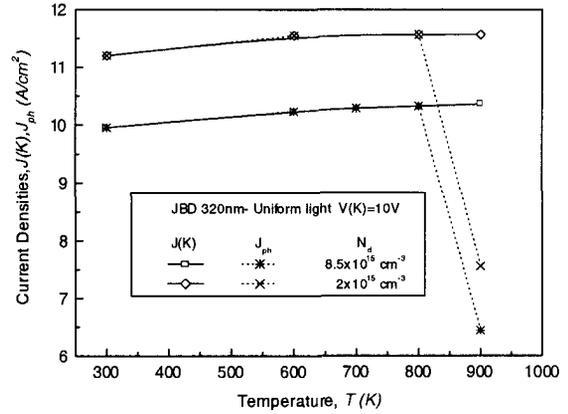
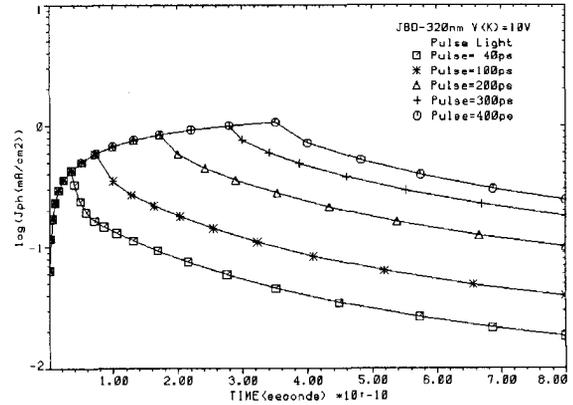
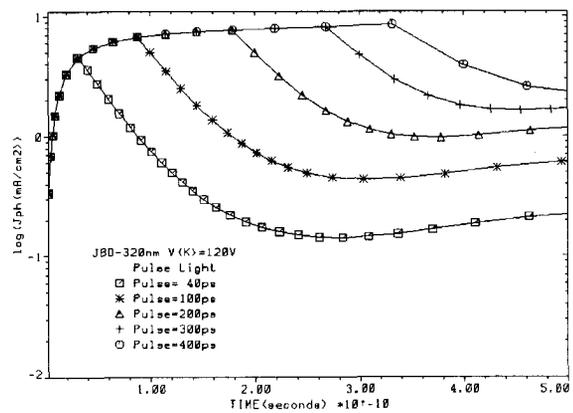


Fig. 3. Total current $J(K)$ and photocurrent (J_{ph}) as a function of temperature for uniform illuminated JBD with an incident photon flux of $10^{20} \text{cm}^{-2} \cdot \text{s}^{-1}$, having $\lambda = 320 \text{nm}$.



(a)



(b)

Fig. 4. Photocurrent density response at different light pulse excitation (with $\lambda = 320 \text{nm}$) of JBD reverse biased at: (a) 10V and (b) 120V (punch-through voltage).