

High Frequency Device

4H-SiC IMPATT Diode Fabrication and Testing (Invited)

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High-Performance Silicon Carbide MESFET Utilizing Lateral Epitaxy

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Hot-Carrier Luminescence in 4H-SiC MESFET's

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Development and Demonstration of High Power X-Band SiC MESFETs

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Influence of Semi-Insulating Substrates Purity on the Output Characteristics of 4H-SiC MESFETs

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Demonstration of IMPATT Diode Oscillators in 4H-SiC

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4H-SiC IMPATT Diode Fabrication and Testing

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Recent progress in 4H-SiC material characterisation, epitaxial growth and device processing paved the way to design and fabricate 4H-SiC IMPact-ionisation Avalanche Transit-Time (IMPATT) diodes. This paper reports on the fabrication and testing of pulsed 4H-SiC IMPATT diode.

Commercial 4H-SiC $p^+ - n - n^+$ epitaxial wafers from Cree Inc. were used to fabricate the diodes. The n layer had a donor concentration of $1.1 \cdot 10^{17} \text{cm}^{-3}$ and a thickness of 2 μm , which is close to the thickness of the space charge region at avalanche breakdown. The acceptor concentration in the 1 μm thick p^+ layer was equal to $8 \cdot 10^{18} \text{cm}^{-3}$. A rapid thermal annealing of Ni containing metal compositions was used to form ohmic contacts to p- and n-type 4H-SiC. This technique provides low resistivity contacts

($\sim 3 \cdot 10^{-5} \Omega \cdot \text{cm}^2$) suitable for further overlay deposition and bonding. The structure of these contacts investigated by x-ray phase analysis is shown in Fig. 1. Another key issue of IMPATT diode device processing is a p-n junction edge termination, due to its operation at high current, high voltage, and high temperature. The edge termination by mesa structure with no sidewall surface passivation was chosen as a most convenient technique for this diode. The mesa structures with different areas were formed by reactive ion etching in SF_6/Ar gas mixture. Test samples with polished backside were fabricated to investigate the initial breakdown localisation by direct observation of the electroluminescence (Fig. 2). This investigation shows an evident correlation of preliminary breakdown with the state of sidewall surface. The RIE process was optimised to obtain contamination free, smooth surface of the sidewalls.

The diodes had breakdown voltages of 300 V and series resistivities of $6 \cdot 10^{-5} \Omega \cdot \text{cm}^2$.

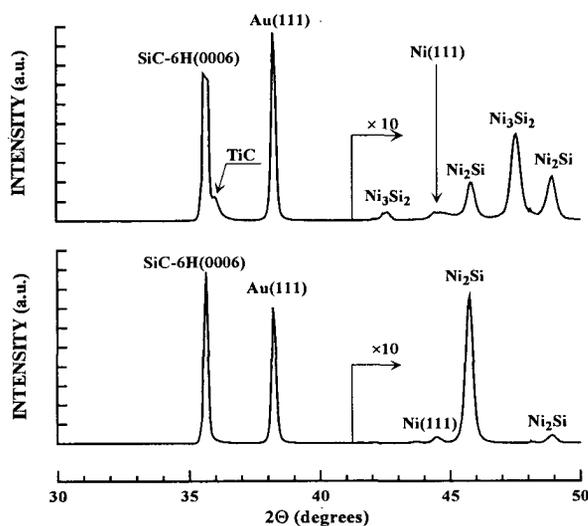


Fig. 1. X ray phase analysis of ohmic contacts to p- (top trace) and n-type SiC (bottom trace) formed on test 6H-SiC samples after Au overlay deposition.

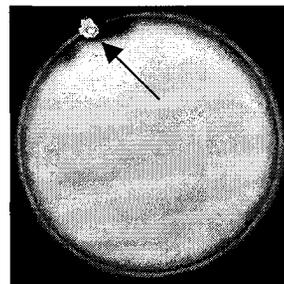


Fig 2. Electroluminescence (EL) of 4H-SiC diodes (mesa diameter of 200 μm) with preliminary breakdown. For localisation of breakdown point, EL under forward bias and at the breakdown shown by arrow are superimposed in one image.

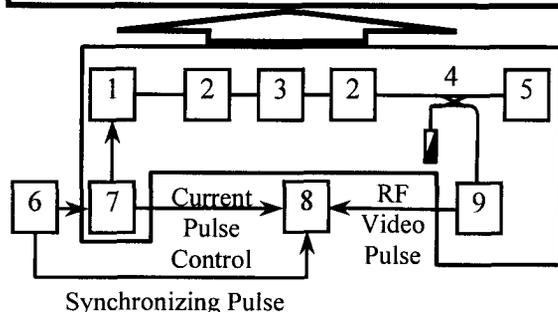
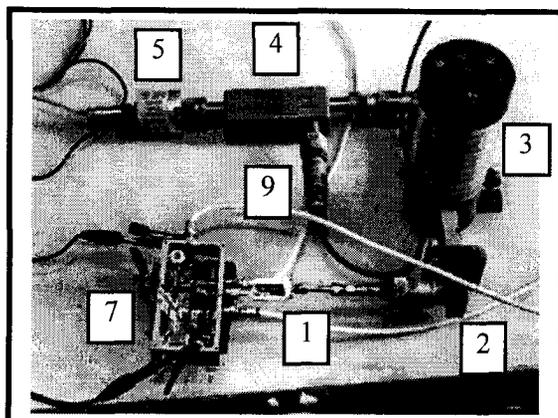


Fig. 3. View and block diagram of the experimental setup for measurement of operating frequency and output power of pulsed SiC IMPATT oscillator. 1- microstrip oscillator; 2- coaxial waveguide junction; 3- cavity-resonator wavemeter; 4- directional coupler; 5- microwave power meter; 6- pulsed voltage master oscillator; 7- pulsed current source; 8- two channel oscilloscope; 9- microwave pulse detector.

A maximum dc current density of 950 A/cm^2 was passed through the diodes. It is much lower than the anticipated operating current density of SiC IMPATT diode. For this reason, microwave measurements were done in pulse mode. The diodes were biased with dc avalanche current of 100 nA to charge the capacitance of the $p-n$ junction. Then, the current pulses were applied to the diode. The shape of pulsed current and voltage was controlled by the oscilloscope.

For microwave measurements, the diodes were mounted in broad band microstrip oscillators, since the operating frequency of the diodes was expected to be from about 6 to 20 GHz. A special design of the microstrip oscillator was performed to meet the very high breakdown voltage of SiC IMPATT diodes. Fig. 3 shows an experimental setup for measurement of operating frequency and output power of pulsed SiC IMPATT diodes.

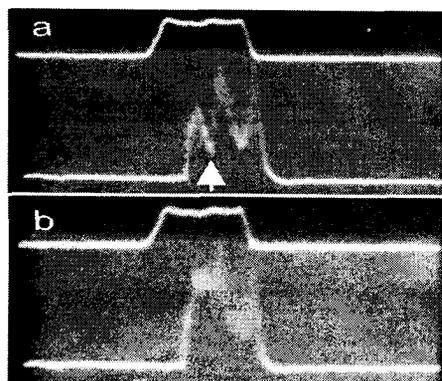


Fig. 4. The oscilloscope patterns of input current pulse (top trace) and corresponding output power video pulse (bottom trace) taken at various positions of cavity-resonator wavemeter; (a) 9.9 GHz, recess due to power absorption by wavemeter is shown by arrow; (b) 9.0 GHz, no recess on video pulse.

The microwave oscillations appeared when an input current of 0.3 A was passed through the diodes with mesa diameter of $80 \mu\text{m}$. The corresponding threshold current density was 6 kA/cm^2 . The frequency of oscillations was in X-band ($8.2\text{--}12.4 \text{ GHz}$). A microwave power of about 300 mW was measured at the pulse current of 0.35 A and pulse width of 40 ns . The self-heating of the $p-n$ junction led to the change of the diode impedance and load matching conditions during the pulse. This caused a delay of the front edge of microwave video pulse clearly seen in Fig. 4 and a frequency chirp through the pulse duration.

In conclusion, the measurements of operating frequency of SiC IMPATT diodes with specific doping profile provide the basis for their accurate numerical design. Simple frequency scaling of these experimental results shows that the maximum operating frequency of 4H-SiC IMPATT diodes (with $p-n$ junction plane oriented close to the basal plane) does not exceed 200 GHz . This dramatically changes a traditional opinion about advanced performance of SiC for fabrication of mm-wave IMPATT diodes.

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HIGH-PERFORMANCE SILICON CARBIDE MESFET UTILIZING LATERAL EPITAXY

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Silicon carbide is a promising material for high power microwave applications. A new generation of microwave power amplifiers is expected with introduction of silicon carbide device technology, however the results demonstrated so far do not meet theoretical expectations. There is currently no common opinion in literature on the origin of problems. In this report we demonstrate that the shortcomings of today's silicon carbide power microwave devices originate from the limitations of conventional MESFET design. We propose a new concept of silicon carbide MESFET with near-theoretical performance.

A high breakdown field in silicon carbide does not automatically result in high operation voltages of a microwave MESFET. This can be illustrated by simulation of a standard MESFET with a low-doped p-type buffer layer. A short gate length is desirable for efficient high-frequency operation, however a decrease of the gate length results in a dramatic drop of the blocking voltage, as it is seen in curve families plotted Figure 1. The low blocking voltage originates from short-channel effects, which result in the current bypassing the physical channel and in punch-through of a parasitic bipolar transistor, as it is illustrated by the 2-dimensional plots in Figure 2.

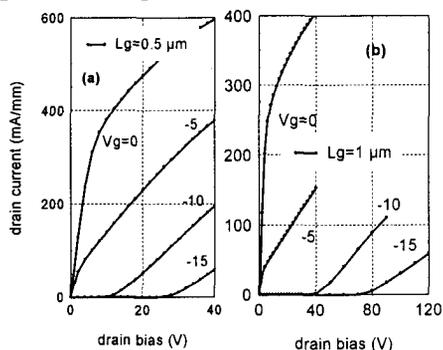


Figure 1. Simulated curve families for SiC MESFETs with uniform buffer-layer doping and a gate length of 0.5 μm (a) and 1 μm (b).

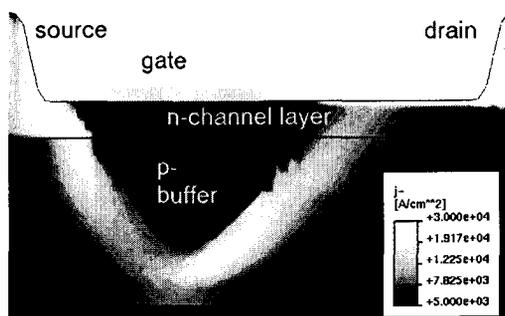


Figure 2. Simulated current contours for the source-to-drain punchthrough of SiC MESFET. $L_g = 1 \mu\text{m}$, p-buffer doping is $3 \times 10^{15} \text{cm}^{-3}$, drain and gate bias is $V_d = 100\text{V}$, $V_g = -15\text{V}$.

The reason for enhancement of short-channel effects in SiC is inherently related to the high breakdown field in SiC. A high electric field implicates a greater penetration of the electric field underneath the channel. The use of either a longer gate or a higher p-type doping in the buffer layer is required to suppress the short-channel effects, however both approaches deteriorate high-frequency device performance. Additional problems appear if the MESFET is formed on a semi-insulating (SI) substrate. Charge accumulation can develop in either the buffer layer or the adjacent semi-insulating material.

The MESFET concept proposed in the present work follows the approach of self-aligned silicon LD MOS design. Self-aligned lateral diffusion (LD) technique is employed in LD MOS fabrication to form a depletion stopper in the vicinity of the source and to suppress short-channel effects. In SiC the required self-aligned doping profiles can be achieved by lateral epitaxy (LE) onto the walls of pre-etched trenches

[1]. The material outside the trenches is removed by planarization. The active region is then deposited by CVD, and source, gate and drain contacts are formed, as it is shown in Figure 3. An important advantage of the design is the possibility of forming

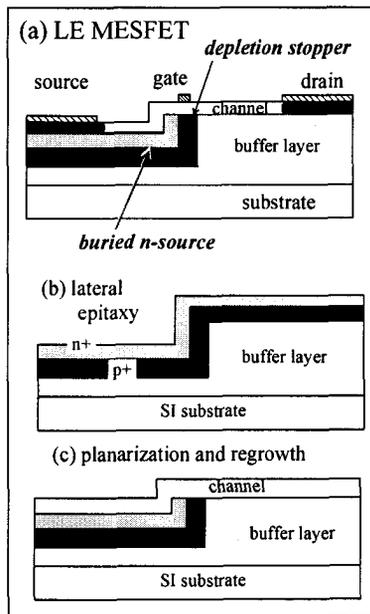


Figure 3. Cross-section of silicon carbide LE MESFET (a) and suggested fabrication scheme (b,c)

a buried source region. This minimizes the source resistance and compensates for relatively low electron mobility in SiC.

Simulations of LE (lateral epitaxy) MESFETs in 4H SiC show a dramatic performance improvement with this design. High electric field is terminated by the depletion stopper, as it is illustrated by the 2-dimensional plots of electric field in Figure 4. Inevitable electric field concentration at the gate edge has therefore no effect on the breakdown voltage. A gate of 0.1-0.3 μm is sufficient for switching a few hundred volts. The curve families for a 0.3 μm gate device show a very low output conductance and an average breakdown field of more than 200 Volts per 1 μm of the drift region length. The knee current is remarkably high due to the low source-to-gate resistance provided by the buried source design. The carrier trapping to the SI substrate is entirely eliminated in LE MESFET design, since the current pathway to the substrate is blocked by the depletion stopper.

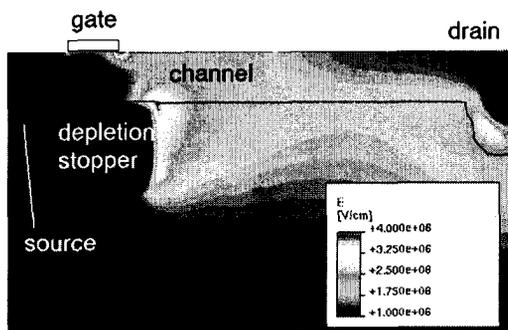


Figure 4. Contours of electric field for SiC LE MESFET simulated for $V_g = -10\text{ V}$, $V_d = 450\text{ V}$. Gate length is 0.3 μm , drift region length is 2 μm

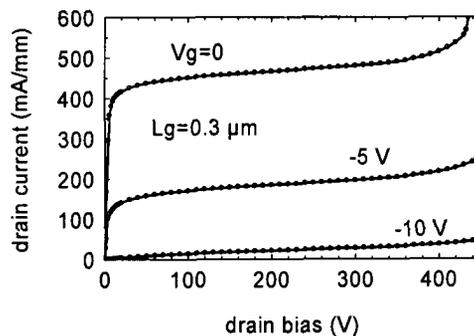


Figure 5. Simulated curve families for the LE MESFETs shown in figure 4

In the report we will discuss the dependence of LE MESFET performance on design features. The possibility of achieving a blocking voltage of up to 300 V/ μm using optimized drain/stopper doping profiles will be demonstrated. The gate length can be decreased below 100 nm without considerable drop of the transconductance. Practical implementation of LE MESFET technology will be presented in a separate report at this Conference. This work was supported by the Swedish Power Microwave Consortium and by the Naval International Cooperation Program, C. Wood, supervisor.

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Hot-carrier luminescence in 4H-SiC MESFET's

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We present the first experimental results of photon emission from MESFET's built on 4H-SiC. When the device is biased in the saturation regime, energy dissipation of the channel hot electrons is possible via two main mechanisms : optical phonon scattering and impact ionization. Additionally, some electrons loose their energy by undergoing radiative transitions which can be detected in the optical range using a photon emission set-up. Analysis of this emission is of particular interest : first, it allows one to detect and localize defects giving rise to excess leakage and premature breakdown in power devices and second, it is a useful tool when investigating the hot carrier properties of FET devices. In this study, we focus on the emission mechanisms and its link to impact ionization in SiC MESFET's.

The MESFETs (see Figure 1) were fabricated at Thomson-CSF/LCR. The channel is an n-type epilayer separated from the 300 μm thick semi-insulating 4H-SiC substrate by a p-type buffer layer. Substrate and epilayers were from Cree Research. For this study, gate lengths from 1 μm to 8 μm were investigated, the source/gate and drain/gate spacing were respectively around 0.5 and 2.5 μm . They are studied using a photon emission set-up already described in [1].

Summarized below are the main features which have been found :

- Light emission mechanisms in SiC MESFET's under high electric fields are strongly related to a midgap level (Figure 2). This level has already been detected in SiC MOSFET's in both 4H and 6H polytypes [1] and is responsible for a specific relationship between ionization currents and light intensity. We shall assume in this study that the relationship still holds in SiC MESFET's.
- When plotted as a function of gate voltage, the light intensity (I_v) follows a "bell-shaped" curve (Figure 3) which reveals its link with hot carriers relaxation in the channel. In contrast, gate currents are dominated by Schottky junction leakage (not shown here) and can not be used for hot carrier analysis. Further analysis allows us to extract the ionization coefficient B_i without measuring the gate current (Figure 4).
- The position of the maximum electric field in the drift region can be monitored (Figure 5) and its shifting towards the gate edge is demonstrated when biasing the devices towards pinch-off (Figure 6).

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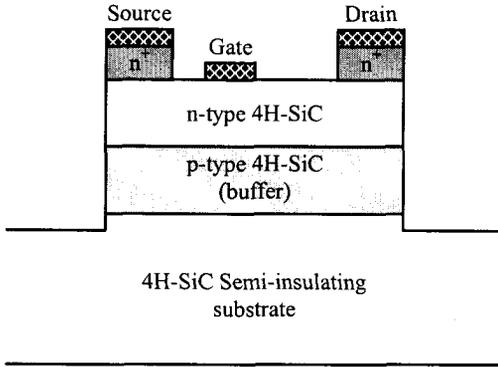


Figure 1 : Schematic cross-section of the studied devices.

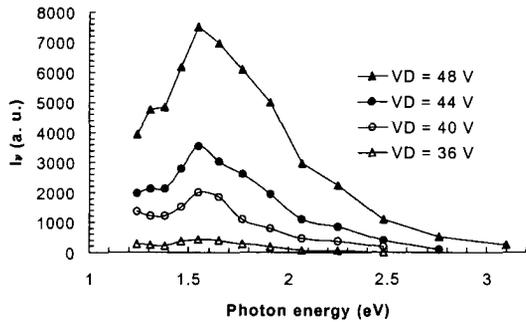


Figure 2 : Spectral analysis.

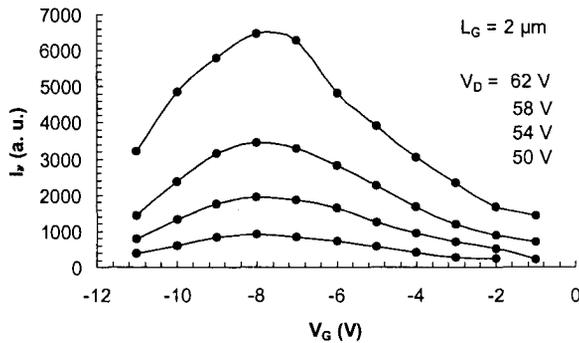


Figure 3 : "Bell shaped" behavior of the light emission.

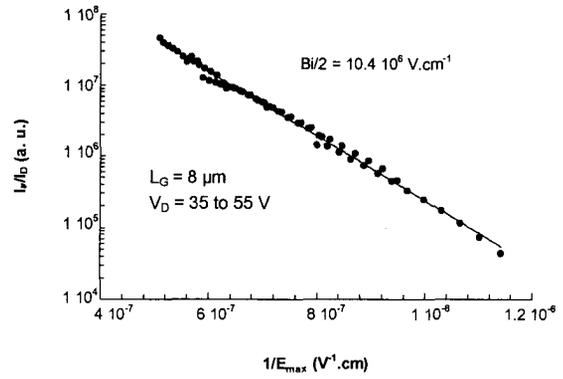


Figure 4 : Extraction of the ionization multiplication coefficient.

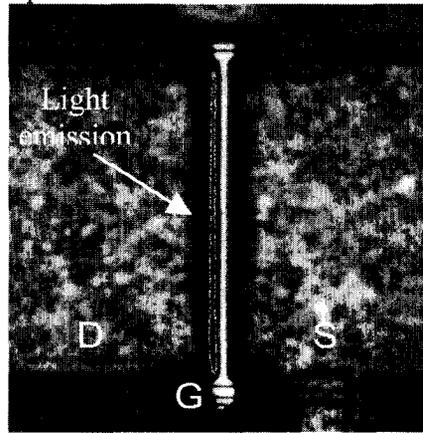


Figure 5 : Photon emission image of a device in the saturation regime superimposed on the same device under direct illumination.

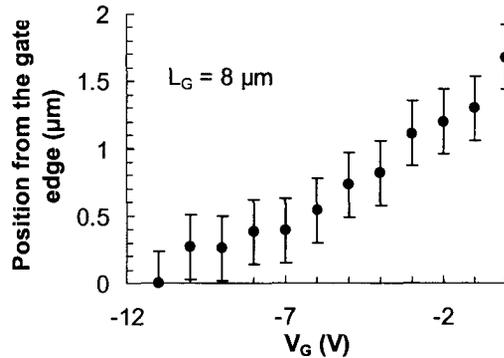


Figure 6 : Position of the electric field peak as measured by photon emission, as a function of the gate voltage.

Development and Demonstration of High Power X-Band SiC MESFETs

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Silicon Carbide (SiC) shows the promise to operate from VHF through X-Band frequencies while providing higher breakdown voltage, better thermal conductivity, and wider transmit bandwidths compared with Si or GaAs. Previously reported SiC MESFETs had small die sizes with gate widths in the range of 100s μm [1-3]. In this paper, we present for the first time the development of large SiC MESFETs with a gate length of 0.2 μm and a total width of 3.2 mm fabricated on semi-insulating 4H-SiC substrate, for high power communications applications. Devices showed a $f_T = 14.5$ GHz, $f_{MAX} = 38$ GHz, and a current gain of 16 dB at 2 GHz while biased at a high operating voltage of 40 volts.

MESFETs were fabricated on semi-insulating 4H-SiC substrate ($>10^5 \Omega\text{-cm}$). Epitaxial layers consists of an undoped buffer layer, 0.25 μm channel layer doped to $2.5 \times 10^{17} \text{cm}^{-3}$, and a 0.075 μm n+ layer doped to 10^{19}cm^{-3} . E-beam lithography was used to define a gate length of 0.2 μm . Fig. 1 is a microphotograph of a MESFET with 32-fingers. Air-bridges were used to interconnect the drain fingers of multifinger devices. Fig. 2 shows the DC characteristics of a 32-finger MESFET with a gate periphery of 3.2 mm; the maximum drain current can be seen is 400 mA. The DC transconductance, g_m , was measured to be 40 mS. These devices exhibit high gate-drain breakdown voltage of 150 volts and a blocking voltage gain of 10. A device yield of 20% was obtained for 50 mm diameter wafers.

Small-signal RF characteristics of these MESFETs were measured on wafer and with packaging. The small signal gain calculated from the S-parameters is shown in Fig. 3; a unity current gain frequency, f_T , of 14.5 GHz was observed. The measured S-parameters are being modeled using the conventional MESFET equivalent circuit model and will be reported in the full length paper.

In summary, we have demonstrated large SiC MESFETs with 3.2 mm gate width on semi-insulating 4H-SiC substrates. These devices show very high drain current while simultaneously providing a high operation voltage of $V_{ds}=100$ volts. These results demonstrate the advantage of 4H-SiC for high power microwave applications where its high thermal conductivity, high voltage and high power density capability are essential for a major reduction on system size/weight.

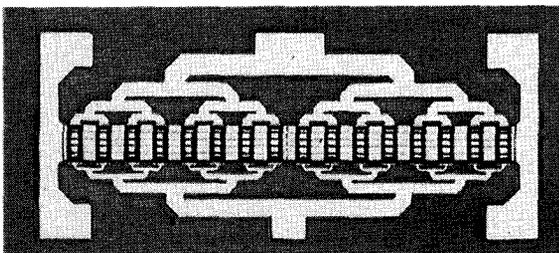


Figure 1. A photomicrograph of a SiC MESFET Die with a total gate width of 3.2 mm.

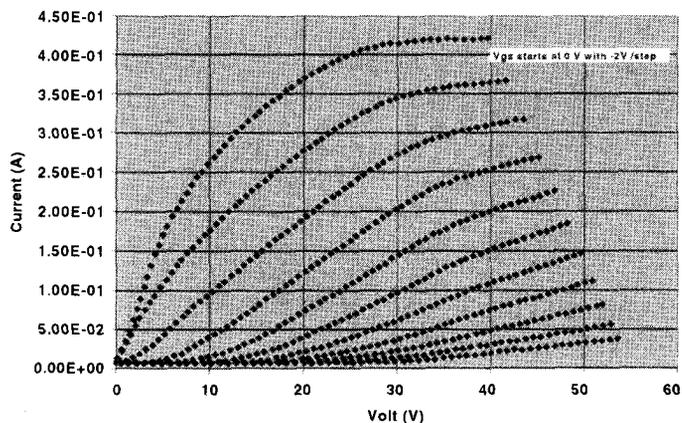


Fig. 2. DC characteristics of 3.2 mm periphery 4H-SiC MESFET. Top trace is for $V_g=0$ volt.

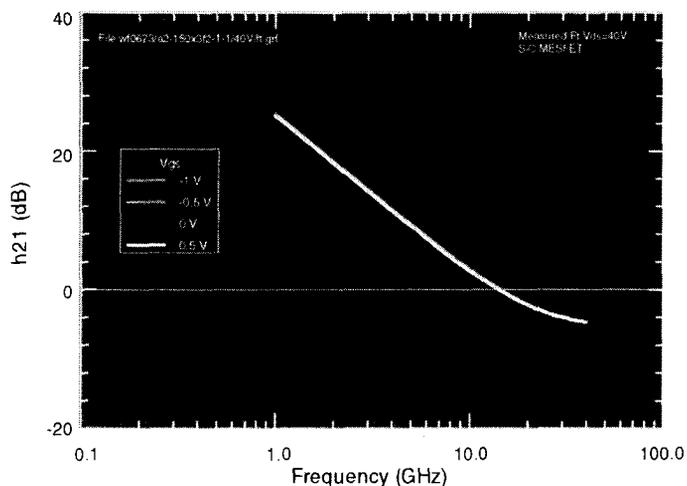


Fig. 3. Small-signal RF characteristics of 0.2 μm gate 4H-SiC MESFET for $V_d = 40$ volts, and $V_g = -0.5$ volts.

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Influence of Semi-Insulating Substrates Purity on the Output Characteristics of 4H-SiC MESFETs

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The ability of SiC for high power RF transistors has been demonstrated by impressive results. For instance, a power density of 4.6 W/mm [1] for a transistor with gate width inferior to 1 mm as been obtained, and, an output power of 80 W at 3 GHz as also been reported [2]. Nevertheless, in the latter case, the power density was only 1.67 W/mm. The origin of this power density reduction for large transistors in comparison to smaller ones has been tentatively attributed to trapping phenomena [3]. An other possible explanation is a self heating of the structure [4]. In this study we will focus on the first point : trapping phenomena. The development of 4H-SiC MESFETs for high frequency applications requires the use of SI substrates in order to reduce parasitic losses. For SI substrates obtained by physical vapor transport (PVT), the semi-insulating behavior is usually obtained by compensation of the conductive substrates by deep level incorporation such as vanadium. Some results on "vanadium free" substrates has also been reported, but deep traps with activation energy of 1.1 eV was also present in this material [5]. Recently an other source of high purity semi-insulating substrates obtained by HTCVD has appeared on the market [6].

Using different defect characterization tools we establish a correlation between the presence of deep defects in the substrate and defective operation in the static output characteristics of the MESFETs. The defects in the structure have been analyzed by DLTS measurement on the gate contact, frequency dispersion of the output conductance as a function of temperature and current transient spectroscopy.

I_{ds} - V_{ds} measurements as a function of temperature have been performed in the range 300 K – 600 K. Different parasitic effects have been observed for the transistors realized on PVT SI substrates. The major one, shown on Fig.1, is an hysteresis effect of the output conductance when the gate voltage is successively increased and decreased. This effect is enhanced for the high gate voltage (i.e. when the current flows near the substrate). When increasing the temperature the phenomenon progressively reduces and almost disappears at 500 K. A possible explanation for this hysteresis effect is the presence of deep centers which are at the origin of a parasitic gate under the channel.

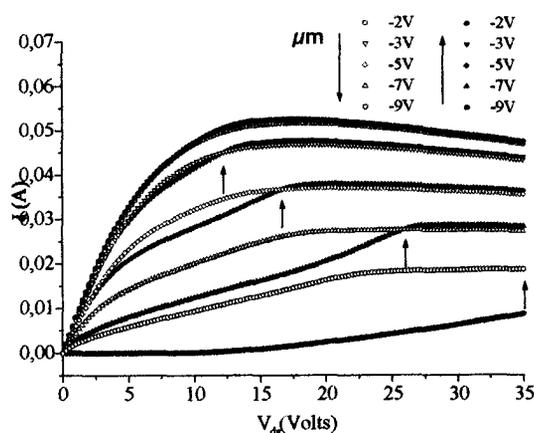


Figure 1 : Output characteristics at 300 K for a sample without buffer layer on a substrate realized by PVT. The hysteresis effect is materialized by the vertical arrows.

Random Telegraph Signal (RTS) measurements have next been realized. For samples without buffer layer, a strong RTS signal is obtained only for high gate voltage. This confirms the presence of traps near the channel/substrate interface.

In order to extract the trap signature, frequency dispersion of the output conductance has been performed in saturation regime ($V_g = -5V$, $V_{ds} = 5V$). The predominant trap detected by this measurement has an activation energy of about 1.1 eV (Fig. 2). The identification of this trap is not yet clear. The activation energy (1.07 eV) is close to the value measured by resistivity variation as function of temperature (1.18 eV) by Augustine et al. in the case of 4H-SiC SI substrates containing Vanadium [7]. Using the same measurement method, an activation energy of 1.1 eV was also found in the case of Vanadium free 4H-SiC SI substrates by Mitchel et al [5].

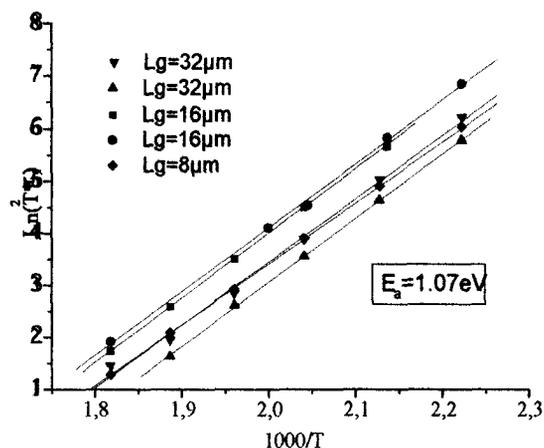


Figure 2 : Signatures obtained by frequency dispersion of drain source conductance measurements for a sample with p-type buffer layer.

From the results we have obtained, it seems clear that deep traps in the substrate are at the origin of parasitic effect on the output characteristics. Nevertheless, no evidence of defective operations in the output characteristics and no variation of the output conductance with frequency was observed in two cases :

- Firstly when an optimized buffer layer is used in order to prevent electron injection toward the substrate,
- Secondly when an high purity HTCVD SI substrate provided by Okmetic is used.

This confirms the role of the substrate purity on the devices performance and gives hope for developing 4H-SiC MESFETs technology.

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Demonstration of IMPATT Diode Oscillators in 4H-SiC

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Impact ionization avalanche transit time (IMPATT) diodes are used to generate RF power at microwave frequencies for applications such as pulsed radar. The RF power available from an IMPATT diode in the electronic limit is proportional to $(E_C \cdot v_s / f)^2$, where E_C is the critical field for avalanche breakdown and v_s is the saturation drift velocity. Since $(E_C \cdot v_s)$ in SiC is approximately 20x higher than in silicon or GaAs, the power available from a SiC IMPATT diode is theoretically about 400x higher than either silicon or GaAs.

We have fabricated both X-band and Ka-band IMPATT diodes in 4H-SiC [1,2] using the hi-lo doping structure shown in Fig. 1. In the X-band device, the p+ layer is $1.4 \times 10^{19} \text{ cm}^{-3}$ and $0.5 \text{ }\mu\text{m}$, the n avalanche region is $5 \times 10^{16} \text{ cm}^{-3}$ and $2.3 \text{ }\mu\text{m}$, while the n-drift region is $3.8 \times 10^{15} \text{ cm}^{-3}$ and $6.0 \text{ }\mu\text{m}$. As shown in Fig. 2, the static I-V characteristics exhibit stable avalanche breakdown at about 800 V reverse bias. Figure 3 shows the predicted operating characteristics of the X-band diode as a function of bias current density, as obtained from MEDICI simulations [1]. The maximum power is expected to be in excess of 3 kW at a bias current density of 8 kA/cm^2 , with an efficiency of 9 %.

Devices are mounted in a pillbox package, coated with silicone gel to prevent arcing, and tested in a microwave cavity as shown in Fig. 4. Bias pulses of 200 - 800 ns and up to 1000 V are applied through a series resistance, resulting in bias currents of 100 - 300 mA. Figure 5 shows the spectral output of an X-band diode [1,2]. Accounting for the 20 dB pad, the RF power is about 0 dBm (1 mW) at 7.75 GHz. The envelope of the voltage waveform across the $50 \text{ }\Omega$ input impedance of the sampling scope is shown in Fig. 6.

The maximum power obtained to date is about 300 mW at X-band. This power is lower than expected due to several factors: (i) to avoid destroying the diode, the bias current is about 5x lower than the optimum in Fig. 3, (ii) v_s parallel to the c-axis in 4H-SiC may be much lower than the $2 \times 10^7 \text{ cm/s}$ assumed in our design [3]; if so, the transit time across the drift region may not be optimum for X-band operation, (iii) our bias circuit does not maintain a constant current during the bias pulse (see Fig. 6), (iv) the diodes tested to date are not of the optimum area for best power, and (v) the microwave environment of the cavity and bias line are not fully optimized. We expect significantly higher power once many of these factors are resolved. Latest results will be reported at the conference.

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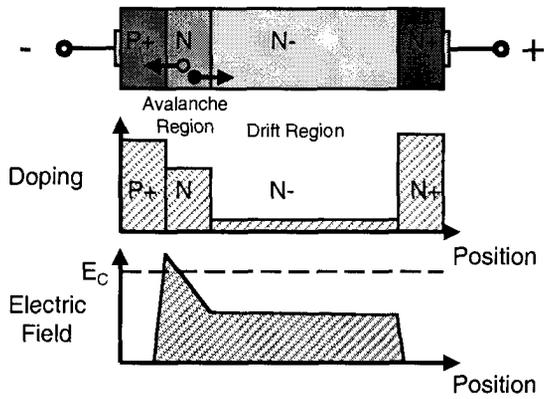


Fig. 1. Hi-lo doping structure and electric field profile of the SiC IMPATT diode.

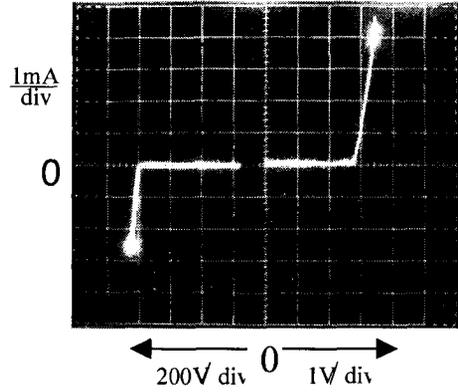


Fig. 2. Forward and reverse static I-V characteristics of the X-band diode.

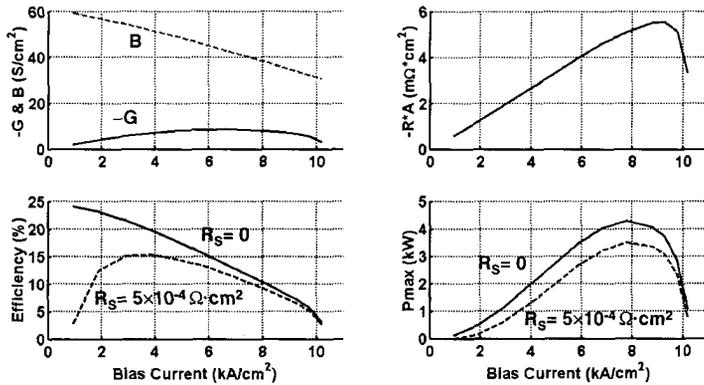


Fig. 3. Simulated admittance, negative resistance, efficiency, and power for the X-band IMPATT diode.

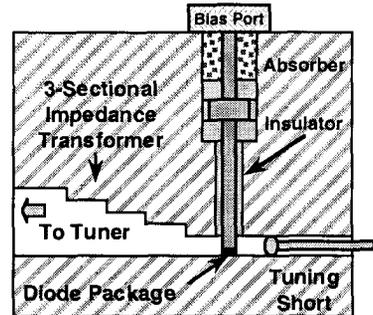


Fig. 4. Reduced-height waveguide cavity with bias port.

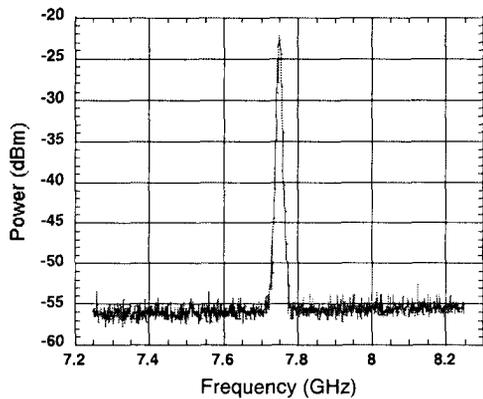


Fig. 5. Spectral output of the X-band IMPATT diode (measured with a 20 dB attenuator).

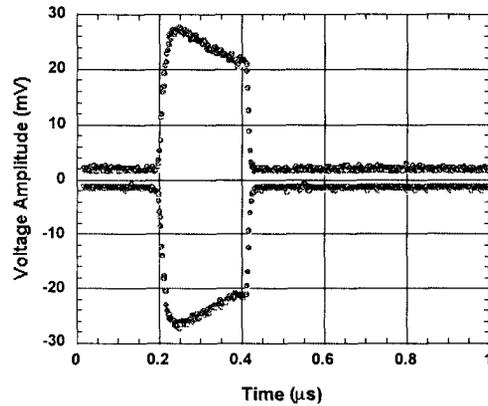


Fig. 6. Time domain envelope of the X-band IMPATT diode into the 50 Ω input of a sampling oscilloscope.