

Interfaces

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New Evidence of Interfacial Oxide Traps in n type 4H- and 6H-SiC MOS Structures

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Observation of Interface States in the Whole Band-gap Region at 6H-SiC(0001)/SiO₂ Interfaces by Means of X-ray Photoelectron Spectroscopy under Bias

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Characterization of the Interface SiC and Oxide Films by Spectroscopic Ellipsometry

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Measurement of the Interface Trap Density in SiC MOS Devices using the Hall Effect

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The conductance of SiC MOSFETs is currently limited by trapping of electrons in inversion layers at the SiC/SiO₂ interface. This trapping causes both a reduction in the number of free electrons and a reduction in the mobility of the remaining free electrons due to increased coulombic scattering. Trap profiles are currently characterized using capacitance-voltage (C-V) measurements using MOS capacitors on n-type SiC substrates (as opposed to p-type substrates used for n-channel MOSFETs), which makes C-V analysis more difficult and somewhat questionable.

Here we present a Hall effect technique for measuring the trap density without the drawbacks of C-V analysis. This technique has a major advantage in that the measurement is performed on the SiC MOS inversion layer and therefore the traps characterized are those which directly affect electron trapping and transport. Similar Hall effect analysis of interface traps was first discussed early in the development of silicon MOS devices [1] but was not widely adopted because the technique is too insensitive for accurate measurement of the low trap densities typical in silicon devices. The technique requires fabrication of an MOS Hall bar, which is basically a MOSFET with extra voltage taps.

In this technique [1], the Hall mobility μ_e and inversion layer electron density n_{inv} are measured as a function of the gate voltage V_{exp} . For each experimental value of n_{inv} , the surface potential $\phi_s(V_{exp})$ required to induce that value of n_{inv} is calculated. Then, for any two values of $\phi_s(V_{exp})$, it is also possible to calculate the theoretical *change* in gate voltage ΔV_{calc} required to cause this change in ϕ_s . The change in the number of trapped electrons Δn_t is then calculated from $\Delta V_{exp} = \Delta V_{calc} + q \cdot \Delta n_t / C_{ox}$ where $q = 1.6 \times 10^{-19}$ C and C_{ox} is the gate oxide capacitance. The trap density D_{IT} is obtained from $D_{IT}(\phi_s) = \Delta n_t / \Delta \phi_s$.

Results for $D_{IT}(E_{TRAP})$ for trap energy E_{TRAP} referenced to the conduction band edge E_c are shown in Fig. 1 for a 6H-SiC sample. $D_{IT}(E_{TRAP})$ was calculated using Fermi-Dirac statistics which is more accurate than Maxwell-Boltzmann close to E_c . Previous measurements using low-frequency C-V analysis of a similar sample from a different wafer from the same process lot are shown for comparison [2]. Below E_c , the trap densities increase with increasing trap energy, consistent with previously reported results [2,3]. At or above E_c , $D_{IT}(E)$ appears to flatten out or even decrease. Correlation with C-V results is reasonable. The Hall measurements clearly show far less scatter than the C-V results and are more accurate.

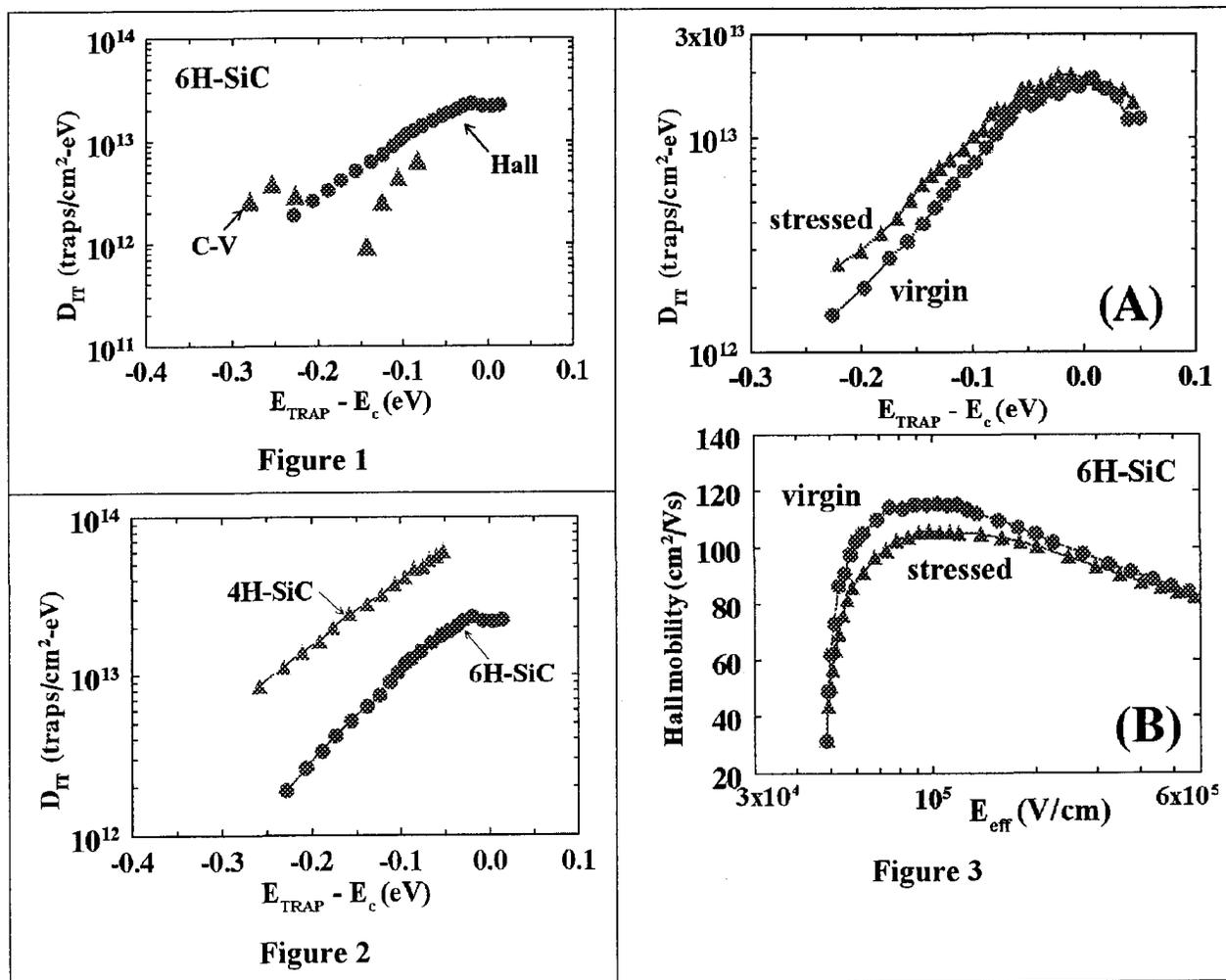
Trap profiles for 4H-SiC and 6H-SiC samples are compared in Fig. 2. Both samples show an increasing $D_{IT}(E_{TRAP})$ with increasing trap energy below E_c . $D_{IT}(E_{TRAP})$ is significantly higher (a factor of 4-5) in 4H compared to 6H-SiC, consistent with many previous results [4].

In Fig. 3, we report an example of the use of these Hall D_{IT} measurements. Results are obtained on a single 6H-SiC MOS Hall bar (A) before stress, or (B) after stressing by high-field constant-current injection of electrons into the gate oxide. Fig. 3A shows the increase in D_{IT} after stress. Fig. 3B shows the accompanying reduction in electron mobility, plotted as a function of inversion layer effective field. The mobility reduction presumably arises due to increased scattering from the higher density of trapped electrons. It is apparent that this method should be useful in studying similar behavior, such as the long-term reliability of SiC MOSFETs under operating conditions.

In summary, we have reported on the initial use of Hall effect measurements to characterize the Dit profile in SiC MOSFETs. This approach is found to be accurate, straightforward to implement, consistent with known behavior and previous results, and is promising for future experiments. Control experiments have also been performed on silicon MOS devices and the results will be presented at the conference.

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Passivation of the Oxide–4H SiC Interface

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Abstract: Current progress in the development of MOSFETs on 4H SiC is seriously hindered by high levels of interface traps that degrade channel mobility. However, it has been established that thermally grown oxides annealed in nitric oxide (NO) ambient provide critical improvements of the oxide–SiC interface: reduction of interface traps density [1-4], increased channel-carrier mobility [5], and increased reliability [6]. Chung *et al* [3] reported that the interface-trap density near the valence-band edge increases by about a factor of two following NO annealing. They speculated that a possible *passivation* of carbon atoms and carbon clusters by nitrogen causes shifts of interface-trap levels from the upper half of the energy gap to just above the top of the valence band. However, past [6] and present studies by our group have consistently demonstrated that NO annealing of dry oxide results in significant reduction of interface-trap density in the case of both N-type and P-type substrates. Figures 1 and 2 show that this reduction is especially pronounced around the midgap, in a direct analogy with the passivating effect of hydrogen in the case of SiO₂–Si interface. The main aim of this paper is to analyze and clarify the passivating role of nitrogen at the SiO₂–SiC interface.

The comparison of interface-trap distributions for dry, wet, and nitrated oxides (Figs. 1 and 2) leads to the following conclusions. **DRY OXIDES:** there are a high density of weak and strained bonds between trivalent silicon atoms from SiC and atoms in the oxide, resulting in energy levels around the midgap. **WET OXIDES:** Si-H and Si-OH bonds replace strained bonds, shifting the energy levels away from the midgap, however, not sufficiently to remove them from the wide energy gap of SiC (the shift is sufficient for the case of narrower energy gap of Si). **NITRIDED OXIDES:** much stronger Si≡N bonds are formed, their energy levels are much further from the midgap, and as a result, the levels appearing in the energy gap (interface traps) is significantly reduced. We have confirmed the existence of Si≡N bonds at the SiO₂–SiC interface by XPS analysis [7]. This analysis also revealed a small amount of C–N bonds, but they appear near the interface and could not be assigned a *passivating* role as assumed by Chung *et al.* [3]. In fact, we identified a number of experimental results indicating that C–N bonds are more likely to be associated with the nitrogen-assisted removal of carbon from the interface [8]. Therefore, we conclude that the Si≡N bonds play the passivating role at the SiO₂–SiC interface.

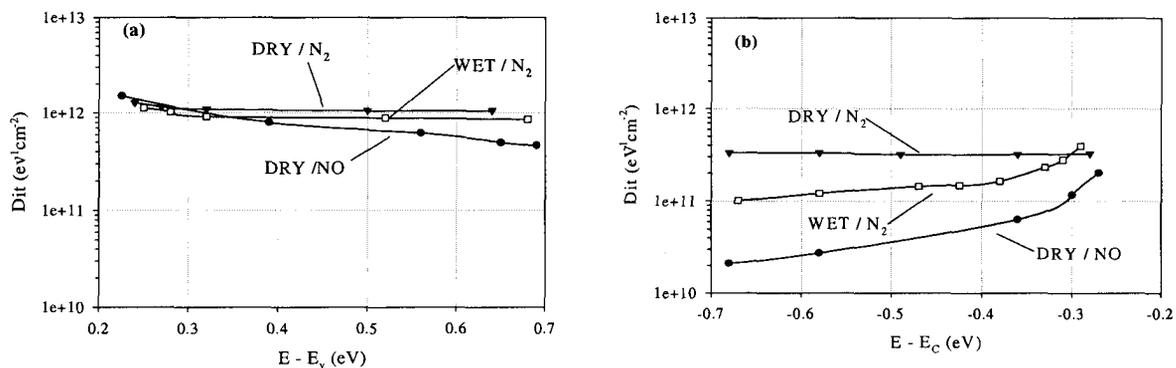


Fig. 1 Interface-trap distributions measured at 200°C by the conductance technique: (a) P-type, (b) N-type.

Much higher density of interface traps is commonly observed on P-type SiC substrates (also obvious in Figs. 1 and 2). We believe this is due to the inferior quality of these substrates, rather than strongly asymmetric distribution of the interface traps. This view is supported by the very large shifts of the C-V curves for MOS capacitors on P-type SiC (Fig.3a). Although this shift is probably due to both interface and near-interface trapped charge, the fact is that such large shifts are not observed with N-type substrates (Fig. 3b). The large reduction of the C-V curve shift in the case of nitrided oxides is probably, to a large extent, due to the nitrogen-assisted carbon removal. Nonetheless, Figs. 1 and 2 clearly reveal analogous and complementary interface-trap reduction for both P-type and N-type substrate, which can be explained by the passivating effect of Si≡N bonds.

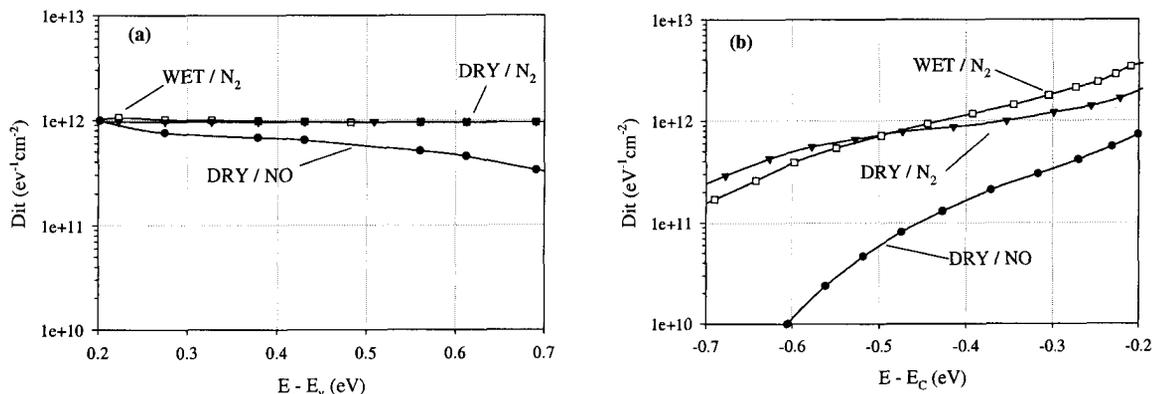


Fig. 2 Interface-trap distributions measured by the Hi-Lo CV technique: (a) P-type, (b) N-type.

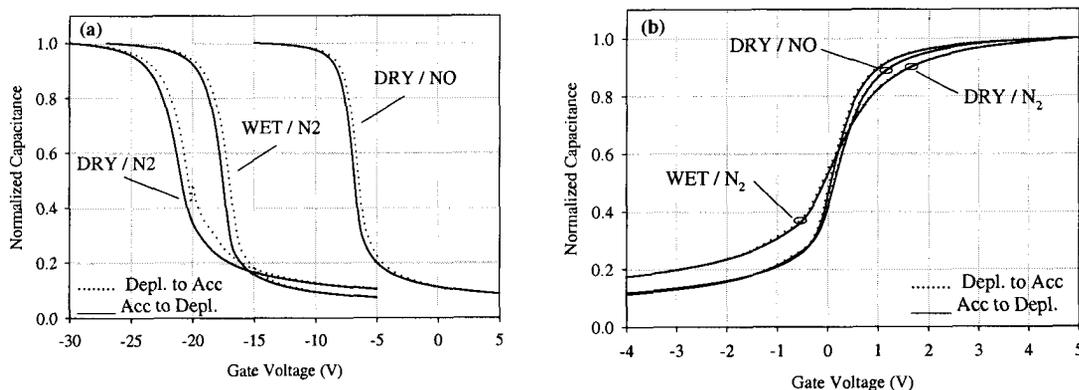


Fig 3 Normalized high-frequency C-V curves of wet, dry, and nitrided oxides: (a) P-type, (b) N-type.

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Improving 4H-SiC/SiO₂ Interface Properties by Depositing Si Nitride Layer Prior to Formation of SiO₂ and Annealing

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I. Introduction

Low channel mobility is known to be a major obstacle in commercialization of enhancement-mode 4H-SiC MOSFETs. Extensive studies have attributed the low channel mobility to high density of interface traps (Dit) near conduction band edge [1]. Recent studies have suggested that nitrogen incorporation in the SiO₂/4H-SiC system may have a significant impact on the interface properties [2]. In this study, we deposited an ultra-thin silicon nitride layer directly on 4H-SiC substrate prior to formation of SiO₂ and annealing, and found much reduced interface-trap density and oxide charge density. Our lowest Dit values are on the order of $1 \times 10^{12}/\text{cm}^2$ -eV or below at energies near the conduction band edge. XPS spectra confirm the presence of nitrogen at the SiO₂/SiC interface and suggest possible bonding between N and C.

II. Experimental

We use research grade n+-4H-SiC with a 10 μm epi-layer doped n-type to $2.6 \times 10^{15}/\text{cm}^3$. Following the standard RCA cleaning, SiC wafers were loaded into jet vapor deposition (JVD) chamber. Details of the JVD system and its operation can be found elsewhere [3]. The control samples are MIS capacitors with a ONO dielectric stack consisting of a 20nm-thick JVD silicon nitride sandwiched between two 10nm-thick JVD SiO₂ layers. The ONOn samples are basically the same as the control, except that they have an ultra-thin silicon nitride ($\leq 2.0\text{nm}$) layer deposited on SiC before the ONO stack deposition. The lower-case n in ONOn signifies an ultra-thin nitride layer, which was deposited in the same way as the thick nitride layer of the ONO stack [4], but with the SiH₄ flow rate adjusted to obtain optimized interface properties. The post-deposition-anneal (PDA) process consists of two steps: a 900 °C anneal in N₂ followed by a 950 °C anneal in a water vapor ambient, with each one lasting 1.5 hr. Al was used as the contacts. No post-metal-anneal was performed before electrical measurements. AC conductance measurements were carried out at room temperature to obtain Dit distribution. XPS spectra were taken on a sample with an optimized ultra-thin nitride layer at the interface and a 10nm SiO₂ on top. This sample resembles the ONOn /SiC interface but without the top O- and N-layers.

III. Results and Discussion

Figure 1 shows multi-frequency C-V curves measured on a capacitor with an ONO gate stack (right) and one with an ONOn stack (left). One can see that the addition of an ultra-thin nitride layer prior to ONO deposition sharpens significantly the slopes of these CV curves, even though the ultra-thin layer was not optimized in this sample. It seems more interesting that, compared to the control, the location where the strongest frequency dispersion occurs has shifted downward, suggesting that the energy of the peak Dit has shifted away from the conduction band edge, which should be beneficial for n-channel mobility. Encouraged by such results, we started a systematic study to optimize the effect of the ultra-thin interfacial nitride layer. Figure 2 compares the multi-frequency C-V curves of a set of samples whose interfacial silicon nitride layers were deposited with different SiH₄ flow rates. It is clearly seen that the frequency dispersion decreases systematically with decreasing SiH₄ flow rate, from 2 to 0.6 sccm, and the nitride layer deposited with a SiH₄ flow rate of 0.6sccm results in the best Dit data. Further decrease of the SiH₄ flow rate causes the C-V curves to degrade again, as manifested in the increased stretch-out and larger frequency dispersion near strong accumulation. The trend shown in Fig.2 suggests that a finite amount of Si is necessary at the interface to realize the beneficial effect, but excessive amounts of Si tend to reduce the beneficial nitrogen effect. Shown in Fig.3 are the Dit distributions of our JVD ONO and ONOn samples along with some published Dit data for comparison. As indicated by the solid triangles in Fig.3, our previous JVD ONO stack yielded Dit values no better than those samples made of conventional thermal SiO₂. However, with an ultra-thin silicon nitride layer added at the SiO₂/SiC interface, the Dit values in the energy range of 0.1 - 0.2 eV below the 4H-SiC conduction band are decreased over an order of magnitude, to $1 \times 10^{12}/\text{cm}^2$ -eV or below. To our knowledge, these are the lowest Dit values in this energy range that have ever been reported for 4H-SiC. Figure 4 shows the XPS spectra of, (a) N1s, (b) C1s, (c) Si2p, and (d) O1s, respectively, for a sample described in the **Experimental** Section. Despite its noisy appearance, Fig. 4(a) clearly shows the presence of nitrogen at the SiO₂/SiC interface for the ONOn sample. The binding energy of

398.3eV for N1s (~0.5eV higher than that for Si₃N₄) suggests that the ultra-thin silicon nitride layer may have evolved to an oxynitride other than a stoichiometric Si₃N₄ during the subsequent oxide deposition and PDA processes. It is also possible that some of the nitrogen atoms have bonded to C and/or Si atoms on the SiC surface, as the binding energies of the N1s peak also overlap the range for N1s in Cyanides (397.5-400.3eV). This latter possibility is supported by the broad tail on the higher energy side of the main C1s peak in Fig.4 (b). Comparing to rest of C1s spectra taken at shallower angles (not shown), this broad tail shows up only at the interface and the energy range of this tail overlaps that indicating C-N bonds. The main peak corresponds to absorbed carbon that exists throughout the depth of the film, which most likely originates from the pump oil vapor during the entire process of film deposition. Both the binding energies and the sharp, symmetric shape of the Si2p and O1s spectra shown in Figs. 4(c) and (d), respectively, demonstrate a quality SiO₂ with unnoticeable amounts of sub-oxides at the interface. The fitted Si2p spectrum in Fig. 4(c) reveals the contribution from the ultra-thin silicon nitride layer (represented by the small peak at 100.83eV) at the SiO₂/SiC interface, which is consistent with the information provided by the N1s spectrum in Fig. 4(a). However, possible contribution from the SiC substrate to this peak cannot be ruled out because the Si2p binding energies for Si bonding in SiC are coincident with energies for Si bonding in SiN_x (e.g., one silicon atom bonded to two nitrogen atoms). In summary, we have demonstrated significant reduction of interface-trap density near the conduction band edge by adding an ultra-thin layer of silicon nitride before gate oxide deposition. This reduction is possibly related to the presence of nitrogen at the SiO₂/SiC interface. More detailed and careful XPS study is necessary to correlate the electrical improvement to possible nitrogen passivation of Si and/or C dangling bonds at the interface.

Acknowledgement

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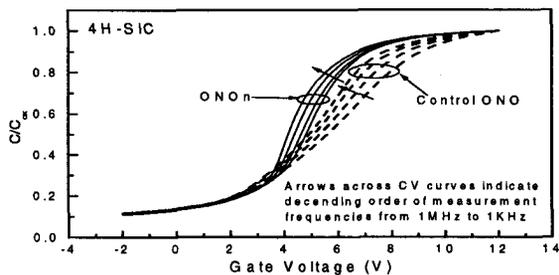


Fig.1 Multi-frequency C-V curves taken on JVD ONO & JVD ONOn samples

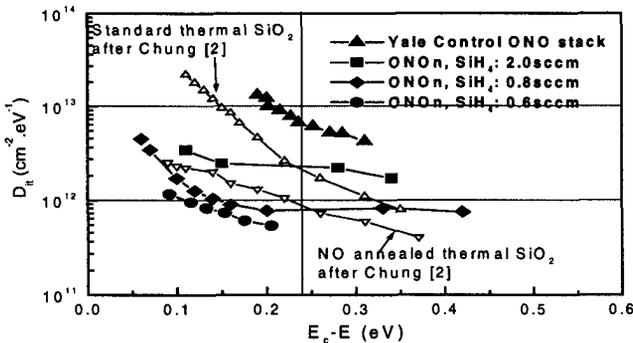


Fig.3 D_{it} distributions for JVD ONO control and ONOn samples with variable SiH₄ flow rate for the ultra-thin silicon nitride layer. Open symbols are reference data after Chung.

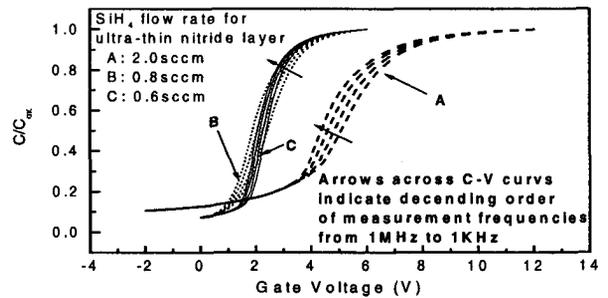


Fig. 2 C-V characteristics improved significantly with decreasing SiH₄ flow rate used for deposition of the ultra-thin interfacial silicon nitride layer

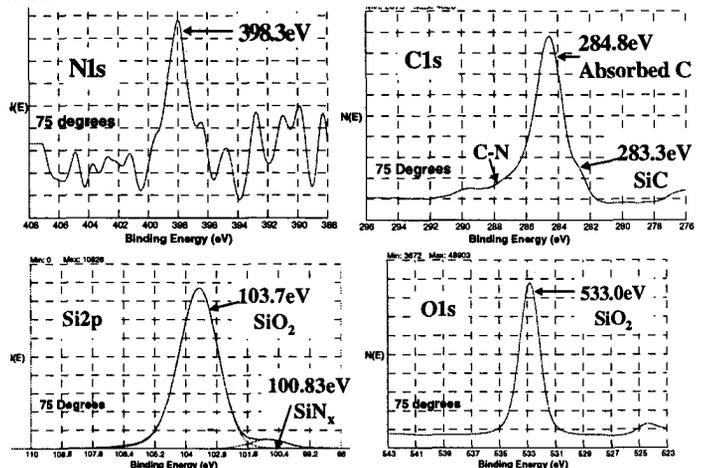


Fig. 4 XPS spectra of N1s, C1s, Si2p and O1s, respectively, taken at ONOn/4H-SiC interface.

New Evidence of Interfacial Oxide Traps in n type 4H- and 6H-SiC MOS Structures

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The great potential of silicon carbide MOS devices for high power and high temperature applications has thus far been hampered by insufficient quality of the oxide grown on SiC. A major concern in MOSFET SiC devices is the low electron channel mobility observed [1, 2]. One of the possible reasons is considered to be charge trapping in shallow interface states whose density is in general higher in 4H- than in 6H-SiC [2, 3].

In this work we study interface traps near the conduction band in n type 4H- and 6H-SiC metal-oxide-semiconductor (MOS) structures using the thermally stimulated current (TSC) technique. We find that differently prepared MOS capacitors show characteristic features in the TSC spectra, which cannot be ascribed to traps located immediately at the interface, and we assign these features to energetically shallow traps distributed in the oxide. The main difference between the TSC spectra observed for 4H- and 6H-SiC MOS structures is the manifestation of the oxide traps in a different temperature range.

Our MOS capacitors were fabricated on commercially available nitrogen doped 4H- and 6H-SiC epitaxial layers grown on the Si-face of SiC substrates and we compare oxides made using several oxidation procedures.

In the TSC technique, occupied trap levels thermally emit carriers which are detected as a displacement current. At a temperature T_0 , the MOS structure is biased with the charging voltage V_0 while the temperature is lowered to T_1 . The bias is then changed to the discharging voltage V_d , which usually corresponds to depletion at the interface, and the temperature is raised with a linear heating rate η while the current is measured. The volume and interface components of

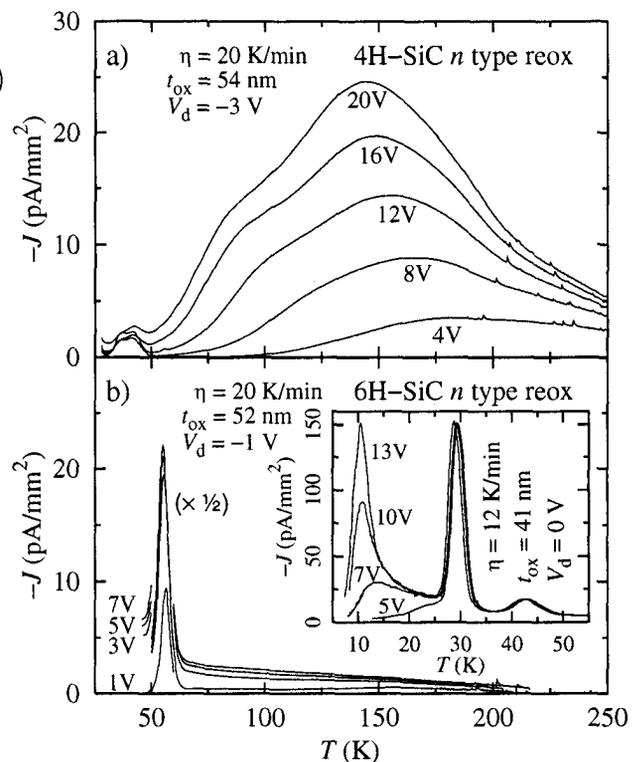


Fig. 1: TSC spectra for n type (a) 4H-SiC and (b) 6H-SiC MOS structures, measured for several charging voltages.

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the TSC spectrum are identified by comparing measurements with various charging and discharging voltages. In addition, MOS structures were characterized using high- and low-frequency capacitance-voltage analysis.

The oxides of the MOS capacitors used for the measurements in Fig. 1 were made by dry thermal oxidation at 1150°C for 4 h, immediately followed by a reoxidation anneal at 950°C in pyrogenic steam for 3 h. The resulting oxide thickness was t_{ox} . Fig. 1(a) shows TSC spectra from a 4H-SiC MOS capacitor, measured for several values of the charging voltage. The signal below 50 K is mostly due to volume states, namely the nitrogen donor in the cubic lattice site. Above 50 K the observed TSC signal comes from interface states. When the charging voltage corresponds to depletion at the SiC/SiO₂ interface, no current is measured in this temperature range. However, when the charging voltage allows accumulation at the interface, a signal appears which grows as the charging voltage increases. Furthermore, we did not observe the saturation of the interface-related TSC signal. This indicates, that the traps responsible for this part of the spectrum are most likely distributed in the oxide. In this case, it is natural to assume that the capture cross section should be very small and dependent on the electric field in the oxide. Thus, the energy levels of these traps could be expected to be close to the 4H-SiC conduction band, in spite of the fact that they are displayed in the TSC measurements at rather high temperatures. It should be emphasized that the typical features of the TSC spectra for our 4H-SiC samples was similar for differently prepared oxides. The observed border traps are possibly a signature of the native oxide defect described by Afanas'ev *et al.* [3, 4].

Fig. 1(b) shows typical TSC spectra of 6H-SiC MOS capacitors measured for different charging voltages. The behavior of the spectra is essentially different from that presented in Fig. 1(a). Here we observe a peak at 55 K which we assign to the nitrogen donor at the cubic lattice sites. Above 60 K the TSC signal is featureless and grows only slightly with increasing charging voltage. We attribute this signal to traps located immediately at the SiC/SiO₂ interface, since it vanishes if the charging voltage corresponds to depletion at the interface and its magnitude saturates as the charging voltage increases.

We expect that due to the bandgap difference between 4H- and 6H-SiC, traps observed in the temperature range from 50 to 250 K for 4H-SiC MOS capacitors, should be displayed at lower temperatures in 6H-SiC MOS structures. The inset in Fig. 1(b) shows measurements on a 6H-SiC MOS capacitor but for a lower temperature range. We assign the peaks at 30 K and 45 K to the nitrogen donor at the hexagonal and cubic lattice sites, respectively. For temperatures below 25 K we see a similar feature to the one found in Fig. 1(a). The TSC signal grows sharply with increasing charging voltage, while no current is measured if accumulation at the SiC/SiO₂ interface is not reached. We assign this signal to interfacial oxide traps and propose that it is associated with the same interfacial traps found in 4H-SiC samples at higher temperatures.

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Observation of interface states in the whole band-gap region at 6H-SiC(0001)/SiO₂ interfaces by means of x-ray photoelectron spectroscopy under bias

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1. Introduction

Interface states in the semiconductor band-gap play an important role in the determination of electrical characteristics of metal-oxide-semiconductor (MOS) devices. Because of the wide band-gap energy of SiC, interface states only in the limited energy region are observable by means of electrical technique such as capacitance-voltage (C-V) [1] and conductance-voltage (G-V) [2] measurements. In the present study, the noble spectroscopic method, i.e., x-ray photoelectron spectroscopy measurements under bias [3-5], recently developed by our group, is applied to the observation of interface states in the SiC band-gap. It is found that a sharp interface state peak is present for dry-oxidation, while it is not observed for wet-oxidation, and the peak is attributed to graphitic carbon at the interface.

2. Experiments

An SiC wafer consisted of a nitrogen-doped n-type SiC epitaxial layer of ~10 μm thickness with the donor density of 6x10¹⁵ cm⁻³ and a 6H-SiC(0001) substrate. After cleaning the wafer using the RCA method, an SiO₂ layer was formed by the heat treatments at 1050 °C either in wet-oxygen or dry-oxygen. Then, a 3 nm-thick platinum (Pt) layer was deposited using a thermal evaporation method, resulting in the <Pt/SiO₂/6H-SiC(0001)> MOS structure.

XPS measurements were performed using a VG SCIENTIFIC ESCALAB 220i-XL spectrometer with a monochromatic Al K α radiation source. During the XPS measurements, the front Pt layer was grounded and a bias voltage was applied to the rear SiC surface.

3. Results and discussion

Figure 1 shows the XPS spectra in the Si 2p region for the <Pt/SiO₂/6H-SiC(0001)> MOS structure. The asymmetric peak in the lower energy region is due to Si 2p_{3/2} and 2p_{1/2} peaks of the SiC substrate, and the broad peak in the higher energy region is attributable to the SiO₂ layer. From the ratio in the area intensity of these peaks, the SiO₂ thickness was estimated to be 3.1 nm.

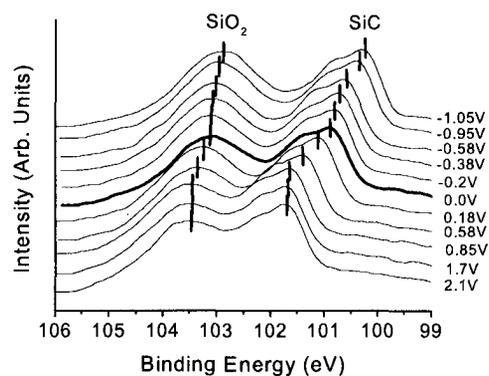


Fig. 1 XPS spectra in the Si 2p region for the <Pt/SiO₂/6H-SiC(0001)> MOS structure observed under various bias voltages applied to SiC with respect to Pt.

By the application of a positive bias to SiC, the peaks were shifted in the higher energy direction, while upon application of a negative bias, the peaks were shifted toward the lower energy. The shifts were completely reversible in contrast to chemical shifts, and they were attributed to charges accumulated in interface states by biasing. Namely, by the application of a positive (or negative) bias to SiC, the SiC Fermi level deviates downward (or upward) from the Pt Fermi level, and consequently interface states between the Pt and SiC Fermi levels are newly unoccupied (or occupied). The interface state charges induce a change in the potential drop across the SiO₂ layer, resulting in the shift of the SiC substrate Si 2p peak by the same magnitude. Therefore, by analyzing the shift of the substrate Si 2p peak measured at various bias voltages [3-5], the energy distribution of interface states can be obtained, as shown in Fig. 2. For the wet-oxidation, a broad interface state peak is present centered at 2.1 eV above the valence band maximum (VBM). For the dry-oxidation, an additional sharp peak was observed at 1.8 eV above VBM. A similar sharp peak was also observed when the wet-oxidation temperature was increased to 1150 °C, and in this case, the intensity of a C 1s

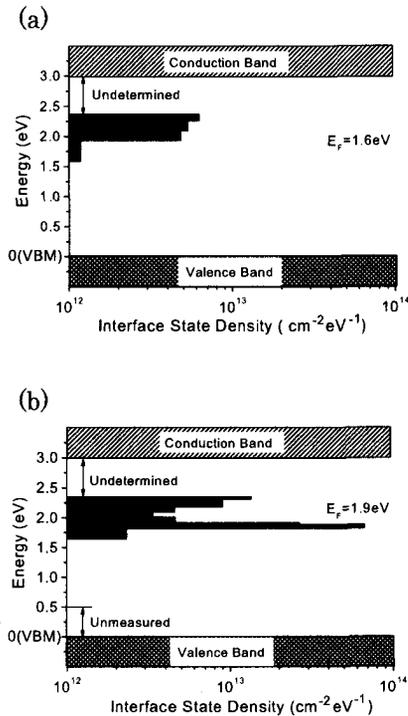


Fig. 2 Interface state spectra for the $\langle \text{Pt/SiO}_2/6\text{H-SiC}(0001) \rangle$ MOS structure with the ultrathin thermal SiO_2 layer formed in the following atmospheres: a) wet-oxygen; b) dry-oxygen.

peak due to graphitic carbon at the interface increased. Therefore, the sharp 1.7 eV-peak is attributable to interfacial graphitic carbon. It is previously reported that loss of Si occurs during high temperature thermal oxidation, resulting in the formation of graphitic carbon [6].

Figure 3 shows the current-voltage (I-V) curves for the $\langle \text{Pt/SiO}_2/6\text{H-SiC}(0001) \rangle$ MOS structure measured in the dark (solid lines) and under x-ray irradiation (dotted lines). Due to the ultrathin SiO_2 layers, the photo- and dark currents easily flowed. The I-V curve in the dark for the wet-oxide layer (curve a) was shifted in the negative bias direction from that for the dry-oxide layer (curve b). This shift is mainly attributable to the variation of the interfacial Fermi level, i.e., 1.6 eV above VBM for the wet-oxide layer and 1.9 eV for the dry-oxide layer. For the dry-oxide layer, the interfacial Fermi level is elevated because of the higher interface state density.

The I-V curve under x-ray irradiation for the wet-oxide layer was close to the ideal I-V curve shown by the dashed line [7]. This result is consistent with the relatively low interface state density. The I-V curve for the dry-oxide layer, on the other hand, deviated largely from the ideal curve. In Fig. 3, the points at the same SiC band-bending are denoted by A to C. The bias voltage at the same band-bending was determined from XPS measurements under bias. It is seen that the photocurrent densities for the MOS diodes with the dry- and wet-oxide

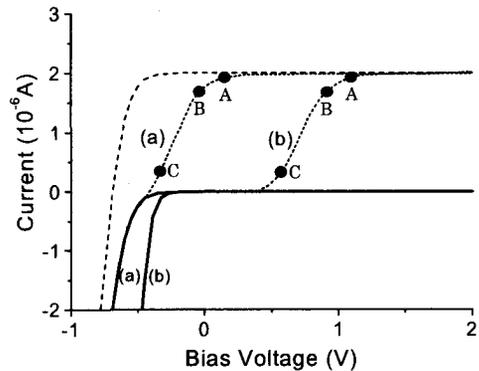


Fig. 3 I-V curves for the $\langle \text{Pt/SiO}_2/6\text{H-SiC}(0001) \rangle$ MOS structure in the dark (solid lines) and under x-ray irradiation (dotted lines) for the $\langle \text{Pt/SiO}_2/6\text{H-SiC}(0001) \rangle$ MOS structure with the ultrathin thermal SiO_2 layer formed in the following atmospheres: a) wet-oxygen; b) dry-oxygen.

layers are the same when the SiC band-bending is identical to each other. For the dry-oxide layer, the density of the interface state charges induced by the bias is high, resulting in a large potential drop across the SiO_2 layer, and consequently the net bias voltage applied to SiC is reduced. Namely, the deviation of the I-V curve from the ideal I-V curve is due to the charges accumulated in the interface states, but not due to the electron-hole recombination at the interface states.

4. Conclusions

Interface states in almost entire SiC band-gap region have been observed by means of XPS measurements under bias. For the wet-oxide layer, a broad interface state peak is present at 2.1 eV above VBM, while for the dry-oxide layer, an additional sharp peak attributable to graphitic carbon at the interface is observed at 1.8 eV above VBM. The I-V curve measured under x-ray irradiation shifts in the positive bias direction from the ideal I-V curve due to the charges accumulated in the interface states.

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Characterization of the interfaces between SiC and oxide films by spectroscopic ellipsometry

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SiC-MOSFET is expected to have two orders of magnitude smaller on-resistance (R_{on}) than those of Si-MOSFET at the same breakdown voltage. However, so far, such a small R_{on} has not been reported. For this reason, the electron mobility in the inversion layer is thought to be severely degraded, probably due to the residual carbon at the SiO₂/SiC interfaces. Diverse oxidation and annealing methods have been studied to improve characteristic of SiO₂/SiC interfaces. Many studies have been carried out to investigate the SiO₂/SiC interfaces by, for example, C-V, X-ray photoelectron spectroscopy (XPS) and secondary ion mass spectroscopy (SIMS) measurements. In the previous report, we have evaluated, for the first time, the optical constants of oxide films on SiC by spectroscopic ellipsometry[1]. In this study, we have measured the optical constants of oxide films on SiC by various oxidation ways by using spectroscopic ellipsometry, and have tried to elucidate the structure of SiO₂/SiC interfaces by comparing their refractive index-profiles.

6H-SiC epilayers, 5 μm in thickness and $5 \times 10^{15} \text{ cm}^{-3}$ in carrier concentration (n-type) (Cree, Inc.), were used for the measurements. The (0001) Si surfaces of SiC epilayers were oxidized by three processes, dry oxidation, pyrogenic oxidation and low temperature deposition of oxide (LTO) films. Dry oxidation was done in a pure O₂ flow at 1100°C for 16h. Pyrogenic oxidation was done in a hydrogen-oxygen flame at 1100 for 8h. LTO films were deposited by low-pressure chemical vapor deposition (LPCVD) at 400°C. The SiC substrates with the oxide layers were immersed gradually into diluted hydrofluoric acid of 8% at a constant speed to etch the oxide layers at an angle. By use of the sloped oxide films, we have measured the ellipsometric parameters (Ψ, Δ) along the slopes in the wavelength range between 250 and 850 nm at an angle of incidence of 75°. The optical constants of the oxide films, as well as the film thicknesses, assuming an optically single layer structure with uniform optical properties, were evaluated by the curve fitting of the calculated ellipsometric parameters to the measured ones. The wavelength-dependence of the apparent refractive indices of oxide films were assumed to follow Sellmeier's dispersion law, $n_{app} = \{1 + ((A^2 - 1) \lambda^2) / (\lambda^2 - B)\}^{1/2}$ and the extinction coefficient k was assumed to be equal to 0. The parameter A indicates the refractive index at infinite wavelength, while parameter B indicates the wavelength corresponding to an intrinsic oscillation.

Figure 1 shows the thickness distribution of a pyrogenic oxide film along the slope, which reveals the oxide film was etched at an angle. Figure 2 shows the thickness dependence of n_{app} for the oxide film by pyrogenic oxidation at the wavelength $\lambda = 630 \text{ nm}$. In the thick region, n_{app} increases with film thickness and approaches to the refractive index of bulk SiO₂ ($n = 1.465$). In the very thin region, n_{app} decreases steeply with decreasing film thickness, approaching to 1. In the both cases of dry oxidation and LTO films, n_{app} changes with film thickness as in the case of pyrogenic oxidation. These results suggest that the refractive indices of the oxide films are not uniform but change with depth from the surfaces. We have considered that the films consist of two layers, thin interface layer and SiO₂ layer on it, and found the thickness dependence of n_{app} can be explained by the changes of the thickness of SiO₂ layers, where the thickness of an interface layer is assumed to be 1nm and its optical constants are assumed to follow Sellmeier's dispersion law. We have evaluated the values of A and

B in the Sellmeier's equation for the refractive indices of interface layers, as well as the thickness of the SiO₂ layers by use of curve fitting method. Figure 3 shows the thickness dependence of the parameter A for various oxide films. All the values of A for three oxide films are higher than the refractive index of bulk SiO₂ (n=1.465). This means there exists thin interface layers with high refractive indices, which suggests the existence of bonds with large polarization, like Si-Si bonds at the interface. The figure reveals the values of A depend on the oxidation process, and the values for LTO films are smaller than those of pyrogenic and dry oxidation. It has been reported that the LTO films have lower interface state densities and effective oxide charge densities than those of thermally oxidized films [2]. These results suggest that the values of A of the interface may relate to the electrical properties of SiC MOS structures in some extent.

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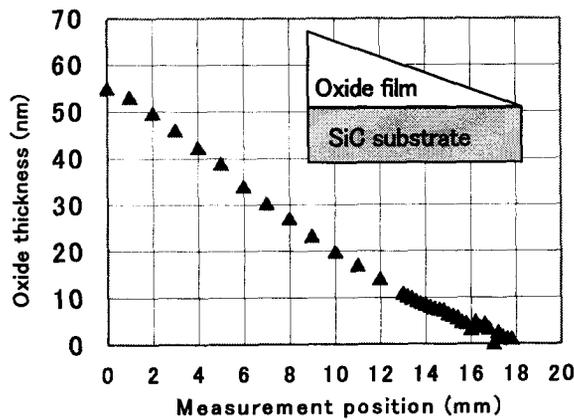


Fig.1. Variations of the thickness of a pyrogenic oxide film along the slope.

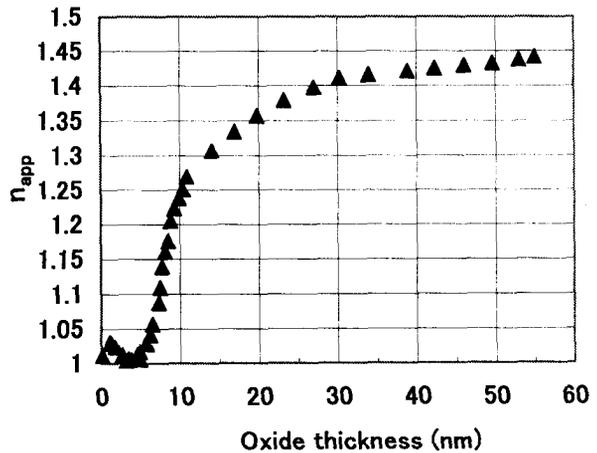


Fig.2. Thickness dependence of refractive index n_{app} for a pyrogenic oxide film ($\lambda=630\text{nm}$).

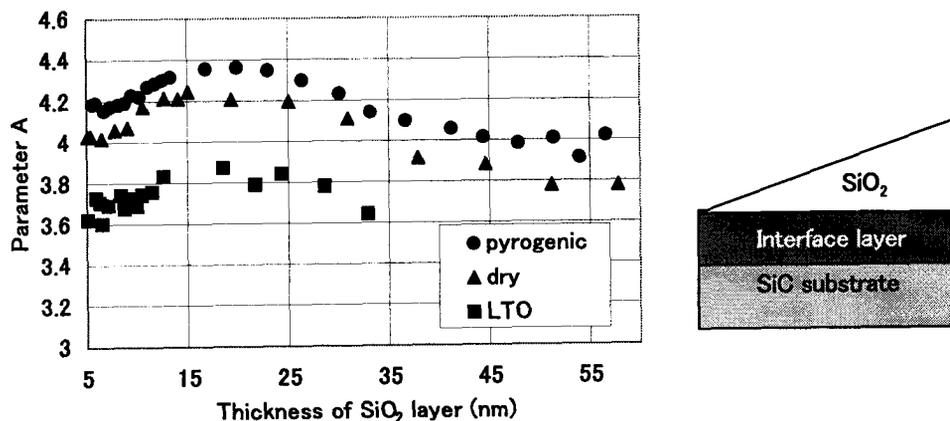


Fig.3. The values of the parameter A in Sellmeier's dispersion equation for LTO film, and pyrogenic and dry oxidation films.