

Electrical Properties I

Study of SiC PiN Diodes Subjected to High Current Density Pulses

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The Effect of Hydrogen Diffusion in p- and n-type SiC Schottky Diodes at High Temperatures

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Schottky Barriers for Pt on 6H and 4H SiC (0001), (000-1), (1-100) and (1-210) Surfaces Measured by I-V, C-V and Internal Photoemission

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Hall Measurements on Inversion and Accumulation-Mode 4H-SiC MOSFETs

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Quantitative High Resolution Two Dimensional Profiling on SiC by Scanning Capacitance Microscopy

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Scanning Capacitance Microscopy of SiC Multiple pn Junction Structure Grown by Cold-wall Chemical Vapor Deposition

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Study of SiC PiN Diodes Subjected to High Current Density Pulses

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In this work, SiC PiN power diodes subjected to single high density forward current pulses have been studied both experimentally and by means of computer simulations. Two sets of diodes were studied. One set of diodes was manufactured by ion-implanting the p⁺-emitter into an epitaxially grown n-base. The other set of diodes was manufactured by epitaxial growth of the p⁺-emitter on an epitaxially grown n-base. Both sets of diodes have a similar set of design parameters. The epitaxial diodes show superior high forward current density properties (i.e. lower power losses and larger SOA).

In the experimental studies the dynamic IV characteristics and the surface temperature have been measured, while the diodes were being subjected to single 1 ms half-sine-wave current pulses having a density in the range 100 to 6200 Amps/cm². The recorded dynamic IV characteristics of both epitaxial and implanted diodes show as a main feature the presence of a single loop that steadily increases as the peak current density is augmented and the power losses become larger. This differs from previous investigations carried out on lifetime engineered 3.3 kV Si power diodes [1]. The dynamic IV curves seem to be dominated by the decreasing mobility as both the carriers' density and the device temperature increase.

The diode surface temperature has been measured using an IR microscope designed and built in our lab [2]. In spite of the high thermal conductivity of SiC, it has been observed that, for current pulses 1 ms long, the heating of the device occurs under almost adiabatic condition, i.e. almost no heat is lost during the time that the current pulse is applied. This has also been observed for Si diodes [2], and it is a consequence of the high thermal impedance between the diode and the metal electrodes [2].

After repeated exposure to high-density current pulses, both epitaxial and implanted diodes showed signs of degradation resulting in the deterioration of the dynamic IV characteristics. Degradation is manifested as an increase in the peak voltage drop and also as a change in the shape of the voltage-drop-as-a-function-of-time curve that results in an ever increasing area of the loop displayed by the dynamic IV characteristics.

Diode degradation has been quantitatively studied by subjecting the diodes to single 1 ms long 3000 Amps/cm² half-sine-wave current pulses, and recording the current and the voltage signals as a function of time. These signals have in turn been related to the accumulated supplied energy. In this way the extent of the generated damage has been quantitatively correlated to the total supplied energy.

The experimental data obtained (i.e. dynamic IV characteristics and surface temperature) have been compared to the results from computer simulations performed using the two-dimensional device simulation package *AVANT! MEDICI*.

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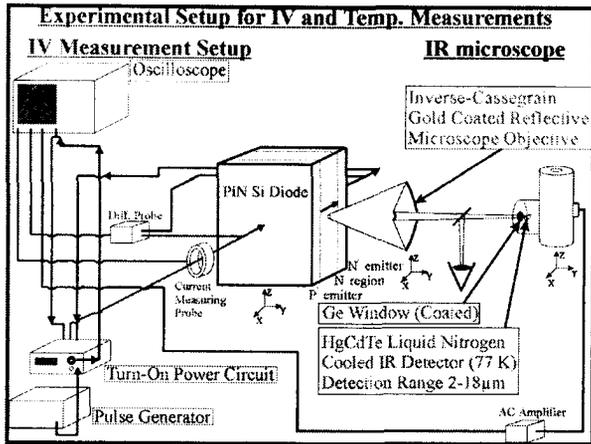


Fig. 1 Experimental set-up used to measure the diode's dynamic IV characteristics and the surface temperature as a function of position, time and current density.

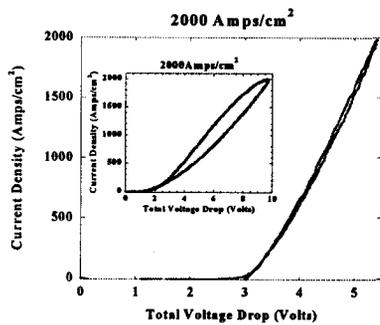


Fig. 2 Measured dynamic IV characteristics for a peak current density of 2000 Amps/cm² on an epitaxial diode. The size of the IV loop is negligible, indicating that the mobility is only slightly affected by the increase in carriers' concentration and temperature during the complete duration of the current pulse. As a comparison, the dynamic IV characteristics of a fast recovery 3.3 kV Si power diode [1] are shown in the inset.

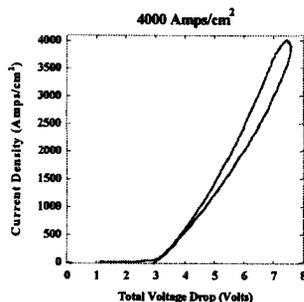


Fig. 3 Measured dynamic IV characteristics for a peak current density of 4000 Amps/cm² on an

epitaxial diode. The hysteresis in the IV curve caused by the decrease in carriers' mobility due to device self-heating can be clearly seen.

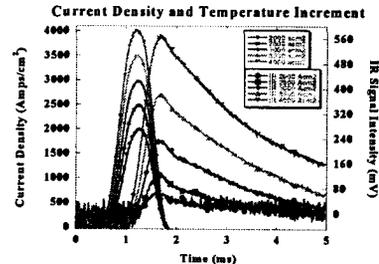


Fig. 4 Measured surface temperature as a function of current density and time on non-degraded diode. The peak temperatures are 101, 131, 166, 210 and 259 °C approximately.

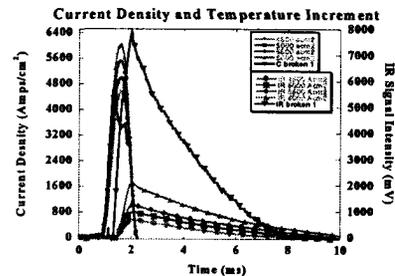


Fig. 5 Measured surface temperature as a function of current density and time on non-degraded diode. Observe the extremely large amplitude of the IR signal during the diode destruction pulse. This is an indication of large localized heating. The peak temperatures under normal operation are 302, 372, 454 and 570 °C approximately.

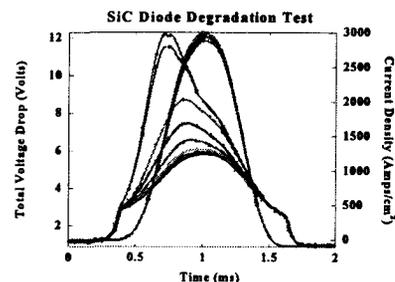


Fig. 6 Measured total voltage drop and current density as a function of time (degradation test). The total voltage drop increases as more energy is supplied to the diode. The curves have been recorded after 65.6 (700 pulses), 132.6 (1400 pulses), 201.9 (2100 pulses), 275.9 (2800 pulses), 358.2 (3500 pulses), 451.8 (4200 pulses) and 461.8 (4270 pulses) Joules have been dissipated by the diode.

The effect of hydrogen diffusion in p- and n-type SiC Schottky diodes at high temperatures

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Chemical gas sensors based on catalytic metal insulator silicon carbide, MISiC devices, have been operated at 600°C for extended periods and shortly up to 1000°C. The speed of response, when changing between an oxidising and reducing ambient at temperatures $\geq 600^\circ\text{C}$ is a few milliseconds. Applications like cylinder specific monitoring in exhaust gases of a car engine, synthetic exhaust diagnosis, and flue gas monitoring have been demonstrated [1]. Devices based on Schottky diodes as well as FET transistor devices have been used for the applications [1-3]. Here we present the effect of a hydrogen anneal at 600°C for Schottky sensor devices based on n- and p-type 4H SiC.

We have investigated MISiC Schottky devices with epilayers grown by hot wall CVD epitaxy ($N_d = 6 \times 10^{14} \text{cm}^{-3}$) [4], sublimation epitaxy ($N_d = 2.5 \times 10^{16}$) [5] and devices processed on p- ($N_a = 6 \times 10^{15}$) and n- type ($N_d = 4,5 \times 10^{15}$) wafers purchased from Cree [6]. The devices have gate contacts of porous Pt, Ta + Pt, or TaSi_x + Pt and ohmic back contacts of TaSi_x + Pt. A thin oxide, 1 nm, is grown on the SiC surface by ozone exposure before the gate metal deposition [1].

It has been shown by SIMS spectroscopy that Pt facilitate deuterium incorporation in p-type SiC at 600-800°C [7]. This is due to the fact that hydrogen or hydrocarbons dissociate on the catalytic metal surface of Pt and hydrogen atoms are formed, which diffuse through the metal and into the SiC in an oxygen deficient atmosphere at $T \geq 600^\circ\text{C}$. The hydrogen may trap at different impurities, such as compensational doping atoms, in the SiC lattice, which in turn will effect the net carrier concentration in a device. This will show up as a change of the IV characteristics of a Schottky diode. For the applications of the devices in, for example, measurements of the air to fuel ratio in exhaust gases the ambient changes within milliseconds between oxygen in excess and fuel in excess [1]. Here the hydrogen atoms are produced and consumed (hydrogen and oxygen forms water on the Pt surface) very fast and adsorbed atoms at the metal SiC interface give rise to a gas response rather than diffuse into the SiC. But it is anyhow of large importance to study the phenomenon of hydrogen diffusion in SiC.

A number of Schottky devices have been studied by recording the IV curves in an oxygen ambient at 400°C after annealing 4-15 hours in 2 % H₂ / N₂ or 2 % O₂ / N₂ atmosphere at 500 and 600°C. The temperature is lowered to 400°C in the annealing ambient. Figure 1 and 2 show the effect on the forward current of annealing at 600°C for an n-doped and p-doped sample, respectively. Hydrogen seems to reversibly increase the doping of the samples, which was valid for all measured samples at this temperature. Surprisingly enough the p-doped sample behaves similarly to the n-doped samples. The effects of the hydrogen anneal at 500°C is much smaller. Here the p-doped sample shows a deviating behavior, hydrogen in fact seem to slightly decrease the doping. Samples with epilayers processed by different growth methods showed some additional behavior, which will be further discussed. SIMS measurements will be performed on both p- and n-type samples, which have been exposed to deuterium, in order to try to understand the effect of hydrogen in the SiC lattice.

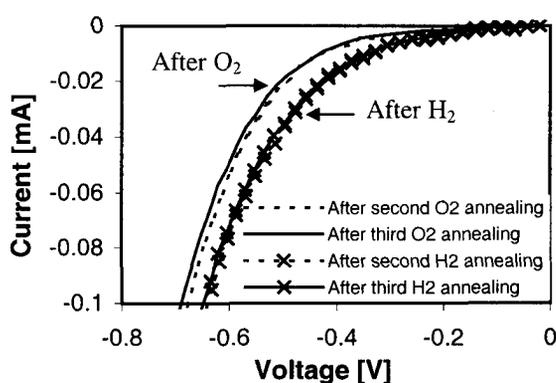


Figure 1. I-V characteristics at 400°C for a p-type Schottky diode after 4 h of annealing in hydrogen or oxygen ambient at 600°C.

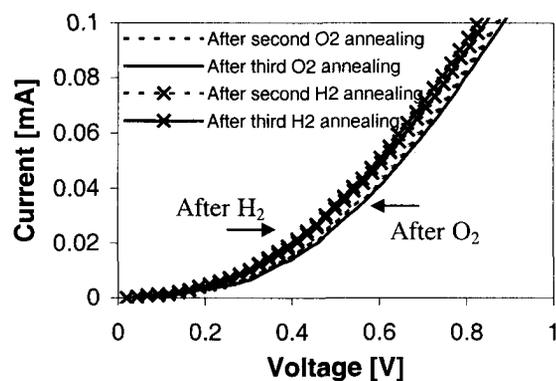


Figure 2. I-V characteristics at 400°C for an n-type Schottky diode after 4 h of annealing in hydrogen or oxygen ambient at 600°C.

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Schottky Barriers for Pt on 6H and 4H SiC (0001), (000-1), (1-100) and (1-210) Surfaces Measured by I-V, C-V and Internal Photoemission

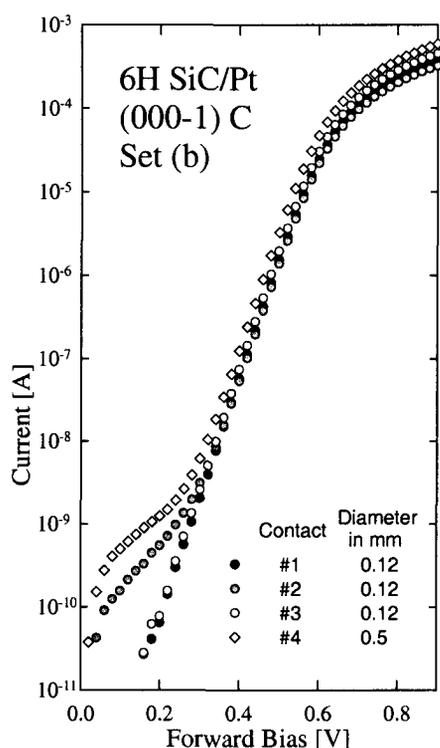
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Our measurements of the Schottky barrier heights (SBH) of 4H and 6H SiC/Pt contacts reveal a dependence on the crystallographic face of the SiC epilayer. The samples were prepared especially for this research. 6H and 4H SiC boule pieces were cut to make slices (thickness 0.5-1.0 mm) with the crystallographic faces (0001) (Si-face), (000-1) (C-face), (1-100) and (1-210). The Si- and C-face samples were cut 3.5° and 8° off <0001> towards <1-210> for 6H and 4H SiC, respectively, to optimize epitaxial growth. X-ray diffraction was used to accurately determine the orientations. The slices were mechanically polished down to 0.25 μm diamond and then chemical-mechanically polished at II-VI, Inc. The substrate doping concentration was 2-3×10¹⁶ cm⁻³ for 6H SiC and 5×10¹⁷ cm⁻³ for 4H SiC.



N-type homo-epitaxial layers about 10 μm thick were grown by cold-wall CVD at 1520°C. The doping concentrations are of order 10¹⁸ cm⁻³ for 6H SiC and 10¹⁵ cm⁻³ for 4H SiC. The surface morphology for (1-100) face samples was not as good (scratches, hillocks) as for the other three faces.

Ni ohmic contacts were fabricated on the front sides of 6H SiC samples (due to the low doping concentration of the substrate) and on the back sides of 4H SiC samples by e-beam evaporation followed by annealing at 1000°C for ten minutes. Pt Schottky contacts were fabricated by sputtering with Ar (0.9-2.0×10⁻⁸ torr base pressure, Pt 99.99% pure). Before deposition the samples were RCA cleaned, etched in HF for five minutes and rinsed in deionized water. The circular contacts are 0.12 mm and 0.5 mm diameter and 2000 Å thick for Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements, and 1.0 mm diameter and 100 Å thick for internal photoemission.

The apparatus for internal photoemission (IPE) spectroscopy includes a quartz tungsten halogen lamp source, a Jarrell Ash double monochromator (1180 l/mm grating, blazed at 6000 Å), an optical chopper and a lockin amplifier. The incident light power was measured with a Labmaster Coherent photon detector.

The figure shows I-V data on a semilogarithmic plot for four contacts on one of the (000-1) C-face samples. Extended regions of linearity are required for extraction of the Schottky barrier height.

Table 1 shows SBH for two different sets of 6H SiC samples, indicated as (a) and (b). Table 2 shows SBH for a single set of 4H SiC samples. For I-V and C-V measurements each sample has 4-20 contacts. For IPE measurements each sample has 1-4 contacts. The tabulated uncertainties, which are likely due to spatial inhomogeneity of the SBH [1], are based on both experimental uncertainty and the statistical distribution of values.

Table 1		Schottky Barrier Heights [eV]			
6H		(0001) Si	(000-1) C	(1-100)	(1-210)
I-V (n-ideality factor)	a	0.98±0.03 (n=1.15)	1.01±0.03 (n=1.15)	-	0.95±0.03 (n=1.21)
	b	0.92±0.05 (n=1.21)	0.94±0.03 (n=1.15)	0.89±0.03 (n=1.24)	0.82±0.03 (n=1.68)
C-V	a	1.37±0.05	1.46±0.05	-	1.31±0.05
	b	1.26±0.05	1.31±0.05	1.24±0.06	1.32±0.08
IPE	a	1.38±0.05	1.41±0.05	1.36±0.05	-

There are two trends in the dependence of the SBH on crystallographic orientation for 6H and 4H SiC. First, the samples with Pt on the (000-1) carbon face have higher SBH than the (0001) silicon face for all samples. This phenomenon was observed before [2,3], but to the best of our knowledge

Table 2		Schottky Barrier Heights [eV]			
4H		(0001) Si	(000-1) C	(1-100)	(1-210)
I-V (n)		1.34±0.03 (n=1.06)	1.41±0.04 (n=1.05)	1.35±0.03 (n=1.09)	1.33±0.03 (n=1.08)
C-V		2.10±0.09	2.13±0.05	1.93±0.15	2.03±0.08
IPE		1.43±0.05	1.45±0.05	1.62±0.05	1.55±0.05

there has not been a satisfactory explanation. Second, the samples with basal plane orientation ((0001) and (000-1)) have higher SBH than the samples with (1-100) and (1-210) orientations for the majority of the samples. The comparatively large SBH measured by

C-V for the (1-210) 6H SiC sample from Set (b) may be due to poor surface morphology. For this sample, there was only one high quality contact, which happened to have a high value for the SBH.

The relationship $\phi_B = S(\phi_m - \chi) + (1-S)(E_g - \phi_0)$, where ϕ_B is the Schottky barrier height, ϕ_m the work function of the metal, χ the electron affinity of the semiconductor, E_g the energy gap and ϕ_0 the pinning level due to interface states is commonly used to interpret measurements on Schottky barriers. The coefficient S provides an interpolation between the Mott-Schottky ($S = 1$) and Bardeen ($S = 0$) limits. SiC is an intermediate case. In this work, we are considering areal densities of (idealized) SiC surfaces with 0.122 Si atoms/cm² for (0001), 0.122 carbon atoms/cm² for (000-1), or equal areal densities of 0.064 and 0.074 Si or C atoms/cm² for (1-100) and (1-210), respectively. In addition, the ideal (1-210) surface is atomically flat, whereas the (1-100) surface is not [4]. The surface double layer, and correspondingly the double layer for the metal-semiconductor interface, will likely be different for each crystallographic face [5]. Surface passivation, reconstruction, contamination, defects, etc., may also contribute. The larger atomic areal densities on the (1-100) and (1-210) faces may give rise to larger electron affinities, and thus lower Schottky barriers, a trend displayed by the data in Tables I and II.

This work was partially supported by the Office of Naval Research (Contract N00014-01-1-0028) and the NASA Glenn Research Center (Contract NAG3-2538).

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Hall Measurements on Inversion and Accumulation-Mode 4H-SiC MOSFETs

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Inversion and accumulation-layer electron mobility in n-channel 4H-SiC MOSFETs have been investigated using the Hall effect. In the inversion-mode MOSFETs, Hall mobilities of ~ 60 - 70 $\text{cm}^2/\text{V}\cdot\text{s}$ were obtained compared to a field-effect mobility (μ_{FE}) of ~ 5 $\text{cm}^2/\text{V}\cdot\text{s}$. Accumulation-layer electron mobilities (μ_{acc}) of ~ 350 $\text{cm}^2/\text{V}\cdot\text{s}$ [1] and 200 $\text{cm}^2/\text{V}\cdot\text{s}$ were extracted on samples with different channel doping concentrations. In contrast, the μ_{FE} under accumulation was ~ 2 - 3 $\text{cm}^2/\text{V}\cdot\text{s}$.

N-channel inversion- and accumulation-mode MOSFETs were fabricated on the same chip, starting with p-type 4H-SiC epilayers. The channel region in the accumulation-mode MOSFETs was implanted using nitrogen with a total dose of 1×10^{12} cm^{-2} and 3×10^{12} cm^{-2} in the "wet" and "dry" oxide samples respectively.

Carrier concentration (N_{inv}) and Hall mobility (μ_{Hall}) were extracted with MOS-gated bar structures. Fig. 1 shows the N_{inv} vs. V_G in the inversion-mode MOSFETs on the "wet" oxide sample for temperatures ranging from 25°C to 125°C . N_{inv} increases with increasing temperature due to the reduced trapping of inversion carriers by the interface traps at higher temperatures. Fig. 2 shows μ_{Hall} vs. V_G in the wet oxide sample for different temperatures; μ_{Hall} increases from ~ 70 $\text{cm}^2/\text{V}\cdot\text{s}$ at 25°C to ~ 150 $\text{cm}^2/\text{V}\cdot\text{s}$ at 125°C . The increase in μ_{Hall} with increasing temperatures is attributed to a decrease in coulombic scattering. N_{inv} and μ_{Hall} obtained on the "dry" oxide sample had similar temperature behavior. The interface trap density ($D_{it}=d(Q_F+Q_{it})/d\phi_s$), extracted using Hall measurements, was slightly higher in wet oxide sample ($\sim 8 \times 10^{13}$ cm^{-2} eV^{-1} at $E_C-E=0.1\text{eV}$) compared to dry oxide sample ($\sim 5 \times 10^{13}$ cm^{-2} eV^{-1} at $E_C-E=0.1\text{eV}$) as shown in Fig. 3; the integrated trapped charge density in the wet oxide sample is larger.

N vs. V_G in accumulation-mode MOSFETs on the "wet" oxide sample extracted at temperatures ranging from 25°C to 125°C is shown in Fig. 4. At large V_G , under accumulation, the increase in N with temperature is due to the reduced trapping of field-induced accumulation electrons in the interface traps. Since the conduction of electrons occurs through both the bulk and a surface accumulation layer, μ_{Hall} extracted (Fig. 5) is a combination of the bulk and accumulation-layer mobility. μ_{acc} is extracted from the slope of the sheet conductance (σ_s) vs. N (as $(1/q)(d\sigma_s/dN)$). At room temperature, μ_{acc} in the wet oxide sample decreases from the bulk value (~ 350 $\text{cm}^2/\text{V}\cdot\text{s}$) to 200 $\text{cm}^2/\text{V}\cdot\text{s}$ in strong accumulation (Fig. 6). The decrease in μ_{Hall} and μ_{acc} with increase in temperature is attributed to phonon scattering. Similar results on N , σ_s , μ_{Hall} , μ_{FE} and μ_{acc} have been obtained on the dry oxide sample.

The large difference between μ_{Hall} and μ_{FE} in the inversion-mode MOSFETs and μ_{acc} and μ_{FE} in the accumulation mode MOSFETs is attributed to the trapping of the field-induced carriers in the interface traps. At higher temperatures, a larger fraction of the field-induced charge contributes to the conduction resulting in an increase in μ_{FE} . Dry oxidation results in a lower interface trap density in inversion mode MOSFETs compared to wet oxidation resulting in a better transconductance, lower threshold voltage, better sub-threshold characteristics and higher carrier concentration. This work, for the first time, has separated the bulk and surface mobility of electrons in accumulation-mode MOSFETs using Hall measurements.

Acknowledgements: Authors from RPI would like to acknowledge support of this work by Philips Research, MURI, DARPA and CPES.

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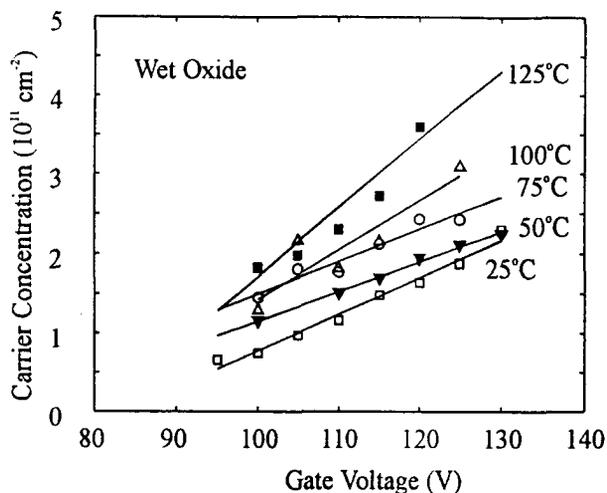


Fig. 1: Carrier concentration vs. gate voltage in inversion-mode MOSFETs in the wet oxide sample at high temperatures.

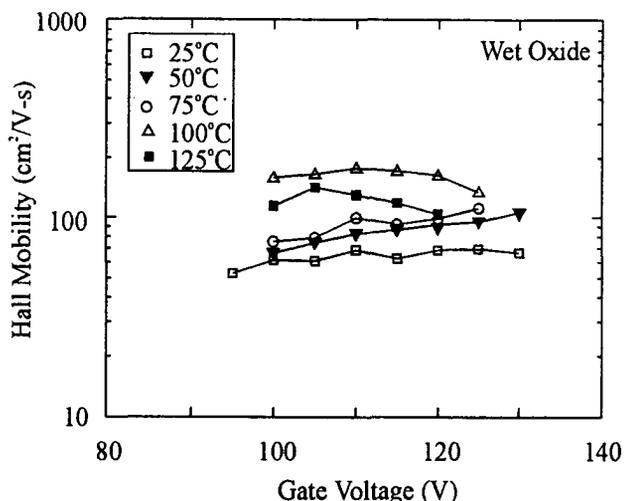


Fig. 2: Hall mobility in inversion-mode MOSFETs in the wet oxide sample at high temperatures.

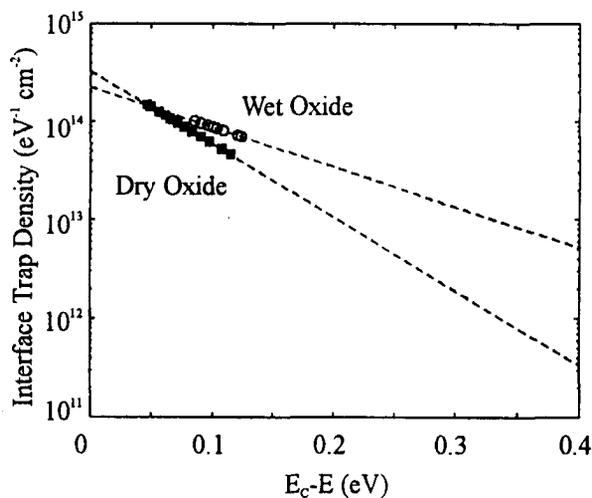


Fig. 3: Comparison of interface trap density in inversion-mode MOSFETs in wet and dry oxide samples.

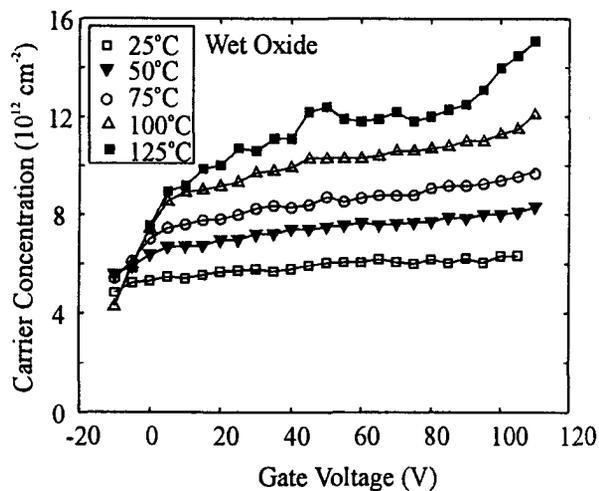


Fig. 4: Carrier concentration vs. gate voltage in accumulation-mode MOSFETs in the wet oxide sample

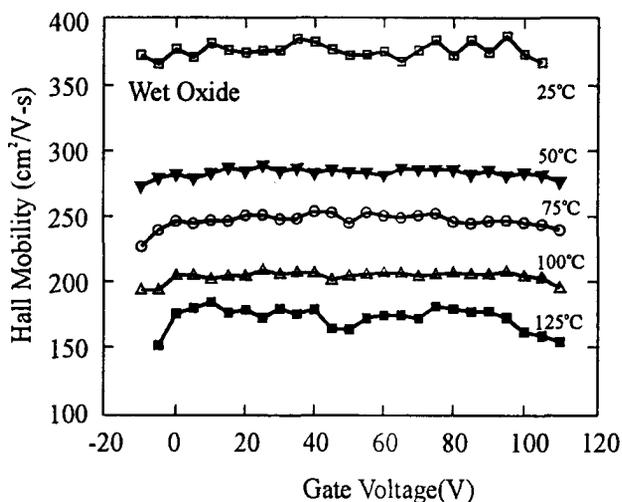


Fig. 5: Temperature dependence of Hall mobility in accumulation-mode MOSFETs in wet oxide sample.

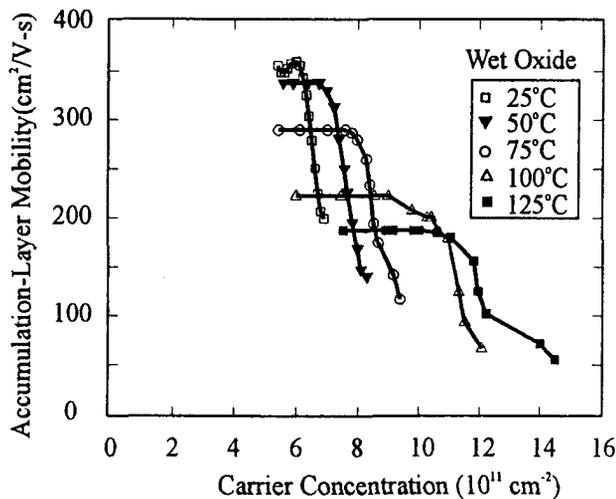


Fig. 6: Accumulation-layer electron mobility in the wet oxide sample for different temperatures.

Quantitative high resolution two dimensional profiling on SiC by scanning capacitance microscopy

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Scanning Capacitance Microscopy (SCM) is one of the most interesting two-dimensional (2D) carrier profiling techniques in Silicon, and recently some attempts have been made to apply SCM to SiC. On the contrary, very little attempts have been done in order to quantify SCM doping profiles measured on SiC. We successfully performed reproducible measurements and quantification of the SCM profiles.

N⁺ and Al⁺ were implanted in the energy range 20 - 200 keV both in p- and n-type 6H-SiC substrates. The implants were performed at a temperature of 500 - 800 °C. The samples were annealed at a temperature higher than 1300 °C in Si supersaturated ambient. Secondary Ions Mass Spectroscopy (SIMS) has been performed to obtain the chemical profiles.

SCM measurements were performed on cross-sectioned n- and p-type 6H-SiC implanted and annealed samples, but a quantification of the SCM profile was carried out for unipolar samples, only since the direct inversion technique delivers reliable results when there is no junction. A DC bias of 1 Volt and an AC bias of 1 Volt peak to peak were applied to the sample to perform the SCM measurement. In fig.1 we report the SCM profiles measured on the n-type sample implanted with two doses of 1×10^{14} and 5×10^{14} cm⁻², respectively. The ion implanted region in the high resistivity 4 μm epitaxial layer and the underlying low resistivity substrate can be clearly identified. The two well defined (and known) concentration levels represents the ideal case for the quantification of SCM.

Reproducible measurements, being crucial for quantification, have been obtained by developing an appropriate sample preparation that will be described in details.

The direct inversion technique, we applied in order to perform the conversion of the SCM profiles to carrier concentration profiles is based on an extended database of capacitance-to-voltage curves obtained by solving the Poisson equation for the metal-insulator-semiconductor system. The metallic tip is described as a parabolic shaped gate contact terminating with a hemisphere of radius r. The tip is surrounded by air (modelled by a dielectric material with relative dielectric constant $K_{\text{air}}=1$). The thin oxide grown by low temperature oxidation is modelled by a uniform silicon dioxide layer ($K_{\text{oxide}}=3.9$) with thickness t_{ox} . The fixed charge density and the interface state density is assumed to be zero. The work function difference between metal and semiconductor is also taken into account. An uniform n-type dopant concentration N_d is assumed in the 6H-SiC substrate and another metallic contact is put on the back side. A voltage V is applied to the tip gate contact, while the back contact is assumed to be grounded. Because of the cylindrical symmetry of the system with respect the tip axis, the problem is basically 2-dimensional (2D). The 2D Poisson equation has been solved by the finite element method, by providing the charge distribution in the semiconductor and the induced charge on the tip for a given bias V. The differential capacitance $C=dQ/dV$ is calculated by variation of the applied AC bias from 5 Volts to -5 Volts, yielding the C-V curve of a MOS capacitor, which ranges from the accumulation to depletion regime. The database produced, according to this scheme, includes 600 C-V curves (see Fig. 2). The calibration curve plotted in fig. 3 has been calculated for an applied DC bias of 1 Volt. It represents the calculated capacitance variation

dC (10^{-18} Farad) produced in the MOS system by a voltage variation $dV=1$ Volt (peak-to-peak) for different uniform concentration levels.

In fig. 4a and in fig. 4b we report the converted SCM profiles and the corresponding SIMS profiles for n-type 6H-SiC samples implanted at 500 °C with 200 keV N^+ ions respectively with doses $1 \times 10^{14} \text{ cm}^{-2}$ and $5 \times 10^{14} \text{ cm}^{-2}$ and then annealed at 1300 °C for 1 hour. The electrically active fractions estimated from converted SCM profiles are in good

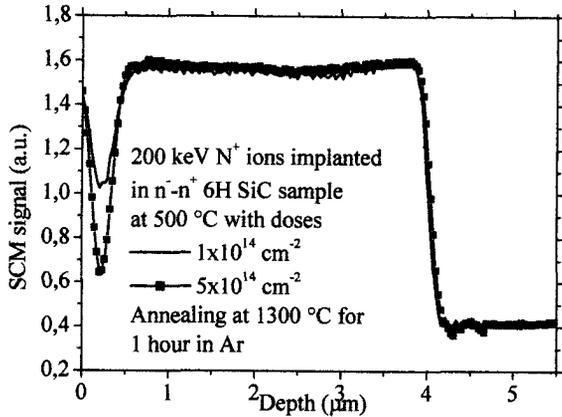


Fig. 1 - SCM signal vs depth for samples implanted with 200 keV N^+ at two different fluences

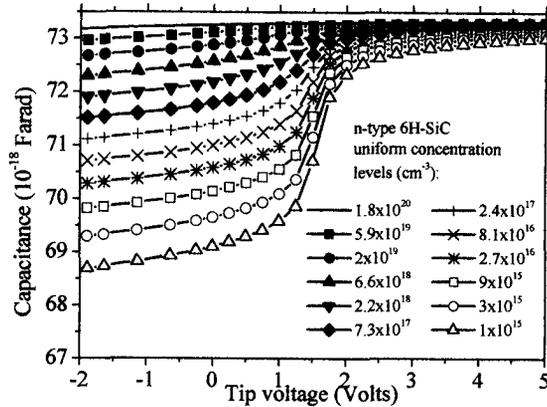


Fig. 2 - Calculated capacitance versus tip voltage for different concentration .

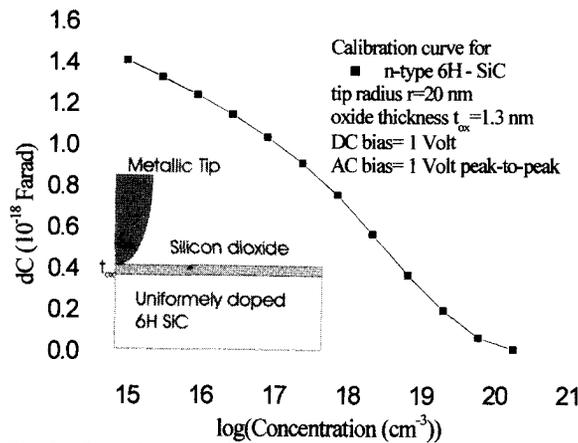


Fig. 3 - Capacitance variation dC versus concentration in the reported conditions. In the inset the MOS system is shown.

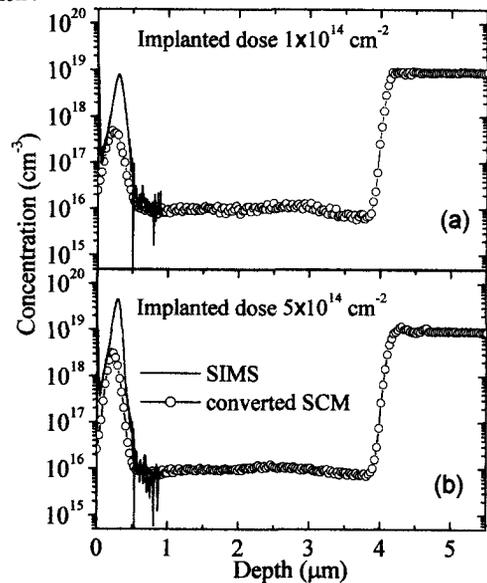


Fig.4 - Concentration profiles obtained by SCM and SIMS measurements for the two implanted samples.

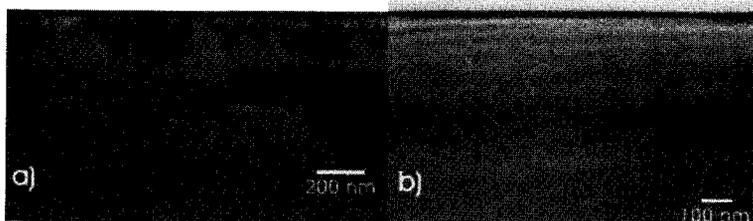


Fig. 5 - TEM analyses of samples implanted with N a) and Al b) and annealed at 1300 °C.

agreement with those obtained by Hall measurements (10%). A quite lower activation has been obtained for Al^+ implanted samples. Transmission electron microscopy allowed to image the defects present in the implanted and annealed samples. Loop dislocations were observed in the N^+ implanted sample while precipitates were present in the Al^+ implanted samples (see Fig. 5). A correlation with the electrically active profile has been done.

Scanning Capacitance Microscopy of SiC Multiple pn Junction Structure Grown by Cold-wall Chemical Vapor Deposition

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Silicon carbide is the most promising material for ultra-low-loss power switching devices because of its high breakdown field. Sophisticated (or complicated) device structures are required to accomplish a full potential of SiC in device performance. To fabricate such structures, device processes such as local impurity doping are extensively studied. It is also important to establish characterization techniques to evaluate such structures. Capacitance-voltage (*C-V*) measurement and secondary ion mass spectrometry (SIMS) are widely used for such a purpose. But these techniques are basically for one-dimensional (1-D) profiling. 2-D or 3-D analyses are needed for real device structures.

Scanning capacitance microscopy (SCM) is recently developed as one of scanning probe microscopy (SPM) techniques. This technique has realized a great success in 2-D doping profiling in Si VLSI-device technology. There are, however, only a few reports on SCM of SiC [1,2]. In this study, we demonstrate SCM of SiC multiple pn junction structure. The SCM result is discussed with SIMS analysis and a scanning electron microscope (SEM).

A sample used in this study was grown by atmospheric-pressure chemical vapor deposition (APCVD). A cold-wall type reactor was used, which is suitable for abrupt changing of doping gas (less memory effect compared to hot-wall CVD). Nitrogen (N_2) and diborane (B_2H_6) were used for n-type and p-type doping gases, respectively. The substrate was off-axis n-type 4H-SiC (0001). SCM was carried out with Digital Instruments D-3100 SPM system with a CoCr-coated conductive probe. The sample for SCM was prepared by a simple cleavage method.

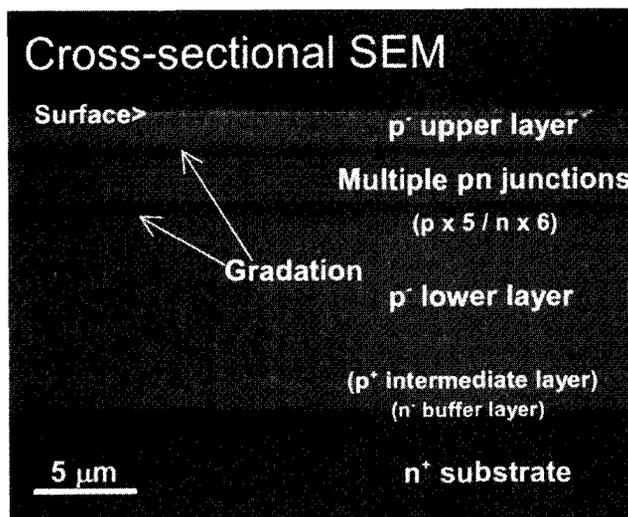


Figure 1: Cross-sectional SEM image for 4H-SiC multiple pn junction structure.

SIMS analysis revealed that uniform and abrupt multiple pn junctions are successfully fabricated. The concentration of both N and B atoms for 0.25 μm -thick n- and p-layers in multiple pn junctions is $1.5 \times 10^{17} \text{ cm}^{-3}$.

Figure 1 shows a cross-sectional SEM image obtained with an acceleration voltage of 5 kV. A SEM is useful to determine pn junction structure. Because the efficiency of secondary electron collection depends on the potential of each portion, an SEM image reflects the potential distribution. Since an n-type region is positively charged, the collection efficiency is smaller than that of p-type region. Therefore, an n-type region appears as a dark contrast in a SEM image. Five bright stripes correspond to p-layers in multiple pn junctions. The widths of stripes are very uniform, consistent with a SIMS analysis. Six dark stripes correspond to n-layers. The gradation observed at the both sides of multiple junctions originates from the depletion layer between n-layer and p⁻ upper/lower layers. From the depletion layer widths, the doping concentrations of p⁻ upper and lower layers can be calculated to be $2 \times 10^{15} \text{ cm}^{-3}$, $7 \times 10^{14} \text{ cm}^{-3}$, respectively, which agrees with the doping levels expected from the CVD growth condition.

AFM (topology) and SCM (capacitance) images are shown in Fig. 2. Since there is no special feature in AFM images, the SCM image originates from local electrical properties. A positive dC/dV signal corresponds to p-type, and a larger |dC/dV| signal means lower doping concentration. The polarity of observed SCM signal (Fig. 3) agrees with the SEM observation. For n-layers, the signal intensity is also consistent with the doping level of each layer. For p-layers, however, the p⁻ layer has a small dC/dV signal in spite of its light doping. Because the resistivity of B-doped layer with an acceptor concentration of $7 \times 10^{14} \text{ cm}^{-3}$ is, at least, $> 10^3 \Omega\text{-cm}$. The SCM measurement was affected by the high series resistance. Combination with a SEM as well as SIMS is very effective to understand the SCM signal. The bias voltage dependence of SCM signal will be also discussed.

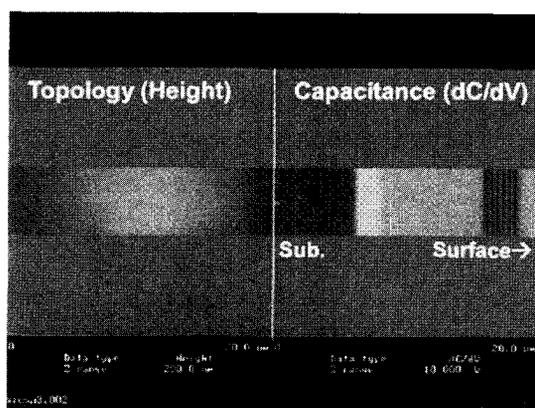


Fig. 2: Cross-sectional AFM and SCM images.

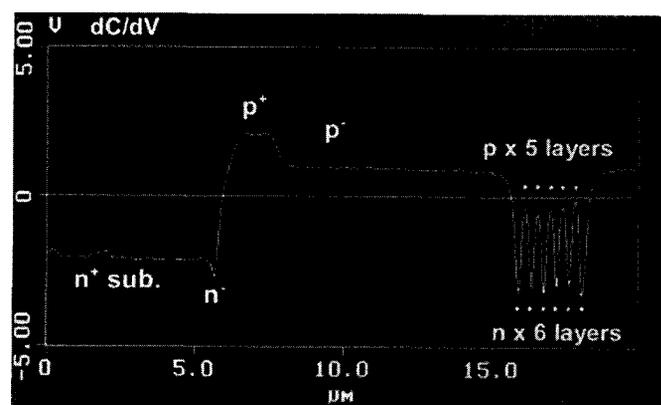


Figure 3: SCM signal along growth direction.

1. N. Nordell, S. Karlsson, and A. O. Konstantinov, *Mat. Sci. Forum* **264-268** 131 (1998).
2. A. Schöner, S. Karlsson and T. Schmitt *et al.*, *Mat. Scie. Symp. Proc.* **512** 469 (1998).