

MOS-Interface

Oxidation of Silicon Carbide: Problems and (Invited) Solutions

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High Current, NO Annealed Lateral 4H-SiC MOSFETs

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N 2 O Processing Improves the 4H-SiC Interface

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Significant Improvement of Inversion Channel Mobility in 4H-SiC MOSFET on (11-20) Face using Hydrogen Post Oxidation Annealing

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SiC-based MOS Structure with an SiO₂ Layer Formed at ,200°C by Use of Perchloric Acid

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Oxidation of Silicon Carbide: Problems and Solutions

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Among compound semiconductors the unique property of silicon carbide (SiC) to form a wide-bandgap native oxide attracted great interest for development of SiC-based metal-oxide-semiconductor (MOS) electronic devices. The core process in MOS-technology— thermal oxide growth— when applied to SiC was demonstrated to yield silicon dioxide (SiO₂) layers of comparable insulating quality as in the case of silicon, where it has secured the continuing triumph of Si MOS electronics. However, in the case of SiC, the development of practical MOS devices is still hampered by the much inferior electrical quality of the SiC/oxide interfaces than the Si/SiO₂ ones, mostly in terms of interface defect density. Moreover, additional problems arise because SiC MOS devices are intended to extend the range of application of solid-state electronics to high temperatures and electric fields. As the result, the SiO₂ gate insulator faces exposure to an environment it never had to tolerate before, and hence, reliability issues become important even for relatively thick gate oxides. Therefore, the future progress of SiC MOS applications will significantly depend on the basic understanding of these problems, which can pave the way to their solution.

The goal of the present review is to combine the available experimental and theoretical results, both regarding SiC/SiO₂ and Si/SiO₂, with the view to address the current understanding of physical and chemical nature of the SiC/SiO₂ interface imperfections and the oxide degradation. On the basis of this understanding, possible approaches to improvement of the SiC/insulator properties will be discussed.

The first major problem concerns the SiC/SiO₂ interface states: While the oxide itself exhibits densities of electron and hole traps comparable to the densities encountered in the oxides grown on silicon, the typically reported densities of the SiC/oxide interface defects are by orders of magnitude larger than at Si/SiO₂ interfaces. The latter is largely related to the fact that a considerable number of SiC/SiO₂ interface states appear stable against inactivation (passivation) by hydrogen. Though typical for the (111)Si/SiO₂ interface (isomorphic to Si-faces of hexagonal SiC), Si-dangling-bond type defects are also present at the SiC/SiO₂ interface, they, however, can be easily passivated by H, and so, do not represent an immediate danger. The possible origin of the states stable against interaction with H has been discussed for years, and currently, two suggestions have received substantial experimental support: clustering of excess carbon at the SiC/SiO₂ interface, and the presence in the near-interfacial oxide layer of defects with energy levels within the SiC bandgap. To battle these imperfections several approaches have been used recently, like SiC surface engineering, low-temperature post-oxidation, oxide nitridation, etc. There is, however, a general trend suggesting that the

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processes determining the elimination of the defects in the upper and lower parts of the SiC bandgap are not always correlated. This might be related to the different origin of the donor-type states dominant in the lower half of SiC bandgap and the acceptor-type states near the conduction band edge. So, it is possible that there exists no single technological solution which would enable simultaneous elimination of these defects. Interestingly, it will be shown that the growth of ultra-thin (< 5 nm) oxides might be of advantage because it allows one to reduce the total amount of excess carbon by minimizing the consumed SiC volume. At the same time, thin oxides can easily be nitrided, which was shown before to reduce the oxide defect density.

As regards the second problem, the basic features of electrical degradation and breakdown of SiO₂ have been studied in detail in Si MOS devices. The degradation appears to be determined by injection of electrons and holes into the oxide accompanied by the release of atomic hydrogen, acting as catalyst in bond-rupture processes. In the case of SiC, the injection-induced degradation may be considerably accelerated because the lifetime of a "hot" charge carrier increases in a wide bandgap semiconductor as compared to Si, leading to an enhanced carrier injection probability. Moreover, the high strength of electric field expected to be present in the gate oxide (particularly near p-n junction regions) may cause further "heating" of the electrons injected into SiO₂ ultimately leading to its breakdown. To counter these injection-induced effects one might consider reduction of the electric field strength in the oxide by employing a gate insulator with higher dielectric constant than that of SiO₂ ($\epsilon = 3.9$). Such insulators are currently under intense investigation for deep-submicron Si MOS technology, and several materials like Al₂O₃ ($\epsilon \approx 7-8$), ZrO₂ ($\epsilon \approx 15-20$), and HfO₂ ($\epsilon \approx 20-25$) were shown to be compatible with standard MOS processing. The major constraint in the application of these materials to SiC consists in their relatively narrow bandgaps (5-6 eV wide) which would result in low valence band offsets and, consequently, in high leakage current. Nevertheless, the experience gained on Si substrates indicates that this problem may be successfully overcome by applying a stack of ultra-thin SiO₂ and high permittivity oxide because the latter can be deposited in amorphous phase at temperatures as low as 300-350 °C.

A more complex reliability issue concerns the degradation of the SiC/oxide interfaces observed upon electrical biasing at elevated temperatures. This phenomenon, known in Si MOS structures as the bias-temperature instability, is basically related to the formation of protonic species in the near-interfacial SiO₂ (by trapping holes from the semiconductor) and their subsequent interaction with the semiconductor surface. Moreover, even without application of an electric field, proton-like species can be created by interface ionization of hydrogen observed both for Si and SiC at temperatures above 500 °C. As hydrogen passivation of defects necessary to fabricate an operational MOS device, its uncontrolled release afterwards cannot be excluded, particularly under conditions of current flow. The obvious (but only partial) solution consists in reduction of electric field at the SiC/oxide interface in devices intended for operation at elevated temperature. However, for the surface-channel MOS devices, the H-related degradation may appear the factor that will limit the temperature range of SiO₂ application as a gate insulating material.

High Current, NO Annealed Lateral 4H-SiC MOSFETs

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Recent advances in 4H-SiC MOS technology has rejuvenated interest in developing this structure for power MOSFET applications. The incorporation of post oxidation annealing in pure nitric oxide (NO) ambient at elevated temperatures has shown dramatic reductions in interface state density and significantly improved performance on test MOSFET devices[1]. However, before this breakthrough can be applied to real power MOSFET devices, we must understand how the NO annealed MOS interface is affected by process and design constraints relevant to power device fabrication. In this paper we show that the benefits of the NO anneal are not lost in the presence of an implanted p-well and the high temperature anneal necessary to activate the p-type implants. For the first time, we present Hall Effect measurements that further verify the improved mobility of electrons in the inversion layer due to NO. And, thanks to the uniformity and isotropy of the NO passivation, we are able to scale-up to large area (1 mm x 2 mm) devices delivering 2 A of on-state current at a 2.05 V forward drop!

4H-SiC n-channel MOS devices were fabricated on a 3 μm epilayer doped in the high 10^{15} cm^{-3} . Half of the wafer was aluminum implanted in order to simulate the effects of forming the MOS channel on a p-well. Nitrogen was implanted to form the source/drain regions. The implants were activated with a 5 min 1600°C argon anneal. A control sample was oxidized using the standard 1200°C dry + 950°C wet recipe [2]. A second sample was oxidized at 1150°C wet for 2.5 hr and then annealed in NO at 1175°C for 2 hr. Molybdenum and nickel were used for the gate and contact metallizations respectively. Figure 1 shows a collection of field effect mobility from 100 μm x 100 μm MOSFETs on these two wafers. Note that the NO annealed devices show higher mobility which is independent of location and channel orientation—necessary criteria for successfully scaling to large area devices. A particular concern for DMOS structures is the MOSFET mobility on implanted p-wells where mobility has been shown to degrade by at least an order of magnitude. The NO annealed MOSFETs remarkably exhibit very minimal mobility reduction on implanted p-wells—a very encouraging result for the DMOSFET.

Extracting true carrier transport properties can be difficult with MOSFET-based techniques due to the large amount of trapping that occurs at the MOS interface. However, the Hall Effect measurement does not suffer from such drawbacks[3]. Figure 2 shows the result of Hall measurements on a Van der Pauw MOS Hall bar for both NO annealed and unannealed samples. Consistent with the drift result, the NO sample shows a higher channel mobility surpassing 60 cm^2/Vs . Hall data can also be analyzed to extract interface trap density near the conduction band (Fig. 3) on p-type MOSFET-like structures instead of n-type MOS-capacitors[4]. A small but significant reduction in interface trap density is observed in the NO-annealed sample.

To test the scalability of the NO anneal technology, we fabricate interdigitated 1 mm x 2 mm lateral MOSFETs. These devices have 20 μm wide source/drain fingers separated by 3 μm channels resulting in a cell pitch of 23 μm . The forward characteristics of such a device are given in Fig. 4. The aforementioned high current level (2 A) is obtained by applying 20 V on the gate (16 V above threshold resulting in 3.5 MV/cm stress on the gate oxide) and 2.05 V of

forward bias. This results in a specific on-resistance of $10.3 \text{ m}\Omega\text{cm}^2$ which is the lowest reported value for any inversion-mode 4H-SiC MOS device. In conclusion, we have found the NO anneal to outperform the previous state-of-the-art MOS process in 4H-SiC, making this an ideal candidate for implementation in power MOSFET processing thereby ushering in a new era of SiC power MOS devices.

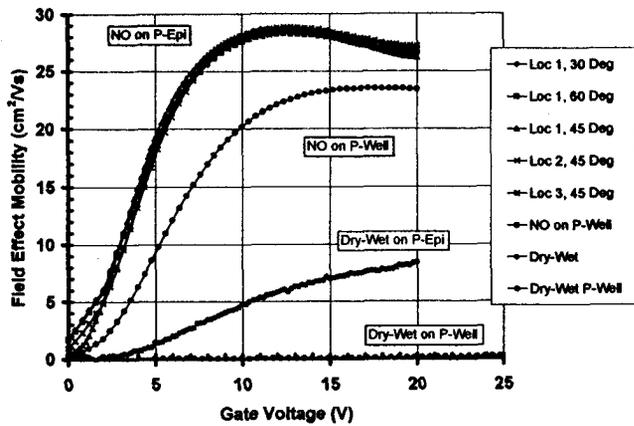


Figure 1. Collection of mobility data for NO annealed 4H-SiC FatFETs at various locations, channel orientation and channel makeup (epi or well). Dry-wet MOSFET data is also plotted.

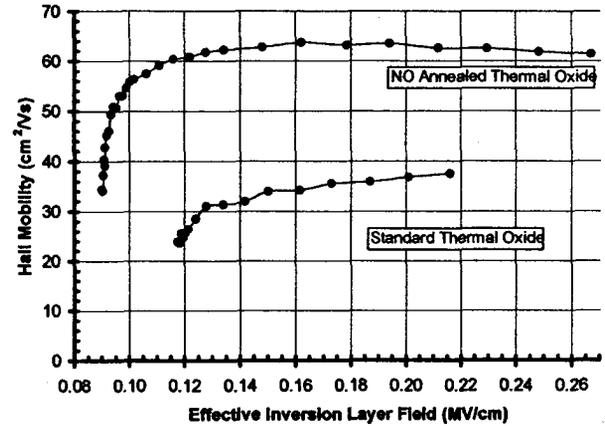


Figure 2. Improved Hall mobility of electrons in the 4H-SiC inversion layer due to a post oxidation NO anneal. Both MOS Hall bars are fabricated on unimplanted epilayers.

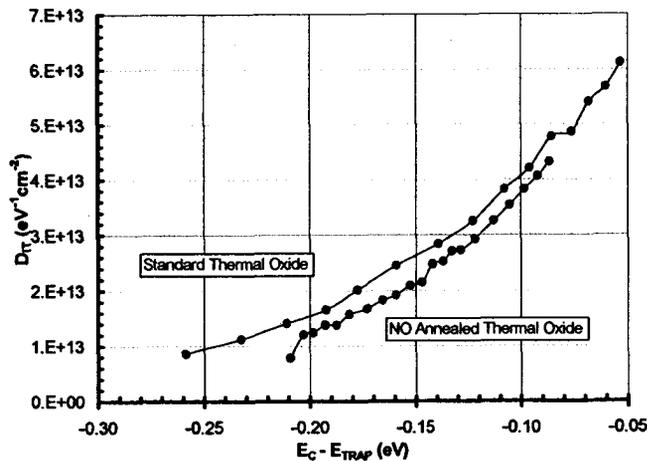


Figure 3. Reduced Hall interface state density near E_C in 4H-SiC due to a post oxidation NO anneal.

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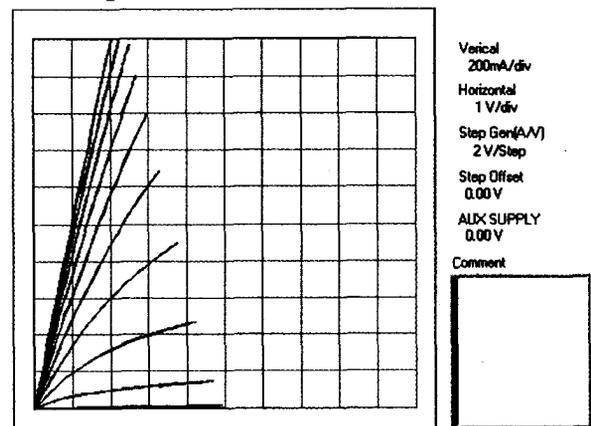


Figure 4. Forward characteristics of a 4H-SiC NO annealed $1 \text{ mm} \times 2 \text{ mm}$ lateral MOSFET.

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N₂O Processing Improves the 4H-SiC:SiO₂ Interface

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SiC Metal Oxide Semiconductor (MOS) devices are severely impacted by the large density of interface states present at the SiC:SiO₂ interface. Interface states near the conduction band-edge are particularly effective at inhibiting SiC device performance. Early improvements in oxidation processes reduced interface states only from the valence band to mid-gap.¹ More recent progress has been accomplished using an NO anneal^{2,3}, which lowers the interface state densities near the conduction band-edge. While these improvements using NO annealing are important, use of this gas in traditional furnaces is not desirable with the health risks associated with pure NO. Use of N₂O has been pursued and effectively developed as an alternative to NO.

As shown in Figure 1, the temperature of the N₂O processing is critical. At lower temperatures (1100°C), exposing an existing oxide to N₂O increases the interface state density, as shown by comparing the heavy solid line representing a thermal oxide to the data for the same thermal oxide exposed to an 1100°C N₂O anneal. At 1200°C, the thermal oxide is dramatically improved with the N₂O anneal. Thermal oxides processed in a wet ambient are more improved by the 1200°C N₂O anneal, as seen by comparing the solid circle to the open circle data.

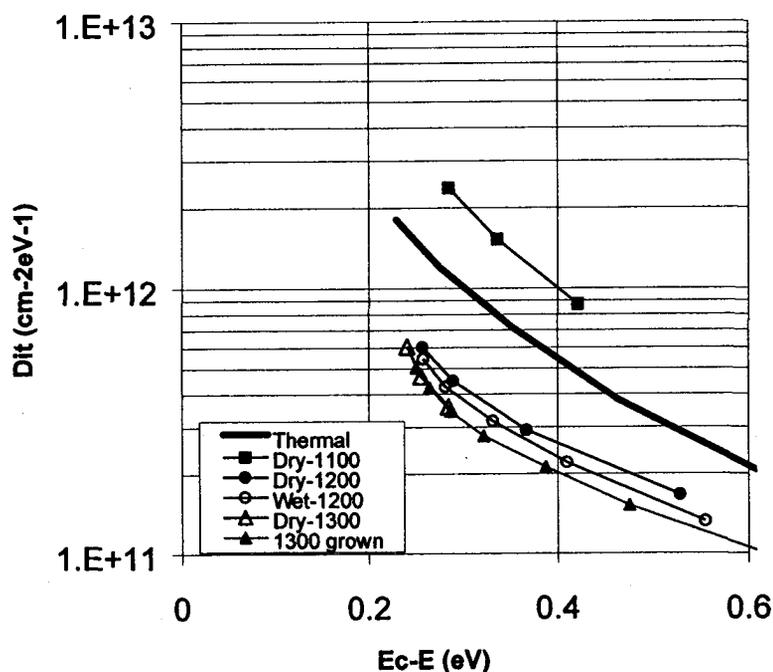


Figure 1. Interface State Density Near the Conduction Band-Edge for 4H-SiC. Samples with thermal oxides with different temperature N₂O anneals and one sample grown in N₂O are compared.

The best results are obtained using a 1300°C N₂O process. At this temperature, the oxidation of SiC is significant. So, in addition to annealing existing oxides in N₂O, some oxides were grown in the N₂O ambient (500 Å was grown in 3 hours). Growing the oxide in N₂O saves about 9 hours of processing time over annealing an existing oxide in N₂O, by eliminating the oxidation step. The same superior results are obtained regardless of whether the oxide is grown prior to N₂O processing or grown in N₂O.

MOSFETs processed with our earlier 1200°C N₂O annealed oxide had higher effective surface channel mobility than devices that did not receive the N₂O anneal, as shown in Figure 2. The interface state densities measured on nearby p-type capacitor structures and corresponding n-type capacitors are shown in Figure 3. The reduction in interface state density directly correlates with an improvement in effective surface channel mobility.

We will also have effective surface channel mobility data on 4H-SiC MOSFETs with oxides grown in N₂O at 1300°C to present at the conference.

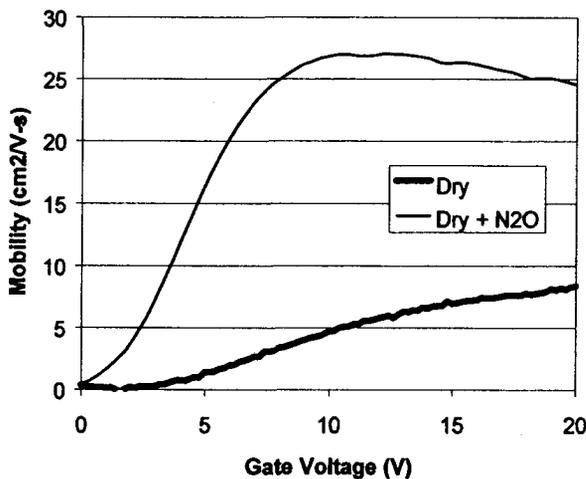


Figure 2. Effective Surface Channel Mobility for 4H-SiC planar MOSFETs, with and without N₂O processing.

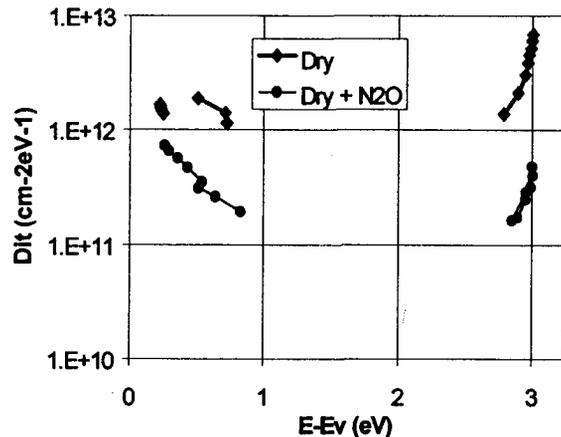


Figure 3. Interface States across the entire band-gap for the oxides of Figure 2.

Acknowledgements

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Significant Improvement of Inversion Channel Mobility in 4H-SiC MOSFET on (11 $\bar{2}$ 0) Face using Hydrogen Post Oxidation Annealing

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4H-Silicon carbide (SiC) metal-oxide-semiconductor field-effect-transistor (MOSFET) is expected as a promising candidate for a high-speed and low-loss switching power device. However, there have been few satisfactory results regarding the fabrication of 4H-SiC MOSFET with high inversion channel mobility. It has been pointed out that high interface trap density (D_{it}) at SiO₂/SiC interface lowers the inversion channel mobility, resulting in high on-resistance (R_{ON}) of 4H-SiC MOSFET. Yano et al. reported that the inversion channel mobility of around 30 cm²/Vs in 4H-SiC MOSFET was obtained utilizing (11 $\bar{2}$ 0) face instead of conventional (0001) Si face, but was not sufficient to reduce the R_{ON} . [1] We have reported that hydrogen post oxidation annealing (H₂ POA) reduce the D_{it} near the conduction-band edge of the n-type 4H-SiC MOS structures on (0001) Si face. [2] In this study, the significant improvement of the inversion channel mobility in 4H-SiC MOSFET fabricated on (11 $\bar{2}$ 0) face using H₂ POA is reported.

N-channel MOSFETs were fabricated on p-type epitaxial layers grown in our group on n-type 4H-SiC substrates with the (11 $\bar{2}$ 0) face orientation purchased from Nippon Steel Co. The thickness and the effective doping density of the epitaxial layers were 3.5 μm and 1x10¹⁵ cm⁻³, respectively. Source and drain regions were formed by phosphorus ion implantation at 500°C with the total dose of 7x10¹⁵ cm⁻². Post implantation annealing was performed at 1500°C for 5 min in Ar. Gate-oxides were thermally grown in water vapor atmosphere [wet oxidation, samples (a) and (b)] at 1150°C and were *in-situ* annealed in Ar at the oxidation temperature for 30 min, resulting in oxide thickness of 49 nm. In addition, the sample (b) was annealed in pure hydrogen at 800°C for 30min [H₂ POA]. Aluminum was evaporated as the gate and source/drain contact metals. The channel length (L) and width (W) were 100 and 150 μm, respectively. Electrical measurements were carried out at room temperature using a Hewlett-Packard Semiconductor Parameter Analyzer 4156B. The drain

current was measured along [0001] direction.

Figure 1 shows typical drain current (I_D) – drain voltage (V_D) characteristics of 4H-SiC MOSFET with gate-oxide prepared by wet oxidation following H_2 POA fabricated on the $(11\bar{2}0)$ face [sample (b)] for different gate voltages (V_G) between 0 and 12 V. The I_D - V_D characteristics exhibit excellent linear and saturation regions. The results of a field-effect mobility (μ_{FE}) measurement for both the wet gate-oxide 4H-SiC MOSFETs with and without H_2 POA are shown in Fig. 2. The μ_{FE} was calculated from I_D - V_G characteristics at $V_D=0.1$ V. The peak μ_{FE} of the sample (a) is almost the same value with that reported by Yano et al.[1] The gate-oxide preparation process including the H_2 POA drastically enhances the μ_{FE} and results in the peak μ_{FE} of $110\text{ cm}^2/\text{Vs}$ in the samples (b). The values of a subthreshold voltage swing for the samples (a) and (b) are 204 and 85 mV/decade, respectively. This result suggests the H_2 POA reduces the D_{it} . To our knowledge, the inversion channel mobility of $110\text{ cm}^2/\text{Vs}$ is the highest for lateral n-channel 4H-SiC MOSFETs with a thermal gate-oxide reported until now.

This work was performed under the management of FED as a part of the METI NSS program (R&D of Ultra-Low-Loss Power Device Technologies) supported by NEDO.

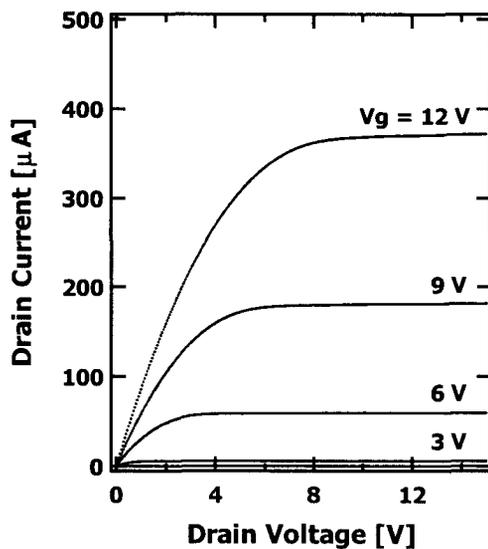


Fig. 1. I_D - V_D characteristics of 4H-SiC MOSFET with gate-oxide prepared by wet oxidation following H_2 POA fabricated on the $(11\bar{2}0)$ face.

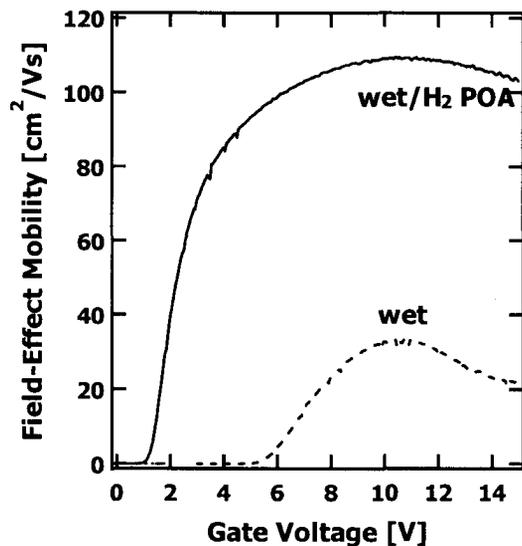


Fig. 2. μ_{FE} - V_G characteristics of wet gate-oxide 4H-SiC MOSFET with and without H_2 POA fabricated on the $(11\bar{2}0)$ face.

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SiC-based MOS structure with an SiO₂ layer formed at ~200 °C by use of perchloric acid

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1. Introduction

SiC is a wide-gap semiconductor that is less reactive than Si, and thus thermal oxidation of SiC requires high temperatures above 1050°C [1-4]. Such high temperature heat treatments degrade interfacial properties, e.g., high interface state density more than 10^{11} cm⁻²eV⁻¹ [3,4]. We have recently found that the Si oxidation proceeds at ~200 °C by use of perchloric acid [5,6] and the resulted silicon dioxide (SiO₂) layers possess a low interface state density of 1.5×10^{10} cm⁻²eV⁻¹ even without hydrogen treatment [6]. In the present study, this noble method is employed in the formation of SiC-based MOS structure. We have found that the concentration of graphitic carbon at the interface is very low in cases where post-oxidation heat treatment is performed at 950 °C, resulting in the low interface state density of 1×10^{11} cm⁻²eV⁻¹.

2. Experiments

MOS structure was fabricated using a nitrogen-doped n-type SiC epitaxial layer of ~10 μm thickness with the donor density of 6×10^{15} cm⁻³ formed on a 6H-SiC(0001) wafer. An SiO₂ layer was formed by the immersion of the wafer in concentrated perchloric acid (HClO₄) at the boiling temperature of 203 °C. Post-oxidation heat treatments were performed at temperatures ranging between 950 and 1150 °C in nitrogen. Then, aluminum (Al) dots of 0.15 mm diameter were formed on the surface, resulting in <Al/SiO₂/6H-SiC(0001)> MOS structure.

3. Results and discussion

Figure 1 shows the plot of the thickness of the SiO₂ layer vs. the immersion time in HClO₄ at 203 °C. It is seen that thick SiO₂ layers of ~80 nm thickness can be formed in spite of the low oxidation temperature. The plot is almost linear, indicating that the oxidation is reaction-limited [7], in contrast to diffusion-limited conventional thermal oxidation [8]. This result shows that diffusion of the oxidizing species (i.e., O⁻ ions formed by the decomposition of ClO₄⁻ ions [5,6]) through the growing SiO₂ layer proceeds

smoothly. The inward migration of O⁻ ions is likely to be promoted by the electrical field induced in the SiO₂ layer by ClO₄⁻ ions at the surface [6]. The reaction at the interface proceeds at the low temperature because of the high reactivity of O⁻ ions.

We have found that the leakage current density of the <Al/SiO₂/6H-SiC(0001)> MOS diodes was high without post-oxidation heat treatment due to the presence of Cl⁻ and ClO₄⁻ ions in the SiO₂ layer, while with post-oxidation heat treatment above 900 °C in nitrogen, it became sufficiently low, i.e., less than 10^{-8} Acm⁻² at the gate bias of 5 V.

Figure 2 shows the capacitance-voltage (C-V) curves of the <Al/SiO₂/6H-SiC(0001)> MOS diodes. When the post-oxidation heat treatment was performed at 1100 °C (curve a), the high-frequency (solid line) and quasi-static (dotted line) C-V curves deviated from each other, due to the presence of high density interface states. From these curves, the interface state density at 0.5 eV below the conduction band minimum is estimated to be 3×10^{11} cm⁻²eV⁻¹. When the post-oxidation heat treatment temperature was lowered to 950 °C, the deviation between the high-frequency and quasi-static C-V curves became much smaller (curve b). In this

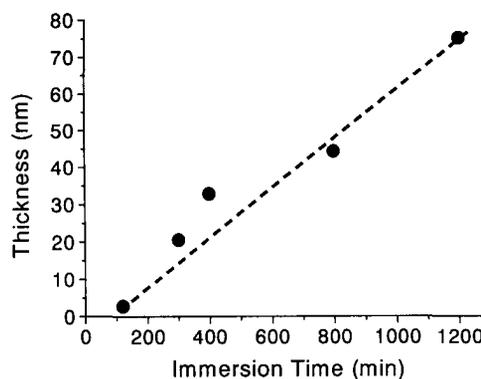


Fig. 1 Thickness of the SiO₂ layers vs. the time of immersion of SiC in HClO₄ at 203 °C.

case, the interface state density at 0.5 eV was estimated to be $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

Figure 3 shows the XPS spectra for the $\text{SiO}_2/\text{6H-SiC}(0001)$ interface. For XPS measurements, thick SiO_2 layers were formed by the immersion in HClO_4 , followed by etching of the layers with a 1 % HF solution. The etching was stopped when the substrate Si 2p peak as well as the oxide peak was observed with considerable intensities (SiO_2 thickness: 2.5 nm). After post-oxidation heat treatment at 1150 °C, a C 1s peak due to graphitic carbon was observed in the higher energy side of the SiC substrate peak (spectrum a), and its amount is estimated to be 1.3 monolayer. The intensity of the C 1s peak due to graphitic carbon was markedly reduced by lowering the post-oxidation temperature to 950 °C (spectrum b), and in this case its concentration is estimated to be 0.6 monolayer. It should be noted that for the thick SiO_2 layers formed with HClO_4 , no C 1s peak due to graphitic carbon was observed, indicating that carbon was not present in the bulk of the SiO_2 layer.

Comparison of Figs. 2 and 3 leads to the conclusion that the interface states are mainly due to graphitic carbon. In the case of thermal oxidation at high temperatures, loss of Si occurs, resulting in the formation of graphitic carbon at the interface [9]. For the oxidation by HClO_4 , the formation of graphitic carbon does not occur because of the low temperature oxidation in addition to the high reactivity of HClO_4 with carbon. However, the SiO_2 layers include Cl^- and ClO_4^- ions with the total concentration of 0.2 atomic%, and these species act as trap states, resulting in the high leakage current density. For the removal of the Cl-species, post-oxidation heat treatment is necessary. In this case, however, post-oxidation heat treatment should be performed

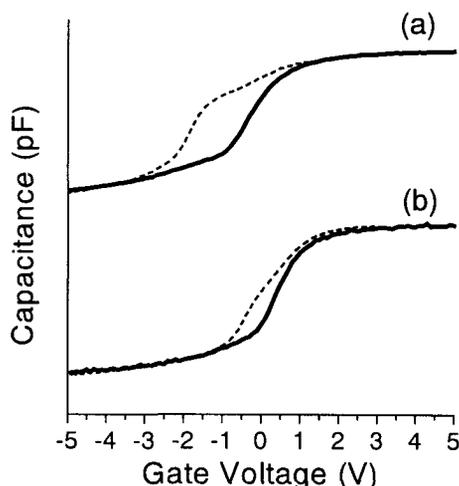


Fig. 2 C-V curves for the $\langle \text{Al}/\text{SiO}_2/\text{6H-SiC}(0001) \rangle$ MOS diodes having an SiO_2 layer formed in HClO_4 at 203 °C with post-oxidation heat treatment at the following temperatures: a) 1100 °C. b) 950 °C.

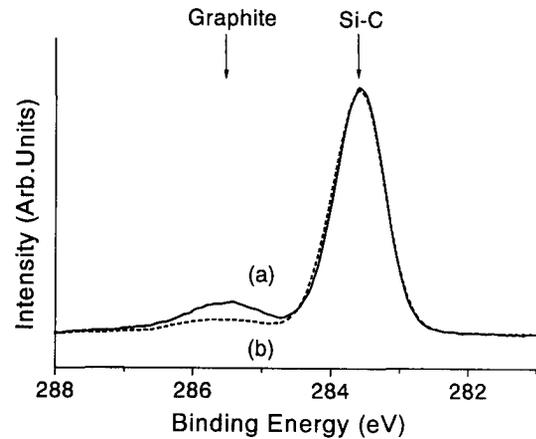


Fig. 3 XPS spectra in the C 1s region for the SiO_2/SiC interfaces with post-oxidation heat treatment at the following temperatures: a) 1150 °C, b) 950 °C.

at temperatures lower than 950 °C in order to prevent the formation of graphitic carbon at the interface.

4. Conclusions

We have developed a low temperature fabrication method of SiC-based MOS structure by use of HClO_4 . In spite of the oxidation at 203 °C, an SiO_2 layer sufficiently thick for the MOS application can be formed. When the post-oxidation heat treatment is performed at 950 °C, the concentration of the interfacial graphitic carbon is very low, resulting in the low interface state density of $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.5 eV below the conduction band minimum.

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