

## Special Symposium

### **Passivation of the 4H-SiC/SiO<sub>2</sub> Interface with Nitric (Invited) Oxide**

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### **Recent Achievements and Future Challenges in SiC (Invited) Homoepitaxial Growth**

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### **High Quality SiC Substrates for Semiconductor (Invited) Devices: from Research to Industrial Production**

S. G. Mueller, M. Brady, B. Brixius, G. Fechko, R. Glass, D. Henshall, D. Hobgood, J. Jenny, R. Leonard, D. Malta, A. Powell, V. F. Tsvetkov, C. H. Carter, Jr.

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### **Growth and Defect Reduction of Bulk SiC Crystals (Invited)**

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### Passivation of the 4H-SiC / SiO<sub>2</sub> Interface with Nitric Oxide

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Silicon carbide material properties such as high breakdown field strength ( $\times 10$  Si), high saturated electron drift velocity ( $\sim \times 2$  Si) and excellent thermal conductivity ( $\sim \times 2.5$  Si) make this wide band gap semiconductor a promising material for high power devices. Silicon carbide is also the only wide band gap semiconductor that has a native oxide. The same thermal techniques that are used to grow oxide layers on Si can be used to oxidize SiC – the one difference being that normal oxidation temperatures are higher for SiC by 200-300°C.

Bulk electron mobility is higher for 4H-SiC than for the 6H-polytype ( $\sim 900\text{cm}^2/\text{V-s}$  compared to about  $450\text{cm}^2/\text{V-s}$ ), and hence 4H-SiC is the polytype of choice for power MOSFET fabrication. However, the problems of surface roughness produced by ion implantation / activation prior to oxidation and a high interface state density near the conduction band edge following oxidation [1] have hindered the development of *n*-channel, inversion-mode 4H-SiC MOSFETs. Much attention has been focused on improving the performance of these devices – particularly with regard to the characterization and passivation of the interface states near the conduction band edge  $D_{it}(E_c)$  [2-4]. Efforts have included the use of deposited oxides [5], low dose ion implantation in the channel region [6] and oxide growth on the “a-face” of 4H-SiC [7]. Herein, we describe an interface state passivation process based on post-oxidation, high temperature anneals in nitric oxide [8]. This process reduces  $D_{it}(E_c)$  by an order of magnitude (Fig. 1) and increases the effective channel mobility for *n*-channel MOSFETs from single digits to  $\cong 30\text{cm}^2/\text{V-s}$  and higher, as shown in Figure 2 and as reported in other papers at this conference [10,11]. The temperature dependencies of the effective channel mobility and the threshold voltage are shown in Figures 3 and 4 for lateral 4H-MOSFETs passivated with nitric oxide. The results for channel mobility may be compared with results reported by others for unpassivated devices fabricated with standard 4H-SiC [12-13] and for devices fabricated with oxide layers that were grown on the 4H-SiC a-face [7]. Unpassivated, standard devices exhibit increasing field effect mobility with increasing temperature, while the low field mobility for a-face MOSFETs decreases with increasing temperature. In Figures 3 and 4, the observed trends for both devices (passivated and unpassivated) are consistent with the thermal liberation of electrons trapped near the conduction band edge. Mobility increases as the result of reduced Coulomb scattering, and  $V_{th}$  decreases because there is less negative charge at the oxide-semiconductor interface.

Details of the NO passivation process will be discussed. Other papers to be presented at this conference [10,11] show that the process is compatible with additional processing steps that are required for SiC MOSFET fabrication – e.g., *p*-well implantation and source / drain contact annealing. The NO passivation technique is the first process that significantly improves the channel mobility of devices fabricated using standard 4H-SiC. However, after passivation,  $D_{it}(E_c)$  remains approximately 100 times higher for SiC compared to Si. This is an indication that work must continue to further improve the 4H-SiC / SiO<sub>2</sub> interface.

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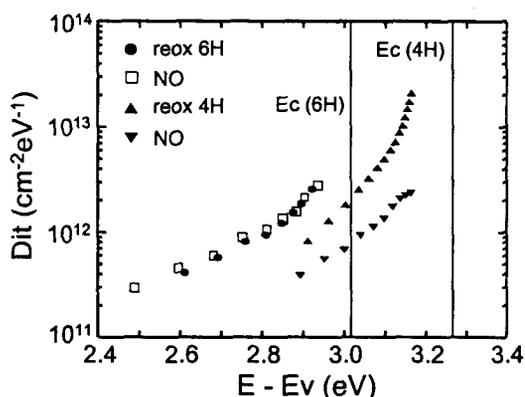


Fig. 1. Effect of NO passivation on  $n$ -4H-SiC.

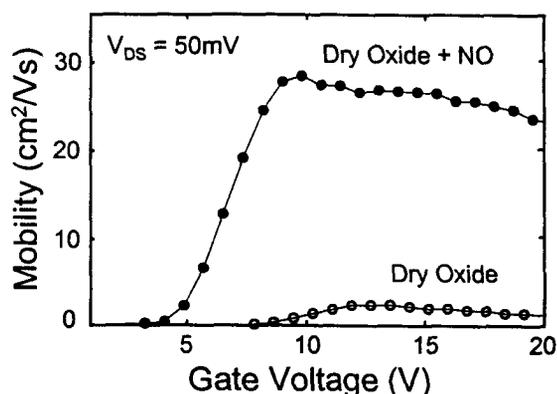


Fig. 2. Channel mobility for lateral 4H-SiC MOSFETs.

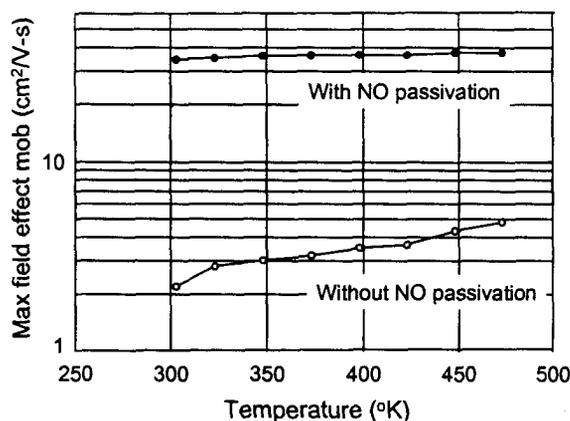


Fig. 3. Temperature dependence of the effective channel mobility for lateral 4H-SiC MOSFETs.

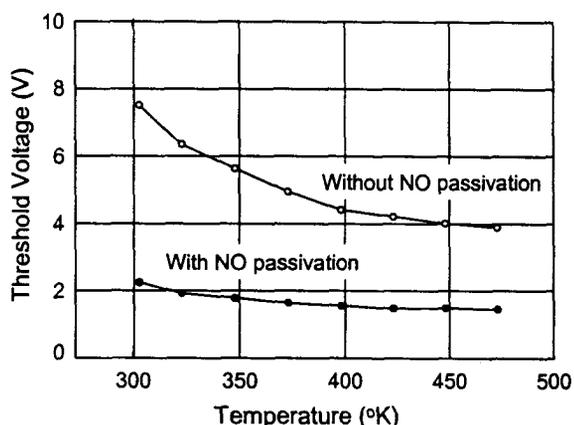


Fig. 4. 4H-SiC MOSFET threshold voltage as a function of temperature.

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## Recent Achievements and Future Challenges in SiC Homoepitaxial Growth

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### Introduction

SiC homoepitaxial growth has been a key technology to fabricate high-performance SiC device structures. Major requirements for SiC epitaxy include good morphology, high purity, low defect density, wide-range and abrupt doping control, thickness and doping uniformity, and high growth rate. Although SiC growth technology is becoming mature to fulfill most of these demands in a 2~3 inch wafer level, further improvements and understanding of growth itself such as doping and defect generation mechanisms are required. In this paper, the authors present three topics of SiC epitaxy: growth of high-purity SiC, fast epitaxy, and a proposal of a new crystal face. Remaining issues in SiC epitaxy are also discussed.

### Growth of high-purity SiC

High-purity and thick 4H-SiC(0001) epilayers have been grown by a horizontal hot-wall CVD system, which was designed and built at the authors' group. Typical flow rates of SiH<sub>4</sub>, C<sub>3</sub>H<sub>8</sub>, and H<sub>2</sub> were 1.5 sccm, 0.75 sccm, and 5~10 slm, respectively. Most growth runs were carried out at 1550 °C and at reduced pressure, by which a growth rate of 5 μm/h was obtained. Figure 1 shows the donor concentration of unintentionally doped epilayers vs. the reactor pressure during CVD. The donor concentration showed significant decrease by reducing the pressure. Preliminary experiments on intentional nitrogen doping have also indicated that the doping efficiency of nitrogen is suppressed at low pressure. A probable reason for this effect might be the enhanced desorption of nitrogen from a growing surface at reduced pressure, but more complicated surface kinetics should be involved. In the present system, the reproducible donor concentration is 1~3×10<sup>13</sup> cm<sup>-3</sup> in CVD at 80 Torr. Free exciton peaks dominated in low- and room-temperature photoluminescence spectra without Ti or point-defect related peaks. The electron mobility reaches 981 cm<sup>2</sup>/Vs at 290 K and 46,200 cm<sup>2</sup>/Vs at 42 K. The total trap concentration could be reduced to as low as 4.7×10<sup>11</sup> cm<sup>-3</sup> by increasing the input C/Si ratio.

### Fast epitaxy of high-quality SiC

Fast epitaxial growth of SiC has been realized by chimney-type vertical hot-wall CVD, also designed at the authors' group. High-temperature growth at 1700 °C enables higher precursor flow rates and thereby a higher growth rate, keeping a specular surface. Typical growth was performed at 100 Torr in a SiH<sub>4</sub>-C<sub>3</sub>H<sub>8</sub>-H<sub>2</sub> system. Figure 2 represents the C/Si ratio dependence of growth rate, donor concentration, and deep trap concentration of undoped 4H-SiC(0001) epilayers. The lowest background doping level is 1×10<sup>14</sup> cm<sup>-3</sup> (n-type) or less. By increasing the C/Si ratio, the trap concentration, the Z<sub>1</sub> center being dominant, was reduced to 5×10<sup>12</sup> cm<sup>-3</sup>, in spite of a high growth rate of 25 μm/h. The authors have fabricated high-voltage (> 3 kV) implanted pin diodes using these epilayers. We will present characterization of more than 100 μm-thick epilayers by various techniques [1].

### Epitaxial growth on new faces: 4H-SiC(11 $\bar{2}$ 0) and (03 $\bar{3}$ 8)

Micropipes and low MOS inversion channel mobility have been recognized as the most severe obstacles to realize high-current and low-loss SiC power MOSFETs. At ICSCRM'99, the authors presented successful homoepitaxy of 4H-SiC(11 $\bar{2}$ 0) and greatly improved performance

of 4H-SiC MOSFETs. In this conference, we propose a novel crystal face: 4H-SiC(03 $\bar{3}$ 8). 4H-SiC(03 $\bar{3}$ 8) is the face inclined by 54.74° toward <01 $\bar{1}$ 0> from (0001), and is semi-equivalent to 3C-SiC(001), as illustrated in Fig.3. 4H-SiC(03 $\bar{3}$ 8) wafers were prepared by slicing ingots grown at SiXON [2]. Homoepitaxial growth on this face has been carried out by both cold-wall and hot-wall CVD reactors. As in the 4H-SiC(11 $\bar{2}$ 0) growth, homoepitaxial layers with a very flat surface can be obtained on 4H-SiC(03 $\bar{3}$ 8) without intentional off angle, as shown in Fig.4. Formation of macrosteps and triangular defects has never been observed. The doping efficiency of nitrogen on this face is slightly higher than on (0001), but a low background doping concentration of  $3 \times 10^{14} \text{ cm}^{-3}$  (n-type) can be achieved. Successful homoepitaxy, the possible availability of micropipe-free wafers, and low interface state density in MOS structure [3] make this face an attractive alternative for high-power SiC devices.

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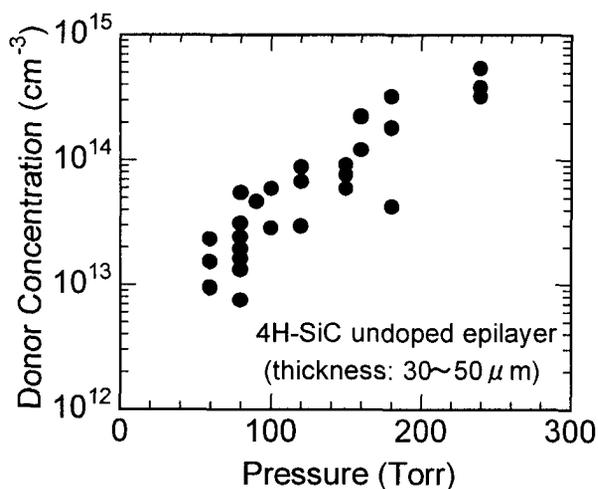


Fig.1 Pressure dependence of donor concentration for unintentionally doped 4H-SiC(0001) epilayers. (horizontal hot-wall CVD)

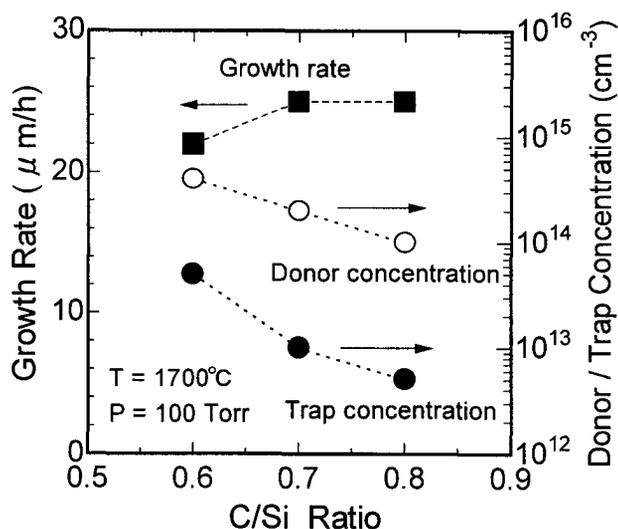


Fig.2 C/Si ratio dependence of growth rate, doping level, and trap concentration of 4H-SiC(0001) epilayers. (chimney-type vertical hot-wall CVD)

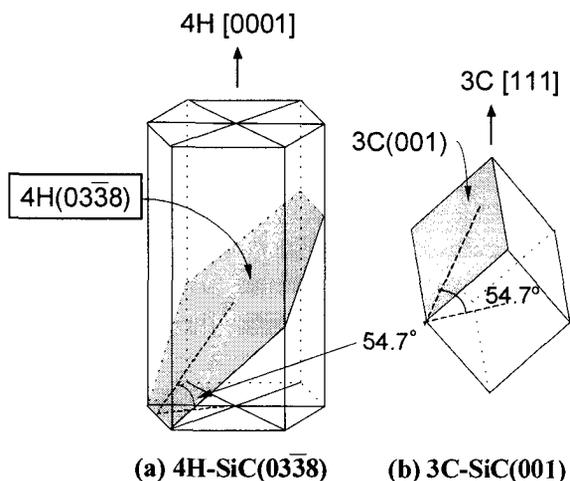


Fig.3 Illustration of 4H-SiC(03 $\bar{3}$ 8) and 3C-SiC(001).

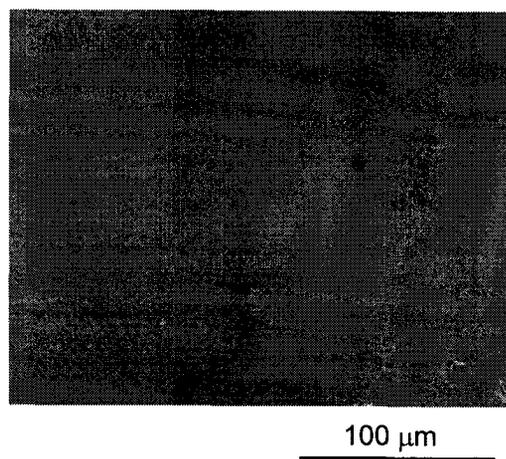


Fig.4 Typical surface morphology of a 4H-SiC(03 $\bar{3}$ 8) epilayer.

## **HIGH QUALITY SiC SUBSTRATES FOR SEMICONDUCTOR DEVICES: FROM RESEARCH TO INDUSTRIAL PRODUCTION**

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The production of large diameter, high quality SiC substrates is essential to realize the full potential of this important semiconductor material. Within the last several years SiC bulk sublimation growth has matured from a research state to a volume process for the production of these substrates. The current state of the art of SiC sublimation growth is reviewed from an industrial point of view. Specific efforts towards larger diameter high quality substrates have led to the production of 50 mm and 75 mm diameter 4H and 6H wafers, which are now commercially available and the demonstration of high quality 100 mm wafers. In SiC, micropipes remain the most critical defects for SiC device production. The unique properties of these defects are characterized by etching and x-ray white beam topography. Results at Cree have allowed us to steadily decrease the micropipe density both in our best R&D results and average production values over the past several years. The analysis of KOH-etched SiC wafers from low micropipe density boules has determined micropipe-free 4H-N material on a diameter of 25 mm, densities as low as  $0.9 \text{ cm}^{-2}$  for an entire 50 mm 4H-N wafer, and  $8 \text{ cm}^{-2}$  for a 6H-N 75 mm wafer. For further defect reduction in SiC substrates of increasing diameter, continued refinement of our understanding of the growth process is essential. We will summarize results of modeling the growth process, focussing on the thermoelastic stress in the growing crystal and the effect on dislocation formation. Recent R&D progress at Cree has resulted in the seeded sublimation growth of high purity 4H SiC bulk crystals of 50 mm and 75 mm diameter exhibiting semi-insulating behavior without resorting to the intentional introduction of deep level elemental dopants, such as vanadium. Additionally, these crystals exhibit micropipe densities in the range of  $10 - 150 \text{ cm}^{-2}$  on a 50 mm diameter. Based on high temperature Hall-effect measurements, the semi-insulating behavior is characterized by a range of activation energies from 0.9 to 1.6 eV. The absence of vanadium was confirmed by SIMS measurements, optical absorption, and EPR spectra of this new material. Correlation of EPR signatures with intrinsic deep level defects will be presented. We present thermal conductivity data for this new high resistivity material and compare it to values of materials of different doping levels. The corresponding doping and temperature dependencies and the relevance for device applications are discussed.

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## Growth and Defect Reduction of Bulk SiC Crystals

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Silicon carbide (SiC) is a wide band gap material with a well-recognized potential for high-power, high-temperature electronics. The fundamental material parameters of SiC are very attractive for the fabrication of semiconductor devices with superior characteristics for high current and high voltage devices. The unique physical properties of SiC include a large energy bandgap, high thermal conductivity and high breakdown electric field. Because of their fundamental material parameters, SiC devices have been predicted to have a higher breakdown voltage (at the same doping level) and to operate at a higher forward current density than Si devices. Recently, because of significant progress in SiC technology, these predictions have become a reality. However, the commercialization of SiC devices is still not fully achieved, and factors limiting the commercialization are largely related to the material quality of available SiC crystals.

In this paper, we discuss the bulk crystal growth of SiC single crystals by highlighting recent advances in crystal diameter enlargement and improvements in crystal quality.

Seeded sublimation growth, also known as physical vapor transport (PVT) growth, has been the most successful method to date for growing large SiC single crystals. In this method, an SiC source powder in a semi-closed crucible is sublimated and recrystallized on a seed crystal maintained at a slightly lower temperature. Although the sublimation technique is relatively easy to implement, having in mind that extremely high temperatures (over 2300°C) are needed, the process is difficult to control, particularly over large seed crystal area. Although significant progress has been made in the growth of SiC crystals, the growth processes governing the polytype control and the defect formation are still poorly understood.

Increasing the wafer diameter is crucial for reducing the cost of SiC devices through economies of scale and the use of Si or GaAs device fabrication lines. In this respect, much effort has been made over the last decade, leading to the recent fabrication of fully single crystal wafers with a diameter of up to 100mm [1]. The crystal quality, however, is generally largely degraded as the crystal diameter increases. This is due to the lack of an established methodology for expanding the single crystal area without degrading crystal quality. To achieve this, a high degree of control of both the transient and continuous thermal profiles during growth is required. We utilized the results of numerical simulation of the temperature profiles inside the crucible, taking into account heat transfer through conductive and radiative mechanisms, and then the results were combined with our compiled experimental database to figure out the key growth parameters for SiC crystal growth. This approach successfully allowed for diameter enlargement of up to three inches in our laboratories.

The most harmful defect in SiC bulk crystals is the so-called "micropipes" which are small pinhole defects that penetrate the entire crystal and cause critical flaws in SiC devices. We have recently proposed a surface step model for the micropipe formation in SiC crystals, taking into account several important aspects experimentally observed for micropipe formation [2]. Micropipes are very often observed at the foreign polytype and secondary phase inclusions during growth, where high density screw dislocations are introduced and the

spiral steps emanating from them interact with each other. The model assumes that the strong repulsive interaction between these steps [3] coalesce the unit  $c$  screw dislocations through the energetic bunching of the spiral steps. Spiral growth mechanism ensures stable lateral advancement of steps of multiple unit cell height, which kinetically prevents the dissociation of the bunched steps and thus prevents micropipes.

The presence of low angle grain boundaries and associated mosaicity in SiC crystals is also commonly observed, and they are fully replicated from the substrates into the device epitaxial layers by the thin film growth process and consequently have a major impact on the performance of SiC devices made on them. We have recently revealed that PVT SiC crystals have a strong [0001] texture around etch pit rows due to edge dislocation walls aligned along  $\langle 1\bar{1}00 \rangle$  directions [4]. The x-ray rocking curve with the incident plane parallel to the etch pit rows showed a narrow single diffraction peak, while the one with the incident plane perpendicular to the rows showed a much broader peak (40–80arcsec), often splitting into multiple peaks. Based on these results, we concluded that the tilting of the (0001) lattice plane has an axis of rotation parallel to both the boundary plane and the (0001) basal plane. We have also found that a major cause of the low angle grain boundaries in PVT SiC crystals is the inclusion of foreign polytypes during growth. The non-basal plane interfaces between the different polytypes accommodate crystallographic imperfections which relax into polygonized low angle grain boundaries during growth.

Over the past several years, a significant reduction in defect density has been achieved, and SiC substrates with low micropipe density and mosaicity have been successfully obtained. We discuss the causes and mechanisms of these crystallographic defects and demonstrate successful reduction of defect density in SiC crystals.

The final part of this paper deals with the growth of bulk SiC crystals perpendicular to the  $\langle 0001 \rangle$   $c$ -axis direction. Drastically enhanced channel mobility has been demonstrated for SiC MOSFET fabricated on the (11 $\bar{2}$ 0) surface [5]. This achievement naturally spurred crystal grower's interest in bulk crystal growth in the [11 $\bar{2}$ 0] direction, which is essential for the fabrication of SiC(11 $\bar{2}$ 0) substrates having a large diameter and reasonable uniformity of doping concentration. In this growth direction, the polytypic structure of grown crystals perfectly succeeds to that of the seed, and thus polytype mixing never occurs during growth, and more importantly, the growth prevents micropipe formation. However, the growth tends to yield a large number of basal plane stacking faults in SiC crystals, and the density of the stacking faults strongly depends on the crystal growth direction and polytype. We present an atomistic surface model for the stacking fault generation and discuss a possible way to circumvent this problem.

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