

Structural Defects

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Propagation of Current-Induced Defects and Forward Voltage Degradation in 4H-SiC PiN Diodes

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Optical Emission Microscopy of Structural Defects in 4H-SiC PIN Diodes

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Polytype Identification and Mapping in Hetero-epitaxial Growth of 3C on Atomically Flat 4H SiC Mesas Using Synchrotron White Beam X-ray Topography

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Behavior of the Micropipes during Growth in 4H-SiC

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Stress Distribution of 2 Inch SiC Wafer Measured by Photoelastic Method

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The Brittle to Ductile Transition in 4H-SiC

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Abstract

One of the proposed main applications for SiC devices is in high power systems such as voltage source converters in motors or HVDC transmission systems. For this kind of applications, the stability of the processed device is crucial. Recently it was shown that some devices can become electrically degraded during long term operation and that this degradation is related to the formation of structural defects in the material. [1] At this stage a comprehensive knowledge of the actual structure of the defects and most of all, the nucleation source for these, is required for a successful outcome of the SiC bipolar device technology. In this work the structural defects in degraded 4H-SiC pin diodes were studied by synchrotron white beam X-ray topography (SWBXT), scanning electron microscopy (SEM) with *in situ* cathodo luminescence (CL) and transmission electron microscopy (TEM).

Figure 1 displays a back-reflection topograph obtained from a reflection towards $\langle 01\bar{1}l \rangle$ of a degraded diode (edges outlined) as recorded by SWBXT. This image outlines triangular areas of dark contrast which are interpreted as stacking faults.

Figure 2a shows a TEM image of a cross-sectional sample prepared by FIB. The picture was taken in a condition where the SiC $\langle 1\bar{1}00 \rangle$ crystal zone-axis was parallel to the electron beam. The straight line seen in Figure 2a makes an angle of about 8° with respect to the surface. This shows that the defect is a stacking fault residing on the SiC basal plane. Figure 2b shows another area of the sample where also sets of parallel stacking faults were present. A defect was studied by high-resolution electron microscopy and the results are shown in Figure 2c. The image was obtained by orienting the $\langle 2\bar{1}\bar{1}0 \rangle$ zone axis in a condition so as to be parallel to the electron beam. It can be seen that the 4H stacking sequence ABACABAC is replaced by ABCBCACB.

We show that the particular stacking fault crystal defect is formed from an existing dislocation which splits into two partial dislocations resulting in a glide type [2] slip on the close packed (0001) basal plane. The slip is nucleated from a stress, acting upon the SiC epilayer, originating from the contact/epilayer interface. [3]

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Figure 1. This image was recorded from a reflection towards $\langle 10\bar{1}0 \rangle$. The diode edges are outlined and a dark contrast appears in the area of the triangular stacking fault.



Figure 2. TEM image of the sample prepared by FIB. A straight line corresponding to the stacking fault runs through the crystal in a) and in b) this set of stacking faults was found. A high resolution TEM image of the defect is finally shown in c).

Propagation of Current-Induced Defects and Forward Voltage Degradation in 4H-SiC PiN Diodes

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Bipolar semiconductor devices stand to benefit greatly by replacing silicon with SiC, especially in high-voltage and high-temperature applications. In addition to the increase in performance afforded by the physical properties of SiC, SiC devices are expected to exhibit higher tolerance to extreme ambient conditions. For these devices to be used in industrial or military applications, their stability and reliability must be proven. Recently, long-term reliability tests of 4H-SiC PiN diodes have indicated that while leakage currents remain stable at constant reverse bias, some devices exhibit increased forward on-state voltage with time under constant forward current [1].

This paper investigates current-induced defect propagation in implanted anode 4H-SiC PiN diodes fabricated on 10-15 μm n-type epi layers grown on n^+ substrates. The p^+ anode, three-zone p-type junction termination extension (JTE), and n^+ field stop were sequentially implanted achieving a planar device structure. The anode area is $6.3 \times 10^{-3} \text{ cm}^2$. Devices with windows in the anode metallization were also incorporated to allow for the observation of light emission across the device under electrical bias.

The characteristics of defect propagation have been examined by combining electrical measurements with optical imaging of the defects. Two striking features were that the degradation of diodes on the same wafer can vary by an order of magnitude and that the degradation varied smoothly as the wafer is traversed. Long-term electrical test data from a row of diodes from wafer center (0,0) to wafer edge (-10,0) are shown in Fig. 1. These devices have an anode with a continuous metal overlay. At room temperature, with a stressing current of 0.5 A (80 A/cm^2) the voltage degradation ranged from 0.2 to 2 V. The voltage increase with time for this set of diodes is shown in Fig. 2. While the magnitudes of the voltage increases were very different, all exhibit the most rapid increase within the first few hours and changed much less slowly after 5 hours. Fig. 3a-f shows a sequence of images for one of the window anode devices where the diode is held in forward bias at a constant current of 0.5 A (80 A/cm^2) at room temperature. The images show dark line features in the light emission, which appear within 20 minutes and propagate perpendicular to the primary wafer flat. After greater than 3 hours of constant bias, no further dark-line propagation was observed for this device. This time dependence is consistent with the forward voltage increase plotted in Fig. 1. Increasing the current to 1 A (160 A/cm^2) strongly accelerated the rate of defect formation.

Based on our electrical results and time-lapse sequences of images, it is possible to make a number of observations about the degradation mechanism. The dark line features are attributed to a localized reduction of carrier lifetime caused by an extended defect, most likely a stacking fault [2]. In these regions of low carrier lifetime, the electron-hole plasma in the drift layer is suppressed, resulting in weaker light emission and lower current. Before current stressing few, if any, defects are observed. However, we assume that there are pre-existing and unobserved defects that are present and the density of these defects is not uniform. The identity of these pre-existing defects has not yet been determined. Based on the smooth variation of degradation observed in Fig. 1, the density of these defects appears to vary on a length scale on the order of a few mm. Once defects nucleate and start propagating, all have a similar growth velocity. This velocity strongly depends on the current. The defects grow in the $\langle 1100 \rangle$ direction and often grow until they span the diode. In other cases, growth abruptly stops as the growth front is pinned. During the operation of the diode, new dark line defects are continually being generated. Defect generation rates are greatest during the first minutes of operation. Initially, new defects are started at the highest rate. At longer times, when the electrical degradation has saturated, the rate of new defect starts is much lower. The growth dynamics of individual defects that start later do not appear to be different from those that start earlier.

Work is in progress to study the current dependence of defect formation in more detail and to examine its temperature dependence. We are also investigating possible precursors for this effect by looking at micropipe maps and cross-polarizer images on starting material.

In conclusion, the combination of electrical measurements and emission images provides a powerful approach to examining the defects responsible for the degradation of the forward I-V characteristics of SiC PiN diodes.

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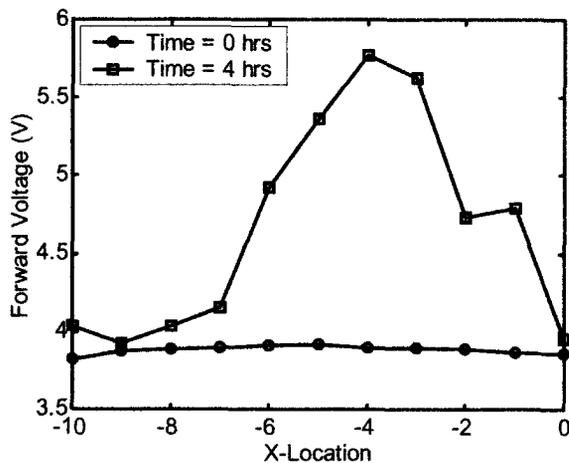


Fig. 1 PiN diode forward voltage versus time at various locations at a constant current of 0.5 A.

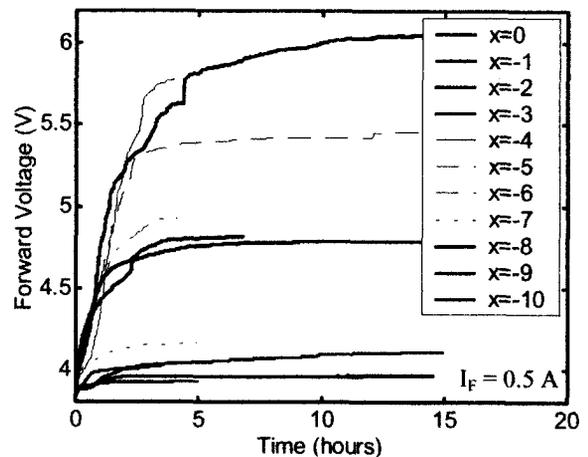


Fig. 2 PiN diode forward voltage versus position on wafer at 0 and 4 hours. The wafer center is denoted (0,0) and the edge as (-10,0).

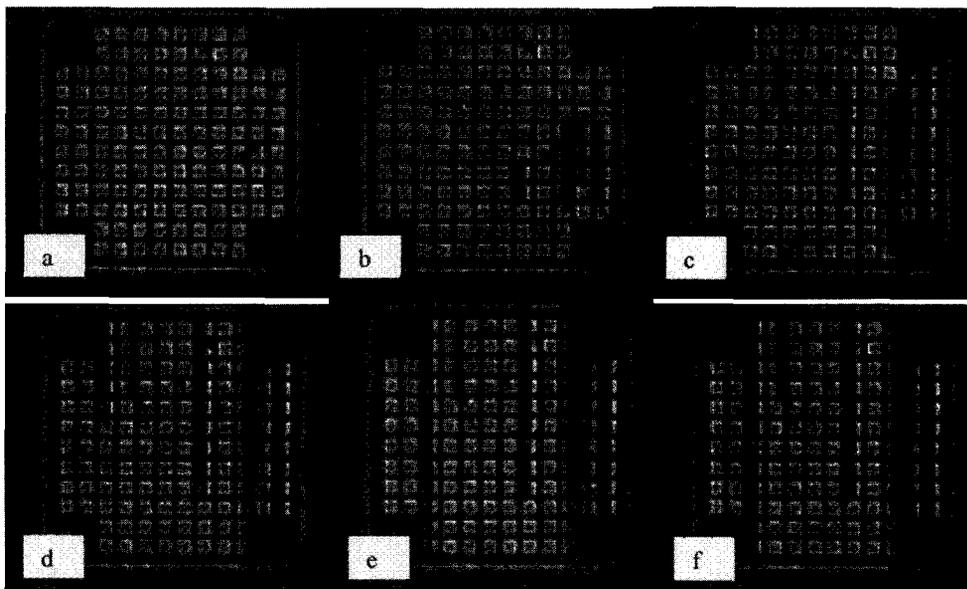


Fig. 3 Light emission from a PiN diode with anode windows at a constant current of 0.5 A at various time intervals (a) 0 hr, (b) 0.3 hr, (c) 1 hr, (d) 2 hr, (e) 3 hr, (f) 3.7 hr.

Optical Emission Microscopy of Structural Defects in 4H-SiC PIN Diodes

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A phenomenon apparently affecting the long-term stability of SiC power device performance was recently introduced by [1]. In present work, we report studies of inherent and long-term operation induced structural defects in 4H SiC PIN structures by employing an optical emission microscopy (OEM) technique. This experimental method was further developed to provide spectrally resolved 3D information by combining imaging of recombination radiation emitted from the backside and cross-sectional plane of forward biased diodes (EL) with a dark field photoluminescence (PL) technique. A variable wavelength laser source was utilized for either resonant band-to-band, or below-band excitation and ensured a homogeneous pump light penetration throughout the probed volume. The PL imaging has exhibited a good correlation with EL data and also revealed presence of some structural features in the active region not observable in EL patterns. The utilized combination of PL and EL methods with OEM is proved to be an extremely effective tool in mapping and analysis of structural defects.

We demonstrate that a successive imaging of emission from the investigated 4H-SiC PIN structures makes possible real time monitoring of the electrical stress related phenomena. In this way, a rapid migration ($>50 \mu\text{m/s}$) of dislocation pairs across the active area of devices was observed *in situ* using backside EL geometry. This propagation is presumably originated by thermal-stress and seems to be terminated once a structural defect is met on the way. An extensive planar defect with a characteristic bright-line edging is then generated throughout entire epitaxial layer. An enhanced, i.e., digitally processed cross-polarized EL imaging was utilized to expose the built-in strain fields around individual dislocations and to reveal the locations of micropipes and elementary screw dislocations. Interestingly, some of EL patterns indicate that these defects could also be responsible for the pinning of the further bright-line expansion. Finally, a cross-sectional imaging has directly provided a 3D outline of the stress-induced defects, indicating clear match with the basal plane. A spectral content of emission obtained solely from the stress-induced features is compared with the luminescence spectra from defect-free areas at different current densities and temperatures.

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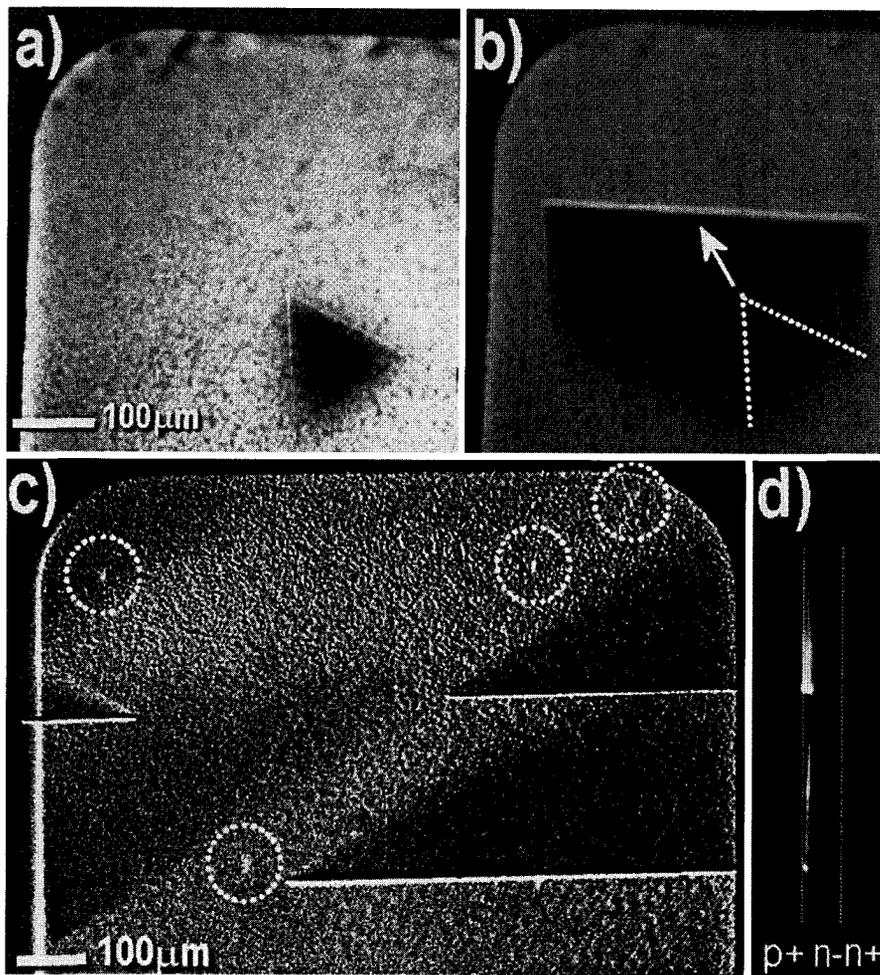


Fig. 1. Imaging of the EL emission from 4H-SiC $p^+/n^-/n^+$ structures: fast migration ($>50 \mu\text{m/s}$) of dislocation pairs across the active area of electrically stressed devices was observed in real time (a). This propagation seems to be terminated once a structural defect is met on the way, and an extensive planar defect with a characteristic bright-line edging is generated throughout entire epitaxial layer (b). An enhanced (cross-polarized) EL imaging was utilized to expose locations of the built-in strain fields around micropipes and screw dislocations (c). A cross-sectional imaging has provided both a 3D outline and spectral contents of emission solely from the stress-induced features (d).

Polytype Identification and Mapping in Heteroepitaxial Growth of 3C on Atomically Flat 4H SiC Mesas using Synchrotron White Beam X-ray Topography

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The identification and mapping of the polytype distribution in nominally 3C heteroepitaxial films grown on atomically flat regions of 4H-SiC using synchrotron white beam X-ray topography (SWBXT) is reported. The procedure for producing the atomically flat regions, which was recently reported [1], consists of promoting step-flow growth on commercial SiC wafers, with surface orientations nominally (0001) (which, in fact, means slightly offset from (0001) by a fraction of a degree), which have had arrays of device-size mesas etched onto them prior to epitaxial growth. Some of these mesas encompass axial screw dislocations that typically occur scattered across the area of SiC semiconductor wafers [2] and some do not. The step flow mode of growth causes the atomic steps to grow out of existence on the vast majority of mesas free of the axial screw dislocations, leaving these mesas with a large basal plane surface tilted with respect to the original surface. Such a large, step-free basal plane surface is potentially useful for improved heteroepitaxy, as the presence of substrate surface steps has been shown to cause defects, in particular double positioning boundaries (DPB's), in heteroepitaxial films [3,4]. To confirm the feasibility of this approach, SWBXT was carried out to identify and map the distribution of polytypes in wafers subjected to these procedures. In order to achieve this, specific use must be made of both the structural and microstructural capability of the technique. This requires analysis of the spatial distribution of those regions of crystal that produce diffracted intensities which indicate the presence of one or other of the two 3C variants (3C I and II, related by a 60°, or equivalently, a 180° rotation about the 4H [0001] axis). Here we report on such studies carried out on two wafers. The first (wafer 1), was a non-optimal sub-region of one of the 4H-SiC wafers that was described in [1] that was subjected to the procedure for production of atomic flatness. The sub-region of interest, located near the wafer edge, experienced imperfect control of the local supersaturation and significant 2D terrace nucleation of the two variants of 3C polytype was inadvertently produced. This sample served to demonstrate the capability for polytype mapping. The second (wafer 2) consisted of a 4H wafer where more controlled heteroepitaxy was carried out following the successful production of the atomically flat mesas. This sample served to demonstrate proof of concept of two issues: (1) to confirm that dislocation-free mesas could be made atomically flat and (2) that complete DPB-free coverage of these atomically flat mesas by one or other of the 3C polytype variants could be achieved. In addition to SWBXT, supplemental thermal oxidation color mapping, Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) was carried out.

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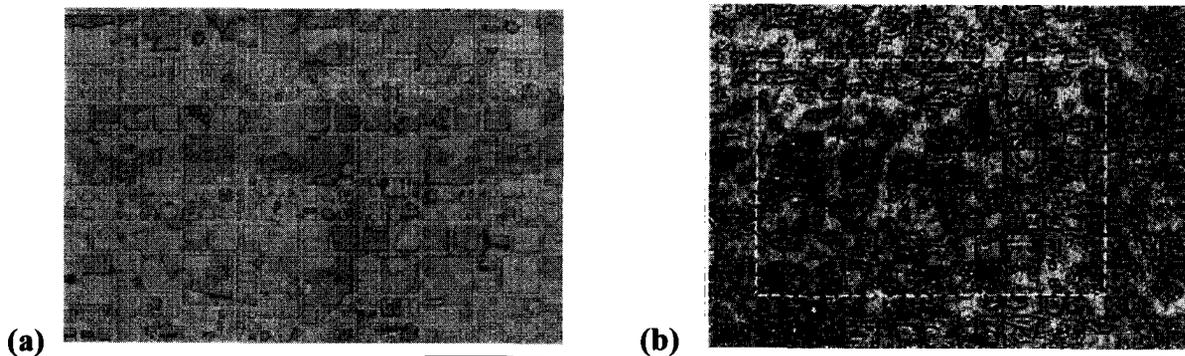


Fig. 1(a) Oxidation color map of part of wafer 1, with unintentional nucleation of 3C polytype; **(b)** Back-reflection SWBXT image showing defect microstructure. The area of correspondence with Fig. 1(a) is outlined. Regions where 3C has nucleated are surrounded by dark line contrast associated with a small tetragonal distortion. Scale marks = 1mm.

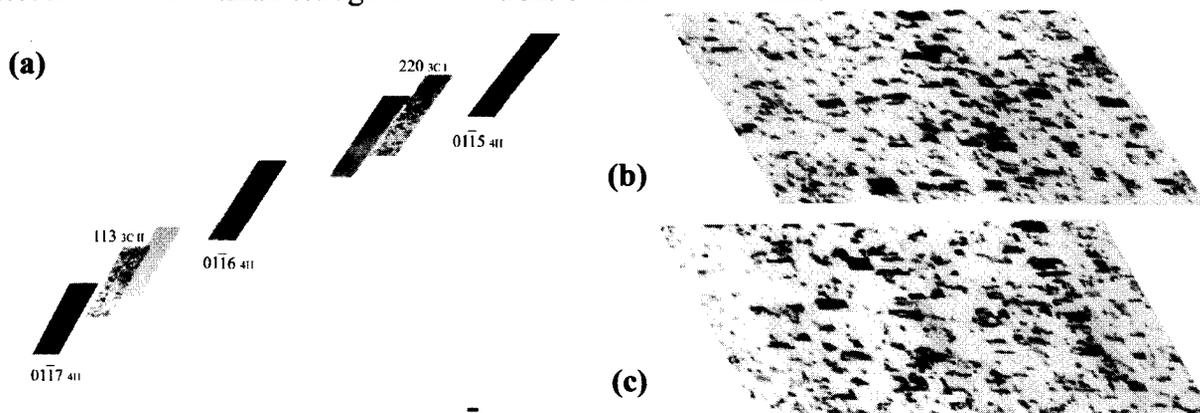


Figure 2(a) Selected area from reflection diffraction pattern recorded from wafer 1; **(b)** and **(c)** composite images showing the distribution of 3CI **(b)** and 3CII **(c)**. Colors were then assigned to these images and, following image processing to remove the geometric distortion, they were superimposed on Fig. 1(b), as shown in Fig. 3(a). Scale marks = 1mm

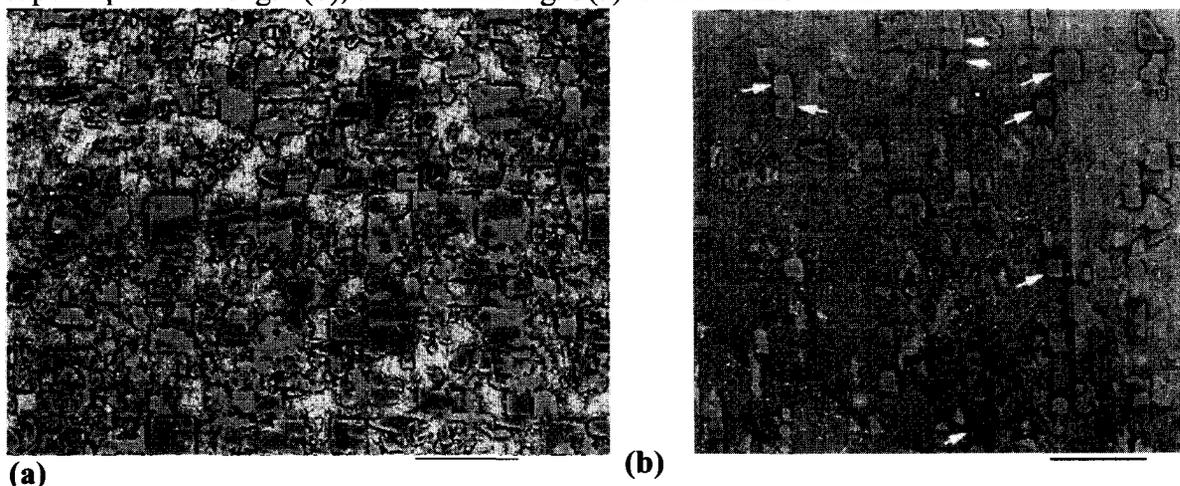


Fig. 3 Composite images showing the distribution of 3CI and 3CII over the surface of **(a)** wafer 1, and **(b)** wafer 2. Note mixtures of 3C polytypes on mesas in **(a)** and the presence of mesas with complete, uniform 3C overgrowth, as indicated by arrows, in **(b)**. Scale marks = 1mm.

Behavior of the micropipes during growth in 4H-SiC

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The improvement of the SiC wafers is substantial for the increase of the yield of the fabricated devices. The SiC wafers suffer from different types of defects, as dislocations, planar defects, carbon and silicon inclusions, low angle boundaries and micropipes. Especially the last ones are detrimental for the device performance, due to their large diameter [1]. A micropipe is usually formed after the breakdown of a screw superdislocation at high temperature, when a hollow core is spontaneously generated [2, 3] Micropipes can be also generated at inclusions or voids [4]. The last few years the micropipe density has been significantly reduced by better controlling of the kinetics during growth [1], or by micropipe healing using liquid phase epitaxy [5]. It is evident that the better understanding of the behavior of the micropipes during growth can lead to a further reduction of the their density.

In this paper evidences for the role of micropipes in extended defect formation are presented. The study is based on Atomic Force Microscopy (AFM) and Transmission Electron Microscopy (TEM) observations.

The 4H-SiC specimen with a thickness of about 50 μm was grown by sublimation epitaxy at 1750C on Si-face, 8 degree off 4H substrate. Details of the growth geometry and procedure are described elsewhere [6]. From the AFM images, it was evident that in some cases the micropipes were related to a shallow trench at the surface as shown in Fig.1. The trench is always extended from the one side of the corresponding micropipe. The trenches coincide with the direction of the growth steps and they may extend up to 500 μm in length. In general the width of the trench corresponds to the diameter of the micropipe, the depth of the trench is between 30 to 140nm as measured by the corresponding profiles. Inside the trench the growth steps due to the lateral growth are distorted towards the direction of the pipe. Therefore the shallow trenches were related with a retardation of the steps due to the micropipe. It is worth noting that the steps are not broken in the trench, but they remain continuous.

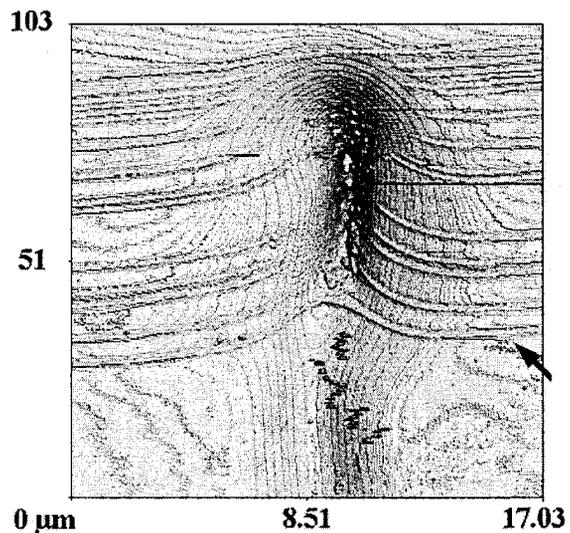


Fig. 1. AFM image of a trench-like defect extended from a micropipe. The arrow points to the steps.

The characterization of the trenches was completed by TEM observations. Due to the very large size (a few μm) and the very low density (10 to 100 cm^{-2}) of the micropipes it was difficult to locate the area of interest due to the very small field of observation provided by the TEM. Due to these limitations the specimen for the TEM characterization was prepared after location of the trench by the AFM. The area of interest was thinned only from the backside up to a thickness of about 200nm . The TEM micrograph including a part of the trench is shown in Fig.2. The bending of the periodic growth steps inside the trench is evident. In the inset in the left upper corner of the picture a magnified image of the origin of the defect is shown. The contrast of these fringes is attributed to surface ripple due to the step propagation and disappears when the specimen is thinned from the front side. The corresponding diffraction pattern from this area confirms the propagation of the trench along the $[1\ 1\text{-}2\ 0]$ direction.

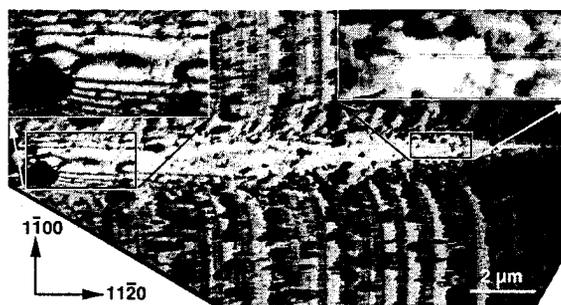


Fig. 2. TEM micrograph of the defect showing the bending of the steps and two insets with details.

A planar defect was also observed running inside the trench and parallel to its axis, as shown in Fig.2. The planar defect lies on the $(1\text{-}1\ 0\ 0)$ plane seen edge on in Fig.2. Details are shown in the upper right inset in Fig.2. In additional images it was evident that a dislocation can be found in the vicinity of the planar defect. We believe that this defect is a stacking fault, which is formed due to misalignment of the growth planes. In order to exclude the case of an artifact produced by a step parallel to $[1\ 1\text{-}2\ 0]$ direction the same specimen was thinned from the front side so that the growth steps and the trench were smeared out. The contrast of the planar defect persists revealing that it is related with the bulk SiC. The formation of the trench-like defect starting from pipes and extending along the flow direction of growth steps may be related to the high V_C/V_A ratio, where V_C is the normal growth velocity and V_A is the tangential component. Synchrotron X-ray topographs reveal dark contrast associated with the defect which might suggest that stress is present during the layer growth. Additional information regarding the relation of the planar defect with the slip trace will be presented.

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Stress distribution of 2 inch SiC wafer measured by photoelastic method

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1. Introduction

Large size defects (for example micropipe and planar defects) were studied for years. SiC-based device technology has made remarkable progress in recent years with decreasing the defects density year by year [1] and the supplier is demanded to decrease more small size defects and stress field.

Sub-grain boundaries were made from stress fields [2]. Not only sub-grain boundaries, but also almost defects occurred by the stress field, which has several origins, thermal, physical and so on. But it is difficult to make clear how to occur these stress fields and the distribution in situ. Because SiC bulk grown by sublimation is occurred in the closed graphite crucible.

So, we tried to observed stress field of the grown SiC wafer by several methods. Kato et. al researched internal stress around the micropipe by the polarizing optical microscope[3]. And the area of existing sub-grain boundary was corresponded with the stress field by cross polarizer and the FWHM(Full Width at Half Maximum) of the rocking curve of X-ray diffraction became large[2]. But we want to know easily the distribution of stress field in the SiC wafer. So we made photoelastic system using the sensitive color plate between the polarizer and analyzer and observed the little double refraction and this orientation.

2. Experiment

The samples were 2 inch 6H-SiC (0001) just wafers made by sublimation method. The wafer thickness was 1mm. Figure.1 shows the schematic system of photoelastic method. The source of light was the white light. The sensitive color plate was cellophane paper, whose retardation was about 500nm and color was orange. We observed the change of color by rotating the sample. If the sample has retardation about +200nm, the color-changed blue, if it has the retardation about -200nm, the color changed yellow. We can know which the force is compress stress or tensile stress from these results.

If the sample is not (0001) just wafer and has some off direction, the oval polarized light is occurred. So we confirmed the samples which are (0001) just wafers.

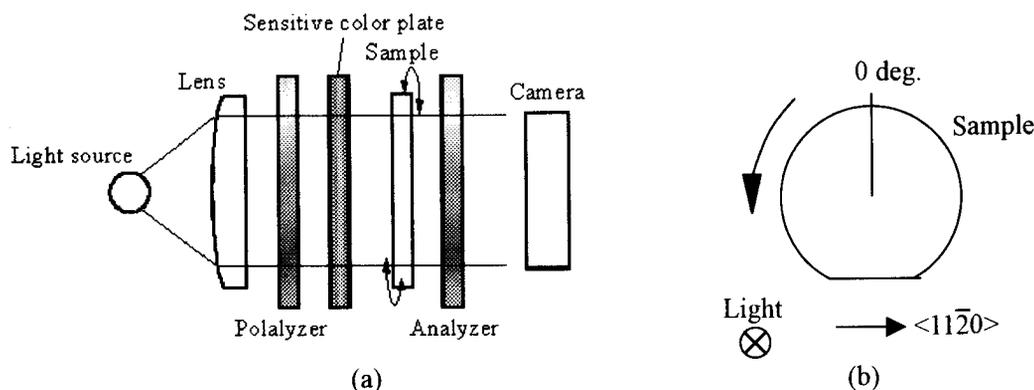


Fig.1 Schematic photoelastic method system

3. Results

Fig.2 (a) and (b) show the photoelastic images whose wafers position were 0 degree and 60 degree, respectively. We decided the wafer position named 0 degree when the wafer positioned like fig.1 (b) and 60 degree means the wafer rotated 60 degree to counterclockwise direction. By comparing with fig.2 (a) and (b), we found the violet area moved to counterclockwise direction but the violet color of (b) became lighter than that of (a). It means the x-axis of sample (x-axis corresponded with the short axis of the ellipse) is $\langle 1-100 \rangle$ direction. This sample is compressed in x-axis direction. Normally the sample was influenced with compress stress along $\langle 1-100 \rangle$ direction and with tensile stress along $\langle 11-20 \rangle$ direction. And from fig.2, the color-changed area exist at peripheral area very much.

And we can observe easily stripes, which corresponded with sub-grain boundary. The crystal is closed to graphite crucible wall in sublimation method. So we think the one of the origins of the sub-grain boundary at peripheral area were the thermal expansions between graphite and SiC grown crystal[2].

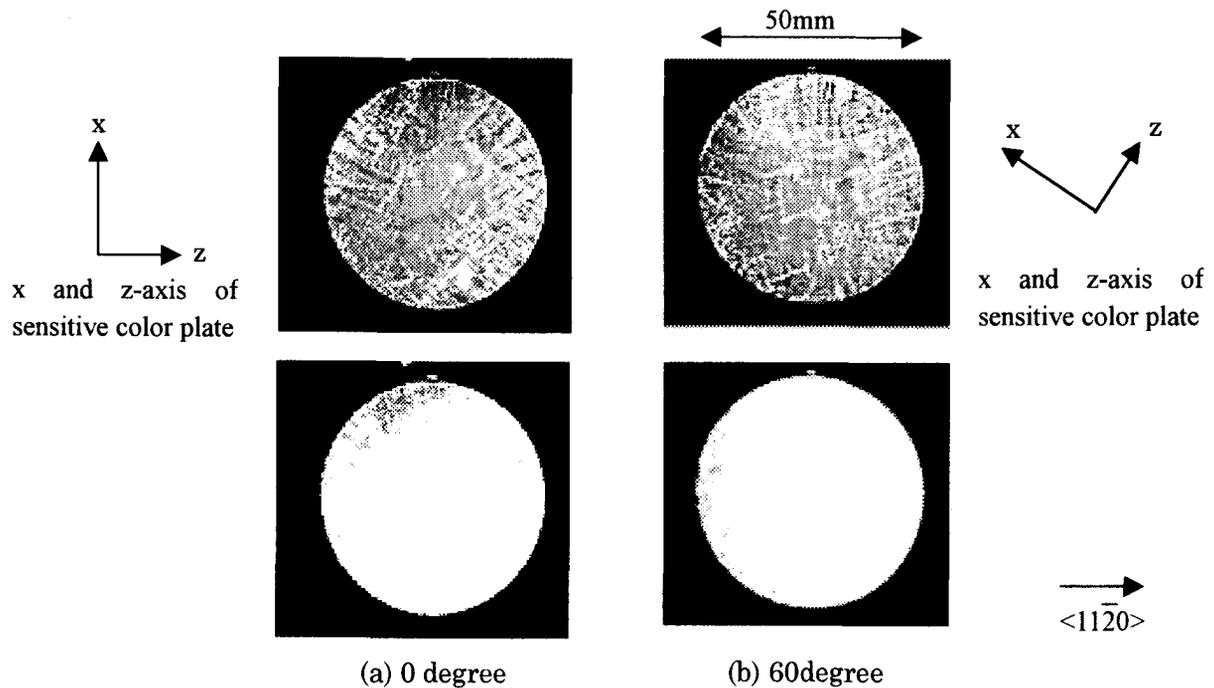


Fig.2 Photo elastic image of 2 inch SiC wafer. The upside images of (a) and (b) were changed to gray scale image, but almost area looked orange and downside images were extracted the violet area.

Reference

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The Brittle to Ductile Transition in 4H-SiC

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The brittle-to-ductile transition (BDT) temperature, T_{BDT} , in semiconductors is an important parameter separating the temperatures over which the material yields by plastic deformation from those at which it fails catastrophically by fracture. Extensive work on this transition in many semiconductors has shown that T_{BDT} is very sharp generally occurring over a temperature range of a few degrees centigrade and it shifts to lower temperatures at lower strain rates. In this paper, we have used the technique of 4-point bend test to measure the BDT temperature of pre-cracked single crystal 4H-SiC. The samples were deformed at temperatures from 800°C to 1300°C and at two different strain rates, $\dot{\epsilon} \approx 5 \times 10^{-7} \text{ s}^{-1}$ and $\dot{\epsilon} \approx 5 \times 10^{-6} \text{ s}^{-1}$. At $\dot{\epsilon} \approx 5 \times 10^{-7} \text{ s}^{-1}$, the BDT temperature has been determined to be $\sim 1005^\circ\text{C}$ while at $\dot{\epsilon} \approx 2.6 \times 10^{-6} \text{ s}^{-1}$, T_{BDT} shifts up to $\sim 1175^\circ\text{C}$. The shear stresses at which the samples yield plastically above T_{BDT} are consistent with the values measured by direct compression experiments, and the values of T_{BDT} appear to be consistent with the transition temperature measured by direct plastic deformation of 4H-SiC. The experimental results will be presented and discussed in the light of a new model for the brittle-ductile transition in tetrahedrally coordinated semiconductors.