

Bipolar and PN Junction

Measurements and Device Simulations of Avalanche Breakdown in High Voltage 4H-SiC Diodes Including the Influence of Macroscopic Defects

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High-Voltage SiC pin Diodes with Avalanche Breakdown Fabricated by Aluminum and Boron Implantation

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Recombination-Enhanced Defect Formation in High Voltage SiC Diodes

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Electrical Characterization of High-Voltage 4H SiC Diodes on High-Temperature CVD Grown Epitaxial Layers

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Investigation of Thermal Properties in Fabricated 4H-SiC High Power Bipolar Transistors

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Improvement and Analysis of Implanted-Emitter Bipolar Junction Transistors in 4H-SiC

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All-SiC Half Bridge Inverter Characterization of 4H-SiC Power BJTs Up to 400 V-22 A

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Measurements and device simulations of avalanche breakdown in high voltage 4H-SiC diodes including the influence of macroscopic defects

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SiC high voltage diodes have important applications as freewheeling diodes in motor drives and power transmission systems. A stable avalanche, which is very important for diode reliability, cannot be taken for granted in SiC due to high concentrations of macroscopic defects. The influence of screw dislocations (SDs) on avalanche breakdown in 4H-SiC was examined by Neudeck [1] who found a typical breakdown voltage reduction by 30 % in low voltage diodes ($V_{br}=90$ V) with SDs, but a high and similar avalanche energy to fail for diodes with and without SDs. This paper addresses the breakdown characteristics of high voltage 4H-SiC diodes with an area large enough that screw dislocations are most likely present. An important effect at high voltages, in addition to a high power dissipation, is that the space charge of free carriers can produce a negative resistance [2]. This effect becomes most pronounced for high voltage diodes since it occurs as the free carrier concentration in the drift region becomes roughly equal to the doping concentration [2]. Device simulations of reverse I-V characteristics were performed using the commercial software AVANT! Medici with physical models according to [3]. The high voltage diodes, which were experimentally investigated, are p^+nn^+ diodes with an implanted p^+ emitter and a similar design as described in [4]. The expected breakdown voltage is 3000-4000 V. The critical field strength (E_{crit}) was reduced by 20 % (to obtain ~30 % V_{br} reduction) in simulations to model breakdown in a SD, since each of the investigated 1 mm^2 area diodes should contain several SDs. Fig. 1 shows a 1D simulation of the reverse I-V characteristics in breakdown together with 2D cylindrical coordinate simulations (to be described). The onset of negative resistance in the 1D simulation occurs at a current density of 6000 A/cm^2 , as the average carrier concentration differs only 2 % from the n-base doping in good agreement with [2]. To include current spreading in the n-base, 2D cylindrical coordinate simulations were performed with E_{crit} reduced by 20 % only inside a cylindrical region of varying radius (R) with base areas at anode and cathode. Fig. 1 displays simulated normalized current density (J_{norm}), i.e. the current divided by the area of the region with reduced E_{crit} . The reason for the much higher J_{norm} at the onset of negative resistance in the 2D simulations compared to 1D is current spreading which reduces the free carrier space charge in the n-base. As the onset of negative resistance is reached, however, a high current density filament is formed through the cylindrical region with a reduced E_{crit} . This current filamentation is assumed to be destructive. The isothermal conditions simulation conditions are valid only during very short times for the highest current densities in Fig. 1. The results indicate, however, that an unstable avalanche can occur at lower current densities in a macroscopic defect with a larger area, such as for instance a micropipe, for which a lower value of E_{crit} should be used in simulation.

Five diodes, of similar design as in ref. [4], with 1 mm^2 area and an expected breakdown voltage of 3000-4000 V were tested with reverse bias pulses of $4\text{ }\mu\text{s}$ pulse-width. Three of the diodes which had static breakdown voltages of 2000, 3400 and 2700 V failed destructively in

pulsed measurements at the voltages 3200, 3670 and 3700 V, all within 2 μ s after reverse biasing after a maximum avalanche current of 5 mA. All three diodes had a visible damage at the junction edge along the surface and this edge breakdown presumably damaged the diodes before a significant avalanche was reached in a SD as can be expected above 4000 V (see Fig. 1). The remaining two diodes (D1 and D2) had a low static breakdown voltage of about 700 V but could be pulsed into breakdown at high currents. Fig. 2 shows the quasi-static reverse I-V characteristics of D1 and D2 as obtained during 4 μ s pulses. Also shown in Fig. 2 are simulations with a 70 % reduction of E_{crit} in a cylindrical region with $R=15 \mu$ m, in one case through the whole epilayer and in the other only in the pn junction region. The results in Fig. 2 suggest that the diodes D1 and D2 have a reduced critical field strength mainly in the pn junction region. The high resistance of the diode in simulations is caused by the space charge limited current and is hence quite sensitive to the radius of the region with reduced E_{crit} . The diodes D1 and D2 also survived a fast turn-off from 1 A forward current to 1500 V reverse bias with a visible avalanche current. A negative temperature coefficient of the breakdown voltage was seen for D1 and D2 as an increasing current during longer pulses. Additional measurements are planned for diodes with even higher breakdown voltages.

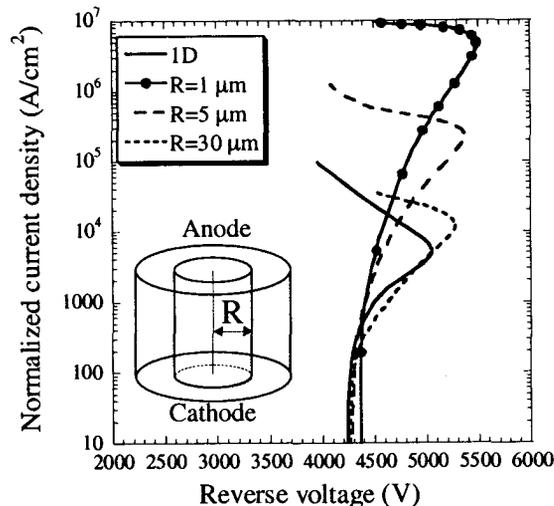


Figure 1: Simulated reverse I-V characteristics of diodes with 20 % reduced E_{crit} , 1D simulation and 2D cylindrical coordinate simulations with E_{crit} reduced inside $R=(1, 5, 30) \mu$ m

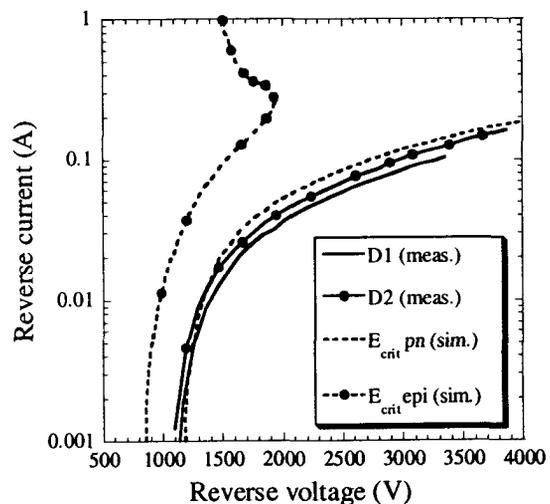


Figure 2: Pulsed reverse I-V measurements for diodes D1 and D2 and cylindrical coordinate simulations with 70 % reduced E_{crit} inside $R=15 \mu$ m in the pn junction region (pn) and through the whole n-base (epi)

Acknowledgements

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References

- [1] P. G. Neudeck et. al., *IEEE Transactions on Electron Devices*, vol. 46, p. 478 (1999)
- [2] H. Egawa, *IEEE Transactions on Electron Devices*, Vol. ED-13, p. 754 (1966)
- [3] M. Bakowski et. al., *phys. stat. sol.*, vol. 162, p. 421 (1997)
- [4] H. Lendenmann et. al., *Materials Science Forum* Vols. 338-342 p. 1423 (2000)

High-Voltage SiC pin Diodes with Avalanche Breakdown Fabricated by Aluminum or Boron Implantation

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The characteristics of planar pn junction are a key issue which controls the performance of various power devices such as pin diodes and DIMOSFETs. In SiC processing technology, high-dose Al⁺ implantation has been a major obstacle, because of its high sheet resistance of 10 kΩ/□ [1]. Regarding the pn junction characteristics, a positive temperature coefficient of breakdown voltage is one of the most crucial requirements for reliable power devices. Many SiC diodes generally show, to our knowledge, negative temperature coefficients except one report [2]. In this study, the authors realized a low sheet resistance below 4 kΩ/□ by hot implantation of Al. A clear positive temperature coefficient of breakdown voltage is also demonstrated.

N-type 4H-SiC (0001) epilayers with a donor concentration of $4 \times 10^{15} \text{ cm}^{-3}$ grown in the authors' group were used in this study. Multiple implantation of Al⁺ (10~180 keV) was carried out to obtain a 0.25 μm-deep box profile of Al. The implantation temperature was RT or 500 °C. Post-implantation annealing was performed at 1600~1700 °C for 30 min in Ar ambience.

Figure 1 shows the measured sheet resistance of Al⁺-implanted regions as a function of total implant dose. The sheet resistances and electrical activation of Al⁺-implanted regions were significantly improved by hot implantation and by increasing annealing temperature up to 1700 °C. A low sheet resistance of 3.6 kΩ/□ was obtained by implantation at 500 °C followed by annealing at 1700 °C, when the total implant dose was $4 \times 10^{15} \text{ cm}^{-2}$.

Pn junction diodes with planar structure were fabricated by employing B⁺ or Al⁺ implantation at room temperature. The junction depth was 0.4 or 0.7 μm with an implanted impurity concentration of $2 \times 10^{18} \text{ cm}^{-3}$. The implantation was carried out for 20 μm-thick n-type 4H-SiC epilayers ($N_d = 3.5 \times 10^{15} \text{ cm}^{-3}$). To reduce the contact resistance on the implanted regions, surface p⁺-regions were formed by Al⁺ implantation at 400 °C. The diodes were annealed at 1700 °C for 30 min. The surface of diodes was passivated with SiO₂ formed by wet oxidation.

Figure 2 demonstrates the current density vs voltage characteristics of deep B⁺-implanted diodes with a diameter of 100 μm measured at RT. The specific on-resistances determined at 100 A/cm² level were 6.3~9.1 mΩcm². These on-resistances include the substrate resistance of 4.1 mΩcm², so that, the contact resistances onto the shallow Al⁺-implanted p⁺-region estimated to be less than 2.2 (6.3 - 4.1) mΩcm². These results indicate that good ohmic contacts were formed by shallow Al⁺ implantation at 400 °C. The diodes exhibited stable and reversible breakdown, in particular, deep B⁺-implanted diodes did not extend to destructive breakdown even at a high reverse current density of 3.0 A/cm² and a reverse voltage of 2600 V. This 2600 V is 80 % of the ideal (parallel

plane) breakdown voltage (about 3200 V) in this device structure. This unusually high breakdown voltage might originate from the formation of a thick *i*-layer due to the indiffusion of B [3] and/or from the extension of space charge regions caused by effective negative charges at the SiO₂/n-SiC interface [4]. Regarding switching, the diodes showed fast switching with a turn-off time of 10 ns.

Figure 3 shows the reverse blocking characteristics of (a) Al⁺- and (b) deep B⁺-implanted diode, measured at RT, 335 K, and 373 K. At RT, the Al⁺- and deep B⁺-implanted diodes could block 1020 and 2900 V, respectively, which were approximately 32 and 90 % of the ideal breakdown voltage. The breakdown voltage of each diode increased with increasing temperature. This positive temperature coefficient of reverse breakdown voltage means avalanche breakdown, not other mechanism such as defect-assisted tunneling.

- [1] J. W. Palmour et al., *Diamond and Related Materials*, **6**, 1400 (1997).
- [2] H. Mitlehner et al., *Proc. 1998 Int. Symp. on Power Semicond. Devices & ICs (Kyoto, 1998)*, p.127.
- [3] G. Pensl et al., *Phys. Conf. Ser.*, **142**, 275 (1996).
- [4] H. Yano et al., *IEEE Trans. Electron Device*, **46**, 504 (1999).

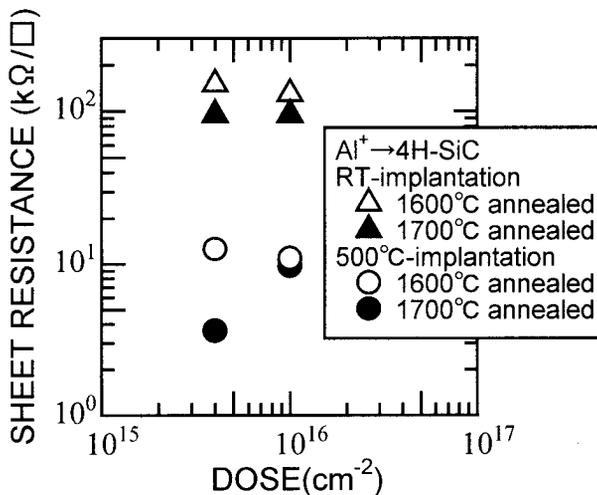


Fig. 1. Dependence of sheet resistance for Al⁺-implanted 4H-SiC layers on total implant dose after 1600°C and 1700°C annealing.

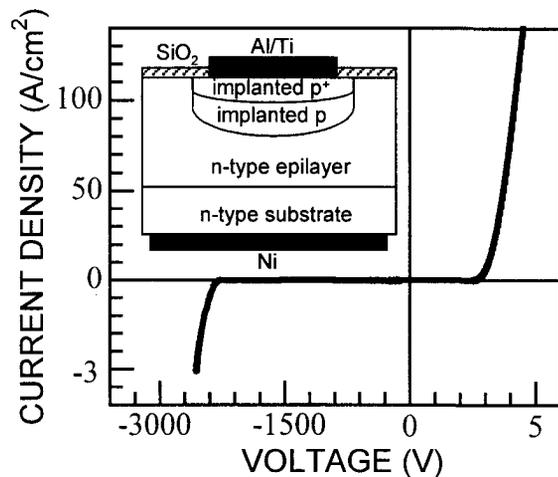


Fig. 2. Current density vs voltage characteristic of deep B⁺-implanted diode.

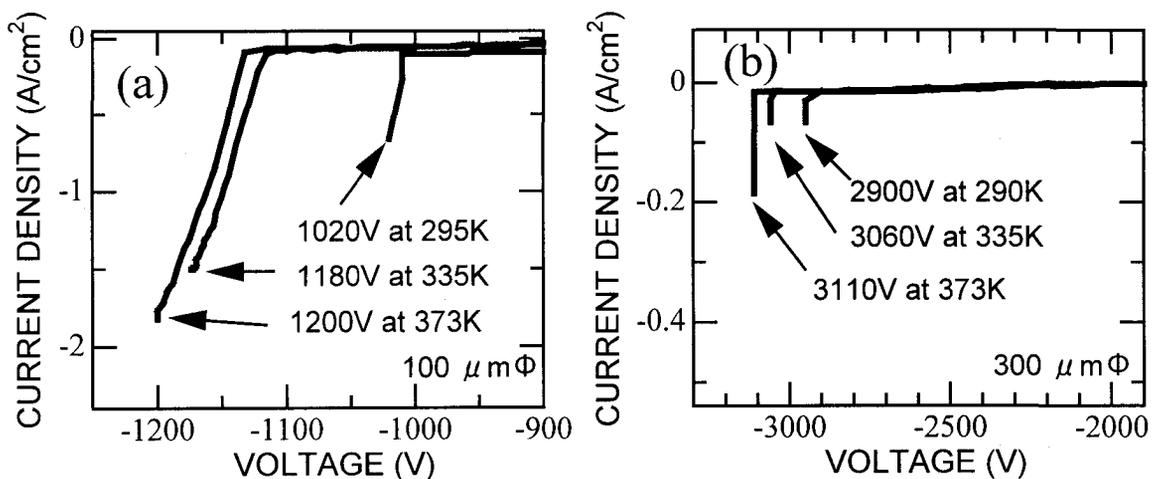


Fig. 3: Reverse blocking characteristics of (a) Al⁺- and (b) deep B⁺-implanted diode.

Recombination-enhanced defect formation in high voltage SiC diodes

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Recent long term reliability tests of SiC p-n diodes revealed increase of forward voltage drop occurring over a period of hours or days under forward bias¹. The electrical characterization results were interpreted as a consequence of recombination-enhanced stacking faults formation based on x-ray topography and luminescence characterization results². This report describes the structure of bias-induced defects studied by conventional and high resolution transmission electron microscopy and discusses the formation mechanism.

High voltage 4H and 6H-SiC p+-n- junctions were stressed at current density of 100 A/cm². Cross-sectional samples have been prepared and analyzed using Philips 420 microscope operating at 120 kV and JEOL 400EX microscope operating at 400 kV. Stressed diodes contained typically between 0.2×10^4 and 2×10^4 cm⁻¹ faults distributed between the metal/semiconductor and epilayer/substrate interfaces. The cross sections of “virgin” device structures were defect free. The stacking sequences of multiple faults in both 4H- and 6H-SiC polytypes have been analyzed using high resolution microscopy. The structure of all defects was consistent with isolated Shockley-type faults (Fig. 1). Such faults in silicon carbide crystals were reported to form during plastic deformation at low temperatures³. The analysis of stacking sequences and of partial dislocations bounding the faults indicates that the driving for formation of defects is shear stress present in the diode structure. The stress is macroscopic in origin.

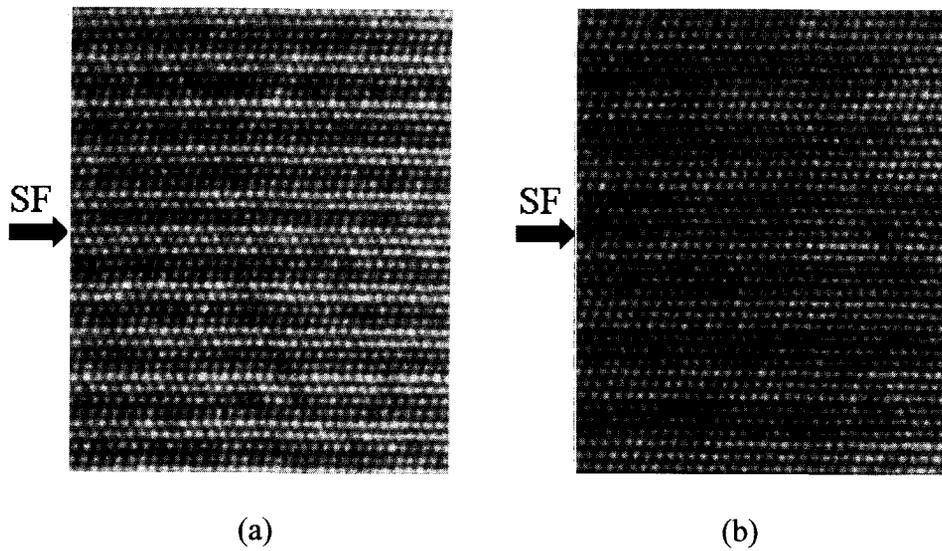


Fig. 1 High resolution TEM images of recombination-induced stacking faults in (a) 4H-SiC and (b) 6H-SiC high voltage diode.

References:

- ¹ H. Lendenmann, F. Dahlquist, N. Johansson et al., *Mater. Sci. Forum* **353-356**, 727 (2001).
- ² J. P. Bergman, H. Lendenmann, P. A. Nilsson et al., *Mater. Sci. Forum* **353-356**, 299 (2001).
- ³ K. Maeda, K. Suzuki, S. Fujita et al., *Phil. Mag. A* **57** (4), 573 (1988).

Electrical characterization of high-voltage 4H SiC diodes on high-temperature CVD grown epitaxial layers

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Silicon Carbide power devices designed for blocking high voltages are known to require comparatively thick low-doped drift zones. Those regions are most often provided by epitaxial layers due to the comparatively high concentration of impurities still present in available bulk 4H silicon carbide material. The growth rate of conventional chemical vapour deposition (CVD) however is limited to a few micrometers per hour when the requirements for residual doping and surface morphology are as high as for base material in power device applications [1]. High-temperature chemical vapour deposition (HTCVD) in vertical chimney reactors has recently been developed and was shown to produce high quality epitaxial layers with low background doping and smooth surface morphology at growth rates of up to 100 $\mu\text{m}/\text{h}$ [2]. So far only limited results exist for the application of these epitaxial layers in electronic devices [3]. In this study high-voltage diodes of different types have been processed on two samples of HTCVD epitaxial layers.

The epitaxial layers were grown on a commercial 4H-SiC wafer (Cree, n-type $7.8 \cdot 10^{18} \text{ cm}^{-3}$) at Linköping University, Sweden and have a nominal epilayer thickness and net n-type doping of 60 μm , $\leq 2 \cdot 10^{14} \text{ cm}^{-3}$ (sample A) and 65 μm , $\leq 9 \cdot 10^{15} \text{ cm}^{-3}$ (sample B) measured by photoluminescence and Schottky barrier capacitance-voltage (CV) technique after growth. Sample A has an additional highly doped buffer layer grown underneath the low-doped epilayer to prevent electrical punch-through into the substrate.

Both Schottky and Al implanted pn diodes as well as merged pn/Schottky diodes (MPS diodes, [4]) were manufactured in a standard process developed at our institute [5]. A titanium-tungsten alloy was used both for the ohmic contact to the p-type implanted regions and the large area backside contact, as well as contact metal for the Schottky barriers. The diodes were equipped with different termination schemes to reduce edge effects under reverse bias operation [6]. Field rings were implanted simultaneously with the anode structures of both pn and MPS diodes through a wet etched beveled silicon dioxide mask. Field plates were formed in the contact metallization layer on top of a 2 μm thick silicon dioxide layer deposited in a CVD process using TEOS as precursor.

Forward operation of both pn and MPS diodes show distinct areas of negative resistance attributed to plasma injection into the low-doped drift zone. The forward voltage drop of a limited number of diodes was increasing when operated under a continuous current density above 100 A cm^{-2} for a couple of hours (see Fig. 1). Similar degradation was observed by Lendenmann et. al. [7] on pn diodes made of conventional CVD material.

The reverse leakage current was found to depend on the presence of up to $2 \cdot 10^4 \text{ cm}^{-2}$ surface defects of the half-moon type [2] (see Fig. 2) on the active area of the samples. Some pn diodes free of, or only containing a few surface defects and with working termination schemes have electrical breakdown above 3500 V while others containing surface defects show soft breakdown already at as low as 800 V (see Fig. 3).

- [1] O. Kordina, A. Henry, E. Janzén, and C.H. Carter, Jr.; Materials Science Forum vols.264-268(1998) pp.97-102
- [2] J. Zhang, A. Ellison, and E. Janzén; Materials Science Forum vols.338-342(2000) pp.137-140
- [3] Q. Wahab, E.B. Macák, J. Zhang, L.D. Madsen, and E. Janzén; Materials Science Forum vols.353-356(2001) pp.691-694
- [4] B.J. Baliga; IEEE Electron Device Letters EDL-8(1987) pp.407-409
- [5] U. Zimmermann, A. Hallén, and B. Breitholtz; Materials Science Forum vols.338-342(2000) pp.1323-1326
- [6] B.J. Baliga. "Power Semiconductor Devices", PWS Publishing(1995), ISBN 0-534-94098-6
- [7] H. Lendenmann et. al.; Materials Science Forum vols.353-356(2001) pp.727-730

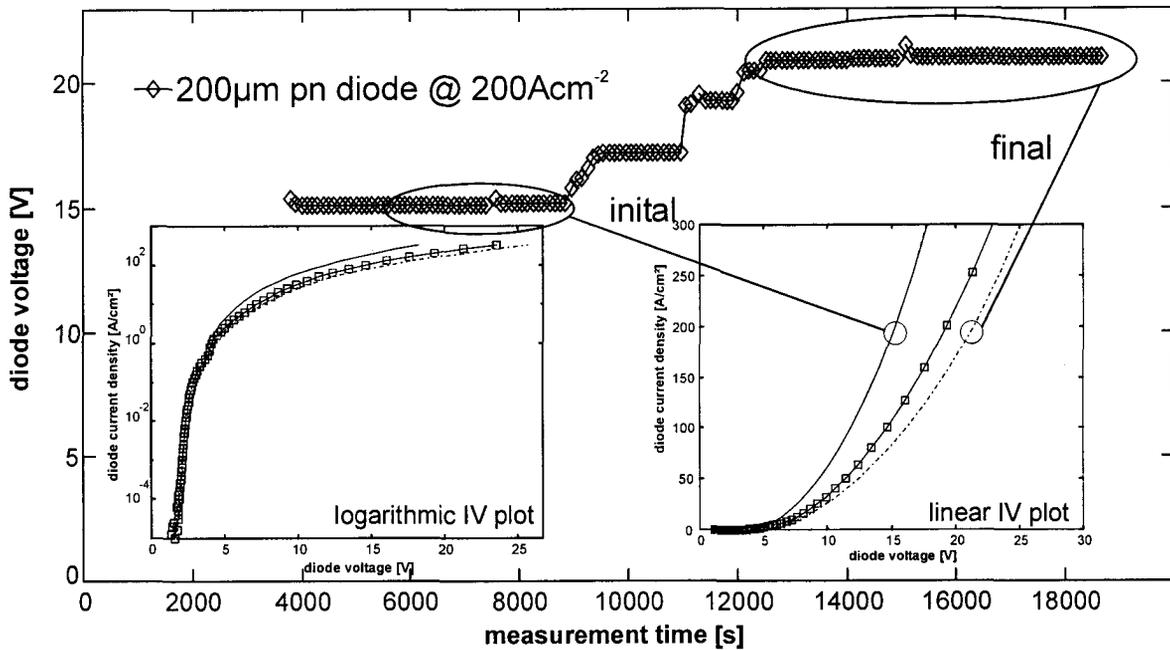


Figure 1: Long term stability measurement of the forward voltage drop of an implanted 200 μm diameter pn diode at a constant forward current density of 200 A cm⁻². Insets show static IV measurements at the indicated times.

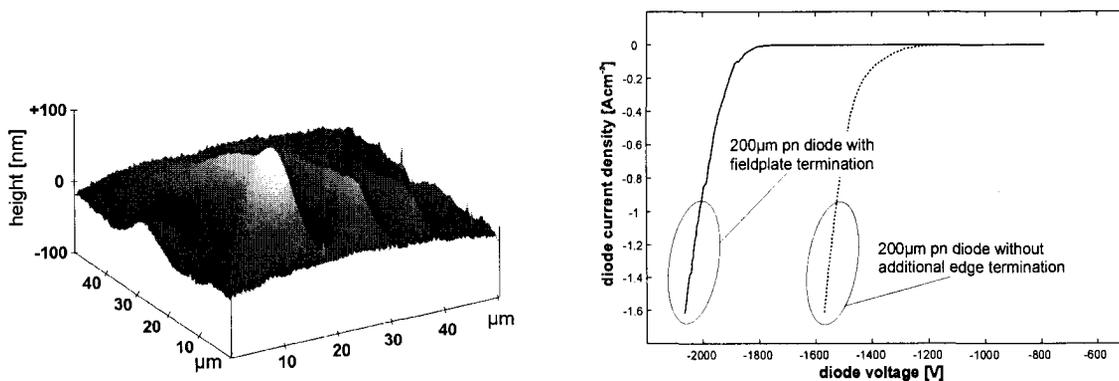


Figure 2: AFM micrograph of a surface defect of the half-moon type. The peak-to-valley height is about 200 nm, the lateral dimension typically $\geq 50 \mu\text{m}$.

Figure 3: Reverse breakdown of two pn diodes with 200 μm diameter. The fieldplate terminated diode contains 4 single half-moon defects in its active area.

Investigation of thermal properties in fabricated 4H-SiC high power bipolar transistors

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Recent research on switch devices has been focused mainly on field effect devices (e.g. MOSFET, MESFET, and JFET). In contrast to this, only a few publications have been presented on SiC bipolar junction transistors (BJT) [1, 2]. One of the main reasons for this is the short minority carrier lifetime in p-type layers, which is detrimental to the current gain. However, as the material quality improves and epi layer growth develops, SiC bipolar transistors can be very competitive. As a switch element the bipolar transistor has the advantages of carrier modulation and better current capabilities compared to most FETs. In Thyristors and IGBTs, the main current flow has a pn-barrier to cross, resulting in an initial forward voltage-drop almost equal to the built-in voltage (~ 3 V for 4H-SiC). In comparison, the BJT switch device has junction cancellation between the emitter and collector, which results in a lower initial voltage drop over the switch [3]. In the study reported here a 4H-SiC BJT was fabricated using an etched mesa structure from an epi layer stack. The doping and epi layer thicknesses were designed for high voltage operation (~ 1.5 kV parallel breakdown), see schematic device structure in Fig. 1. Measurements of the fabricated transistors were performed with a HP4156 and a probe station equipped with a hot chuck, allowing measurements up to temperatures of 300 °C.

The measured transistors showed a strong self-heating effect when the power dissipation was increased, which led to a lowered current gain. This temperature dependence was investigated with relatively small self-heating conditions ($V_{CE} = 20$ V), and the current gain decreased from 10 at 25 °C to 6 at 300 °C. By assuming that the current gain only depends on temperature, the junction temperature can be extracted from three V_{CE} -diagrams at three different temperatures on the heat sink at the backside contact [4]. This extraction technique was used on the fabricated transistors at heat sink temperatures of, 25 °C, 50 °C, 75 °C, see Fig. 2. The extracted junction temperature at $I_C = 60$ mA was 120 °C, which is approximately 100 °C above the heat sink temperature. In addition, the total thermal resistance to the heat sink was estimated to 27 K/W at 25 °C. The measured device in Fig. 2 had an emitter area of $1.5 \cdot 10^{-4}$ cm² (i.e. 50 mA corresponds to 333 A/cm²).

Furthermore, thermal device simulations have been performed in order to investigate the origin of the current gain reduction, and also to confirm the thermal dependence in the included device simulation models. The measured data presented in Fig. 2 has a much steeper drop in current gain (β), in comparison with a temperature dependent simulation with models taken from [5] and [6]. In this work various simulation geometries and models have been investigated to explain the thermal behavior (e.g. 3D-simulation, surface recombination, Auger recombination, and temperature dependent life-times). The model parameters are taken from literature, and a discussion on minor adjustments of these values is undertaken. Furthermore, pulsed measurements are compared with transient simulations in order to investigate the self-heating transients, which have been shown to be very fast in SiC.

- [1] Y. Luo, L. Fursin and J. H. Zhao, *Electron. Lett.* 36 (2000), p. 1496.
- [2] S.-H. Ryu, A. K. Agarwal, R. Singh and J. W. Palmour, *IEEE Elec. Dev. Lett.* 22 (2001), p. 124.
- [3] T. P. Chow, V. Khemka, J. Fedison, N. Ramungul, K. Matocha, Y. Tang and R. J. Gutmann, *Solid-State Electron.* 44 (2000), p. 277.
- [4] S. P. Marsh, *IEEE Trans. Electron Devices* 47 (2000), p. 288.
- [5] M. Bakowski, U. Gustavsson and U. Lindefelt, *Phys. stat. sol. (a)* 162 (1997), p. 421.
- [6] U. Lindefelt, *J. Appl. Phys.* 84 (1998), p. 2628.

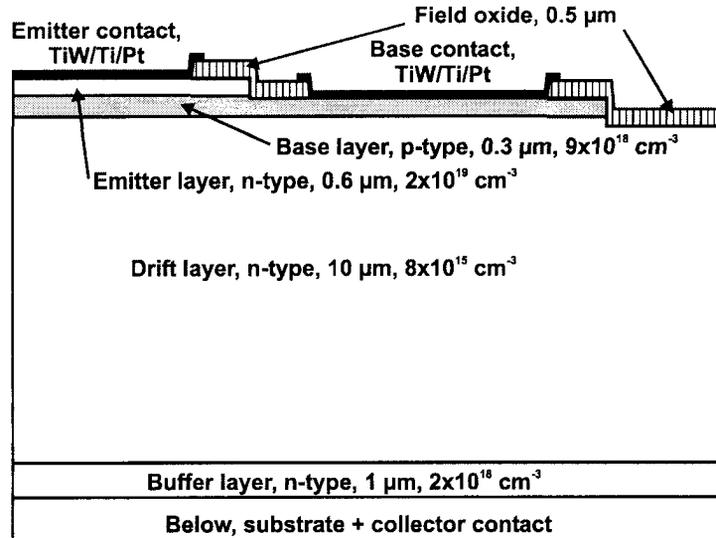


Fig. 1. A schematic cross-section of the fabricated devices.

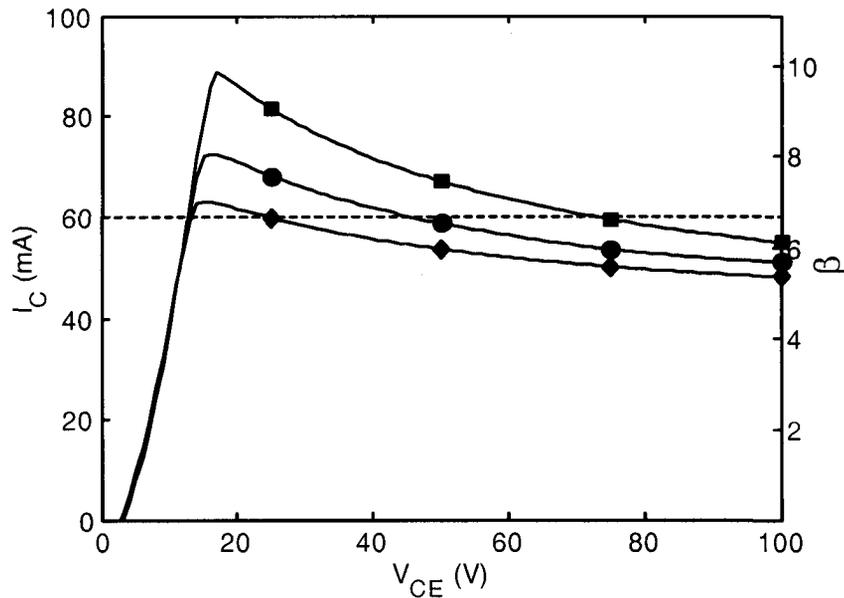


Fig. 2. Measured V_{CE} -diagrams at three different temperatures, ■ 25 °C, ● 50 °C, and ◆ 75 °C. The intersections with the dashed line was used for the extraction of $T_j = 120$ °C.

Improvement and Analysis of Implanted-Emitter Bipolar Junction Transistors in 4H-SiC

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SiC has long been recognized as the choice for high voltage, high temperature, high power applications. Significant progress has been made in SiC bipolar junction transistors, most of which on epi-emitter BJTs [1-4]. The implanted-emitter BJTs offer ease of controlling base width by varying the emitter implants. We reported the first implanted-emitter BJT in 4H-SiC [5]. The device showed a record-high common emitter current gain of 40, and forward drop of 1V at 50A/cm². The open-base breakdown voltage was less than 60V due to base punch through. In this work, high voltage, implanted-emitter, npn BJTs were fabricated. Different emitter implantation species and annealing cycles were used to study the effect of emitter implant. The devices showed maximum blocking voltage of 500V and common emitter current gain of 8.

The device cross-section is shown in Fig. 1. The starting wafers were (0001), Si face, P⁺/P/N/N substrate wafers. The top P⁺ epi layer ensures good P-base contact and also avoids high temperature anneal of P⁺ implant. The emitter was formed by implanting into P-base region at 600°C using five successive implants. Four samples were fabricated with different implantation species and annealing cycles, but all with the same dose of 3×10¹⁵ cm⁻². The implantation splits and the measured sheet resistances are shown in table 1. Previous study has shown that low sheet resistance can be obtained for phosphorus and arsenic when annealed at 1200°C [6,7].

The distribution of the common emitter current gain of the four samples and their medians are shown in Fig. 2. At room temperature, maximum common emitter current gain of 8 was measured on 300 μm×300 μm devices of sample C with phosphorus implantation and 1600°C anneal. Fig. 3 shows the effect of emitter periphery on current gain for sample C, it is seen that current gain increases proportionally with the increase of emitter periphery. At high temperature, specific on-resistance increases as shown in Fig. 4, making this device attractive for paralleling and for preventing thermal run-aways. The reason is that base carrier concentration increases at high temperature due to increased ionization of deep level acceptors. As a result, β decreases with temperature, leading to the increase of specific on-resistance at high temperatures. This feature was also observed in the previous samples [5].

The distribution of the open-base breakdown voltages of the four samples are shown in fig. 5. The As sample does not have a high blocking voltage. The majority of the other samples show BV_{CEO} ranging from 100V to 500V, the highest blocking is 550V. The increase of the breakdown voltage and the decrease of the current gain are both due to the increased base width.

Fig. 6 shows the open-base turn-off transient of sample A and sample C. During open-base turn-off, the device is turned off mainly by recombination. The turn-off time is ~ 1 μs.

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References:

- [1] W. von Munch et al, Solid-state electronics, vol. 21, no. 2, pp. 479-80, 1978.
- [2] Y. Wang et al, Silicon Carbide and Related Materials Conf, pp. 809-812, Kyoto, 1995.
- [3] S-H. Ryu et al, IEEE Electron Device Letters, vol. 22, no. 3, pp. 124-6, 2001.
- [4] Y. Luo et al, Electronics Letters, vol. 36, no. 17, pp. 1496-1497, 2000.
- [5] Y. Tang et al, IEEE Electron Device Letters, vol. 22, no. 3, pp. 119-20, 2001.
- [6] V. Khemka et al, Journal of Electronic Materials, Vol. 28, No. 3, pp. 167-174, 1999.
- [7] J. Senzaki et al, Silicon Carbide and Related Materials Conf, vol. 338-342, pp. 865-868, 1999.

TABLE I Emitter implantation splits and measured sheet resistance

Sample	Emitter implant species	Annealing temperature (°C)	Annealing time (min)	Sheet resistance (Ω/sq)
A	Nitrogen	1600	15	3000
B	Arsenic	1200	30	3400
C	Phosphorus	1600	15	230
D	Phosphorus	1200	30	1200

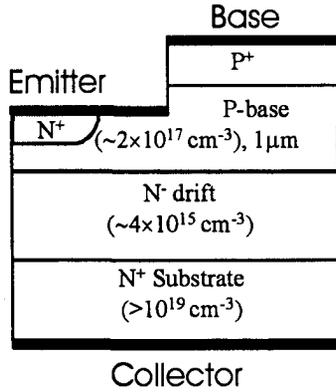


Fig.1 Schematic cross-section of implanted-emitter 4H-SiC BJT studied in this work

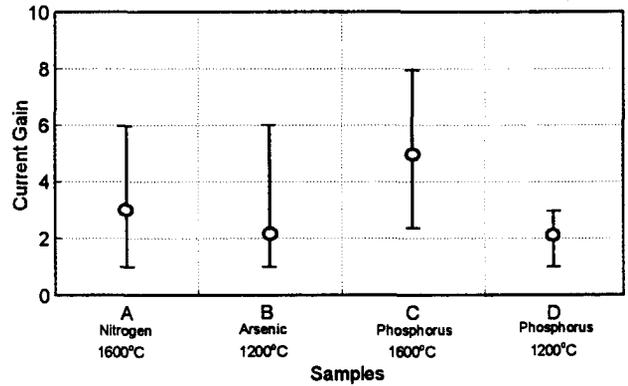


Fig.2 Distribution and median of maximum common emitter current gain at $V_{ce}=10V$

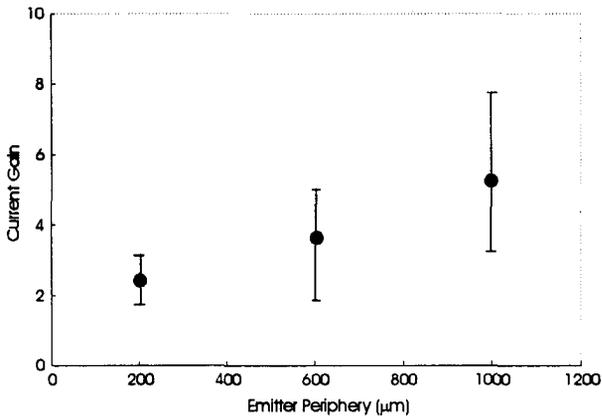


Fig.3 Effect of emitter periphery on current gain of sample C

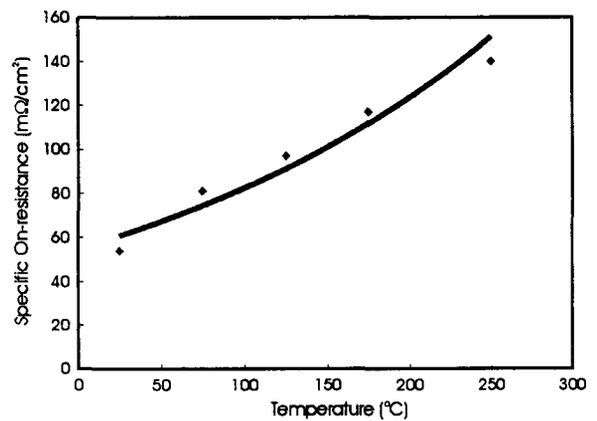


Fig.4 Temperature effect on specific on-resistance of sample C

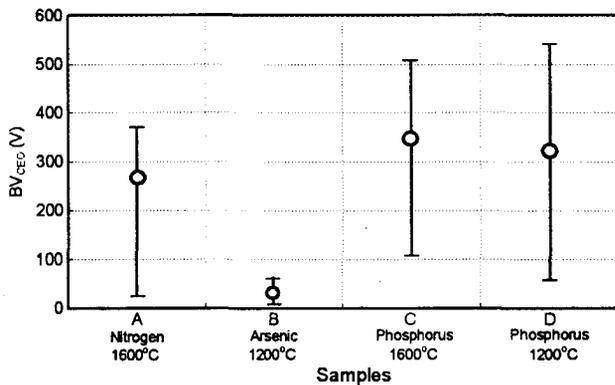


Fig.5 Distribution and median of open-base breakdown voltage

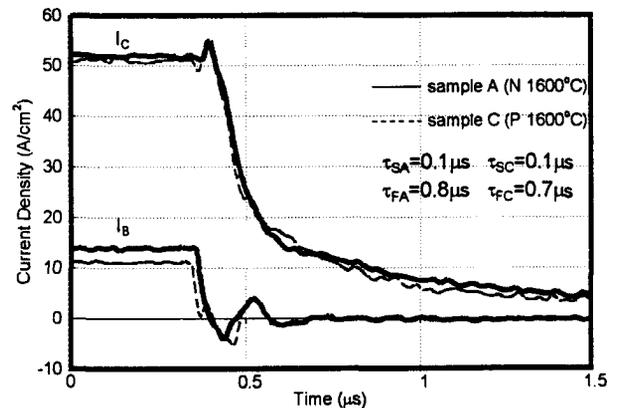


Fig.6 Open-base turn-off transient of sample A and C at room temperature

All-SiC Half-Bridge Inverter Characterization of 4H-SiC Power BJTs Up To 400V-22A

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SiC BJT has the advantage of being free of gate oxide, which makes it suitable for applications under high temperatures (over 150 –200 C). It is also a better candidate for many high temperature applications when compared to the latch-on SiC GTOs. 6H-SiC BJTs capable of blocking 50V were first fabricated and measured up to 0.8mA with a current gain of 4~8 in 1978 [1]. The first 4H-SiC power BJT was reported in 2000 with a capability of 800V-2.7A and a current gain of 9 [2]. High gain and high voltage 4H-SiC BJTs were subsequently reported [3,4], showing increased interests in 4H-SiC power BJTs. In this paper, we report BJTs fabricated in 4H-SiC with emitter current measured up to 16A (312A/cm²) with a maximum common emitter current gain of 7. Blocking voltage BV_{CEO} measured up to 600V is achieved, with some devices blocking more than 900V.

The 4H-SiC wafer used for the BJT fabrication is purchased from Cree Inc. Fig. 1 shows a section of the cross sectional view of the BJT structure. The BJTs have six 96μm x 990μm emitter fingers surrounded by seven base fingers. The base-emitter spacing is 6 μm. The total collector area, including the three MJTE regions, is 1.57x1.66 mm². The BJT p-base is ion implanted with Al and C co-implantation to 6x10²⁰cm⁻³ to reduce base contact resistance. To improve device blocking capability, the base-collector junction is terminated by multi-step junction termination extension (MJTE), as shown in Fig.1. After MJTE etching, sacrificial oxide and about 40nm of passivation oxide is grown thermally followed by 1 μm LPCVD SiO₂. Then oxide window is opened. Al/Ti/TiN multiple-layer base contact metal is sputtered and patterned by lift-off. Emitter contact metal (Ni) is then sputtered after opening the emitter oxide window. Following Ni sputtering onto the backside of the samples, all the contacts are annealed in nitrogen forming gas (5% H₂ in N₂) at 1050°C for 5 min. The multi-cell BJTs are packaged in nitrogen ambient at 390°C and Au ribbon bonding is conducted at 180°C.

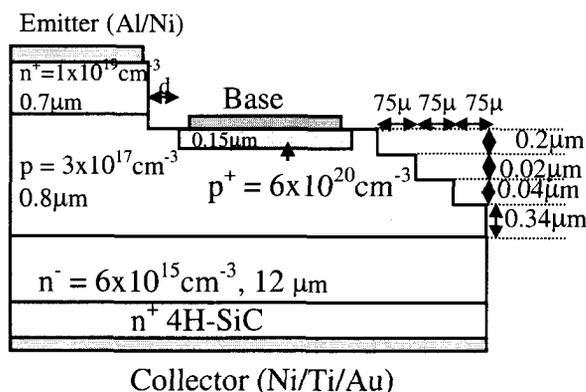


Fig.1 Cross-sectional view of BJT structure

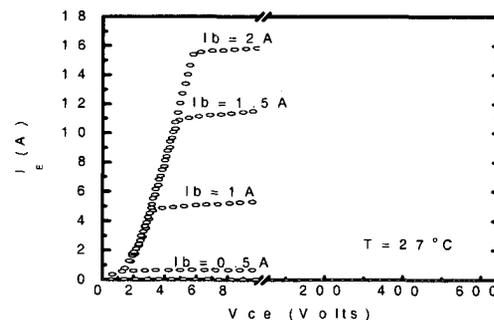


Fig.2 I_c-V_{ce} characteristics of 4H-SiC npn BJT

Fig.2 shows the common emitter I_E vs. V_{CE} characteristics at room temperature for a packaged BJT with 9 cells in parallel. The BJT shows a common emitter current gain I_C/I_b of 7 with a

forward blocking voltage (BV_{CEO}) measured up to around 600V. The DC emitter current is measured up to 16A at a base current of 2 A, corresponding to an emitter current density of 312 A/cm². Poor sidewall passivation and surface recombination contribute to the first 2V drop without current gain. Low carrier diffusion length in base region and low conduction modulation in the drift region may partly contribute to the large voltage drop at high current ($I_E=15.5$ A with $V_{CE} = 5.8$ V). The large emitter size is designed for high quality 4H-SiC with long minority carrier lifetimes. With the base minority carrier lifetime still quite low (sub-microsecond), current crowding and low carrier diffusion length reduce area efficiency of the emitter. Devices with smaller cell pitch sizes are being processed and the result will be reported.

The packaged 4H-SiC BJTs have been tested in an all-SiC inductively loaded half-bridge inverter by using 4H-SiC MPS diodes as the free-wheeling diodes. The inductive load used in the switching measurements is chosen to be as high as 1 mH to simulate a high power AC induction motor. Fig.3 shows 400V-22A switching waveforms of SiC BJT with a base driving current around 3 A. The effect of SiC MPS diodes on the SiC BJT switch turn-on loss is shown in Fig.4. It is seen that, when compared to the ultrafast commercial Si PiN free-wheel diodes, 4H-SiC MPS diodes result in reduced SiC BJT switching loss. Further measurements are underway to compare all-SiC half-bridge inverter BJT turn-on and turn-off losses with Si-IGBT based half-bridge inverters. The results will be reported.

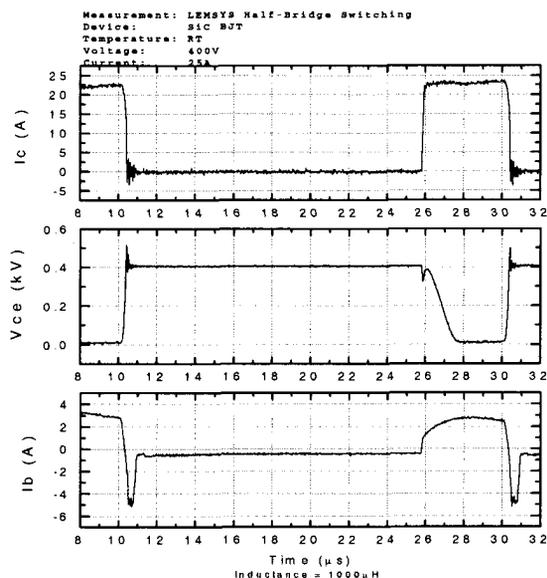


Fig. 3 Half-bridge inverter switching waveforms for the 4H-SiC BJT.

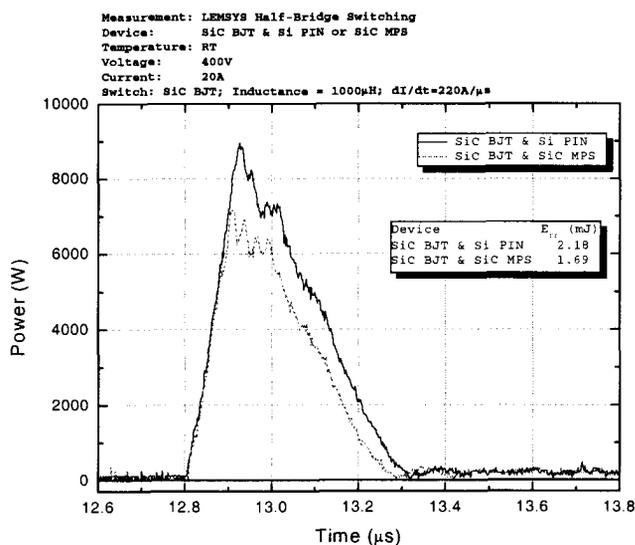


Fig.4 Turn-on power loss of 4H-SiC BJT in a half-bridge inverter using either Si PiN or SiC MPS free-wheeling diodes.

References:

- [1]. Muench, W. V. and Hoeck, P.: ' Silicon Carbide bipolar transistor', *Solid-State Electronics*, 1978, 21, pp.479-480.
- [2]. Luo, Y., Fursin, L. and Zhao, J.: ' Demonstration of 4H-SiC power bipolar junction transistors', *IEE Electronics Letters*, 2000, 36, No.17, pp.1496-1497.
- [3]. Ryu, S., Agarwal, A.K., Singh, R. and Palmour, J. W.: ' 1800V NPN Bipolar Junction Transistors in 4H-SiC', *IEEE Electron Device Letters*, 2001, 22, No.3, pp.124-126.
- [4]. Tang, Y., Fedison, J.B. and Chow, T.P.: ' An Implanted-Emitter 4H-SiC Bipolar Transistor with High Current Gain', *IEEE Electron Device Letters*, 2001, 22, No.3, pp.119-120.